FastFLASH™ XC9500XL 3.3 V CPLD Family

December, 1997 (Version 1.0) Advance Product Information

Features

- Optimized for high-performance 3.3 V systems
  - 4 ns pin-to-pin logic delays, with internal counter frequency to 200 MHz
  - In-system programmable exceeding 10,000 program/erase cycles
  - Small footprint packages including VQFPs, TQFPs and CSPs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Six pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6,400 usable gates
- Advanced system features
  - Superior routability with FastCONNECT II™ switch matrix
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Flexible clock structure with 3 global clocks and individual product-term clocks
  - Individual output enable per output pin
  - User programmable ground pin capability
  - Input hysteresis on all user and boundary-scan pin inputs
- Fast concurrent programming of multiple XC9500XL devices in boundary-scan chain
- Slew rate control on individual outputs
- 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
- 3.3 V or 2.5 V output capability
- Enhanced data security and integrity features
- Advanced 0.35 micron CMOS FastFLASH™ technology
- Pin-compatible with 5 V-core XC9500 family in common package footprints

Family Overview

The FastFLASH XC9500XL family is a 3.3 V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where minimizing board space and power dissipation is important. Each XC9500XL device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XL family is designed to work closely with the Xilinx XC4000X and derivative FPGA families, allowing system designers to optimally partition logic between fast interface circuitry and high-density general purpose logic.

Architecture Description

The XC9500XL family is a 3.3 V-core derivative of the popular 5 V-core XC9500 family. Each XC9500XL device comprises versatile 18-macrocell Function Blocks (FB) interconnected by an enhanced FastCONNECT II switch matrix (see Figure 1). Each Function Block consists of an AND-array, which provides 90 product terms arranged as groups of five assigned to each of 18 macrocells. Flexible product term allocators allow product terms to be allocated to specific macrocells on an individual product-term basis, allowing any number of product terms (up to a maximum of 90) to drive a macrocell.

Each macrocell can also select between global or product term signals for clocks, 3-state enable, set, and reset. The XC9500XL architecture also provides for a product term-based clock-enable signal into each register.

Small Footprint Packages

The XC9500XL family supports VQFPs, TQFPs and CSPs (Chip Scale Packages) to address tight space contraints. Boundary-scan capability allows superior solder ball contact check and internal node observability during system verification and debug.

Process Technology

The 0.35 micron FastFLASH process is used to fabricate all devices in the XC9500XL family. It supports 3.3 V program/erase, high-performance logic capability, and endurance of 10,000 program/erase cycles. The FastFLASH process is compatible with industry-leading flash processes for continued process scalability.

Development System

Like the current XC9500 family, the XC9500XL family will be supported in all Xilinx development systems, including the push-button Foundation series and versatile Alliance series of Xilinx development systems. Designers can create the design using schematics, equations, VHDL or other HDL languages, and run device and system simulations in a variety of software environments. Device programming can be done with the supplied cable, an embedded microcontroller, or automatic test equipment.

Additional Information

Please check the Xilinx home-page on World Wide Web for the latest information on this family: http://www.xilinx.com.

Table 1: XC9500XL Planned Device Family

	XC9536XL	XC9572XL	XC95108XL	XC95144XL	XC95216XL	XC95288XL
Macrocells	36	72	108	144	216	288
Usable Gates	800	1,600	2,400	3,200	4,800	6,400
Registers	36	72	108	144	216	288
Pin-to-pin Delay tPD (ns)	4	5	5	5	6	6
Planned QFPs	44-pin VQFP 64-pin VQFP	44-pin VQFP 64-pin VQFP 100-pin TQFP	100-pin TQFP 144-pin TQFP	100-pin TQFP 144-pin TQFP	144-pin TQFP 208-pin TQFP	208-pin TQFP
Planned CSPs* (body dimension in mm)	48-pin CSP (7mm x 7mm)	160-pin CSP (10 x 10)	160-pin CSP (10 x 10)	160-pin CSP (10 x 10)	240-pin CSP (14 x 14)	240-pin CSP (14 x 14)

*Note: Please contact your sales representative for additional information on the availability of chip-scale packages.

Figure 1: XC9500XL Architecture
Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

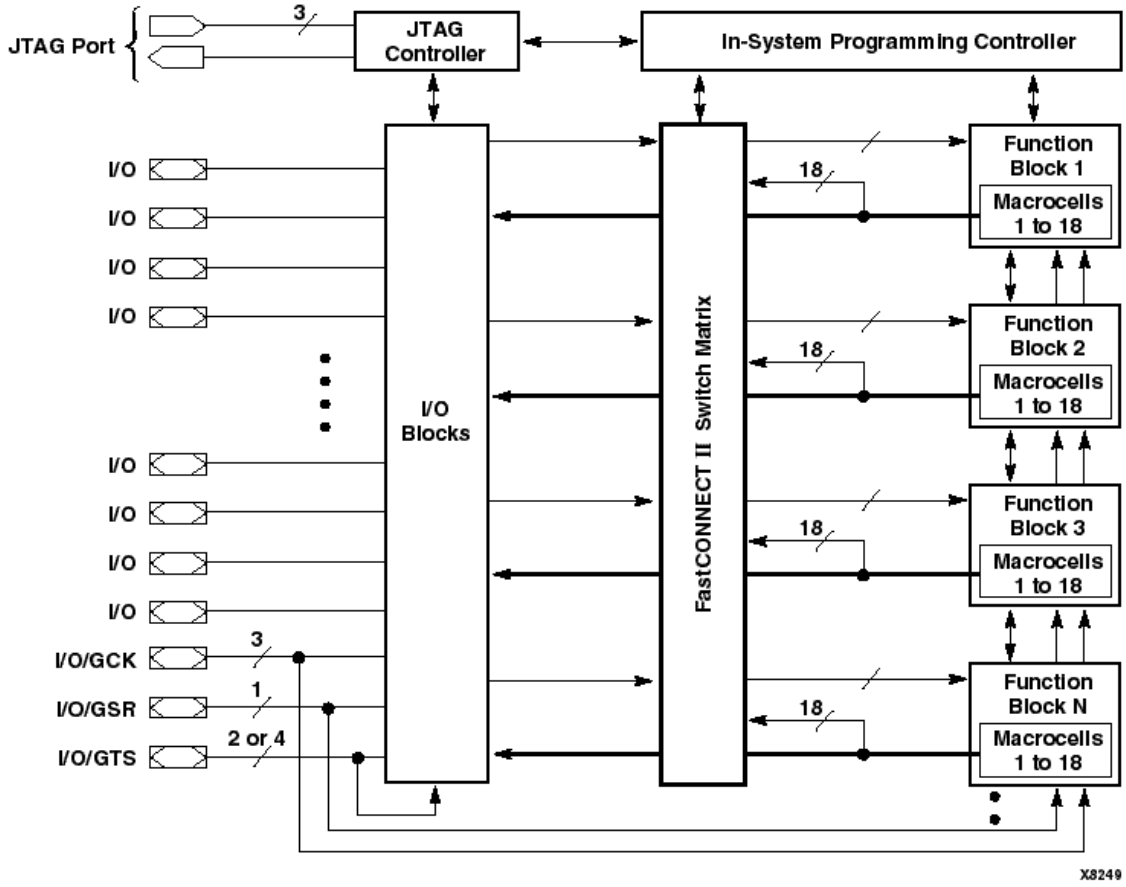

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Figure 2: XC9500XL Macrocell Within Function Block