Ann Duft
Xilinx, Inc.
(408) 879-4726
publicrelations@xilinx.com

Kathy Keller
Oak Ridge Public Relations
(408) 253-5042
kathy.keller@oakridge.com

FOR IMMEDIATE RELEASE

XILINX ANNOUNCES NEWEST MEMBER

OF INDUSTRY'S FASTEST GROWING CPLD FAMILY

New XC95144 device targets sweet spot of ISP CPLD market with lowest price per macrocell

SAN JOSE, Calif., May 6, 1998—Xilinx, Inc., (NASDAQ:XLNX), announced today it will begin volume shipments this month of the newest member of the 5-volt XC9500 family of aggressively priced CPLDs. The XC95144 device, with a 7.5 ns pin-to-pin speed, is the first member built on a new advanced process technology. This device completes the company's popular ISP family and, with 144 macrocells, it addresses the designers' needs in the density sweet spot of the CPLD market.

The XC95144 device is the first CPLD using an advanced FastFLASH process technology from United Semiconductor Corporation (USC), Taiwan. During 1998, all other members of the XC9500 family will be transitioned to this new process, which offers more than a 50 percent die size reduction compared to the initial 0.6-micron process. The die size reductions afford lower cost thereby allowing Xilinx to offer the lowest priced, high-performance CPLDs on the market.

"Offering our customers more efficiently engineered silicon on advanced process technology is paramount to our leading-edge technology strategy," said Evert Wolsheimer, vice president and general manager of the Xilinx CPLD division. "We are setting the price standard in the CPLD market with the lowest price per macrocell available from any CPLD vendor."

Customers spoiled by easy ISP

"The compelling design advantages of a mature in-system programmable technology combined with the promotional pricing of the Foundation Series tools made the change to Xilinx and the XC9500 CPLD family an easy choice. We've completed one design, a complex board with several XC9500 devices, and have started another project which will have multiple XC9500 devices per card," said Howard Katz, engineer, from Anatek,

Ann Duft
Xilinx, Inc.
(408) 879-4726
publicrelations@xilinx.com

Kathy Keller
Oak Ridge Public Relations
(408) 253-5042
kathy.keller@oakridge.com

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XILINX ANNOUNCES SMALLEST PACKAGING TECHNOLOGY FOR CPLDS IN SMALL FORM-FACTOR APPLICATIONS

New chip scale packaging, available in 0.8-mm pitch, is three times smaller than thin quad packaging

SAN JOSE, Calif., May 4, 1998—Leading the industry in packaging technology, Xilinx, Inc., (NASDAQ:XLNX), announced new chip scale packaging available for its XC9536 complex programmable logic device (CPLD). Xilinx is the first non-memory manufacturer, and programmable logic supplier, to have chip scale packaging (CSP) technology available now. This package is ideally suited for a growing number of applications such as PCMCIA cards, PC boards, PC add-in cards, and many portable and wireless designs.

Chip scale packaging is an ultra-miniature IC package, approximately 20 percent larger than the size of the die, with a ball-pitch less than one millimeter. The first Xilinx CSP with 48 pins has a seven-millimeter by seven-millimeter ball array configuration using a 0.8-millimeter solder ball pitch. The 0.8-mm technology defines chip scale packaging and measures the pitch width from one solder ball to the other on the bottom on the package. Package technologies measuring greater than 0.8 millimeters are considered ball grid arrays. The footprint of the Xilinx 48-pin CSP is three times smaller than the 44-pin very thin quad (TQ44) package and 40 percent smaller than the 48-pin thin quad (TQ48) package.

“Our very popular XC9536 device, in this new 48-pin chip scale package, contains the same amount of logic as a 44-pin PLCC but in a package that is roughly the same size as the head of a pencil,” said Evert Wolsheimer, vice president and general manager of the CPLD division. “CSP growth is expected to grow quickly due to the increasing demand in wireless and portable design applications requiring the in-system programming of our CPLD FastFLASH products. Xilinx is prepared to meet this demand involving future CPLD families and we are also anticipating putting our FPGAs into CSP technology later this year.”

Manufacturers who require extremely small form factor packages for applications such as video games, handsets, and PCMCIA applications can now take advantage of the time-to-market flexibility

–more–

Ann Duft
Xilinx, Inc.
(408) 879-4726
ann.duft@xilinx.com

Frankie Borison
Oak Ridge Public Relations
(408) 253-5042
frankie@oakridge.com

FOR IMMEDIATE RELEASE

XILINX SHIPPING LARGEST MEMBER OF ISP CPLD FAMILY

SAN JOSE, Calif., August 6, 1997—Xilinx, Inc., (NASDAQ:XLNX), today announced it has begun volume shipments of the newest member of the XC9500 family of aggressively-priced complex programmable logic devices (CPLDs) combining FLASH technology and an advanced architecture with in-system programming (ISP) capability. This largest member of the Xilinx CPLD family has 288 macrocells.

Five members now comprise the XC9500 CPLD family—the XC9536, XC9572, XC95108, XC95216 and the XC95288 devices—and range in density from 36 to 288 macrocells in a variety of packages. The XC9500 family features an architecture optimized for pin-locking. Pin-locking is a necessity for digital designers who want to take advantage of the XC9500 family's in-system programming (ISP) capability that enables easier prototyping, simpler manufacturing, and remote equipment upgrades.

“Our customer are responding to the pricing and features of the XC9500 family,” said Evert Wolsheimer, vice president and general manager of the CPLD business unit. “Design wins are increasing at a high rate and we expect this to continue. As much as 30 percent of Xilinx’s total design wins are derived from this product line. The company's long-term success will depend on its ability to deliver a broad range of products as customers choose a single supplier for their programmable logic needs.”

Xilinx targets the innovative XC9500 family at ISP users, who constitute the fastest growing segment of the CPLD market. In the manufacturing process, for example, ISP permits the new Xilinx CPLDs to be programmed and tested as part of the production process. This eliminates the need for device programmers and helps prevent mechanical damage that can occur to CPLDs during the manual programming process. ISP also eliminates labeling, inventorying and assembling of unprogrammed parts

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Product Backgrounder
The XC9500 CPLD Family

Introduction

The XC9500 family is the third generation of CPLD products from Xilinx. It is targeted for system manufacturers who require the most complete in-system programming, test, and manufacturing capability to support the entire product life cycle. From initial prototyping, to system integration, manufacturing, and field upgrade, the XC9500 product provides a total support solution with fully integrated in-system operations using a standard IEEE 1149.1 boundary scan (JTAG). The XC9500 family also provides superior pin-locking capability necessary for unexpected changes during design iterations and field upgrades. By using FastFLASH technology, a revolutionary 5 V flash technology optimized for high performance CPLDs, the XC9500 provides a leadership endurance of 10,000 program/erase cycles. This allows the XC9500 devices to be used in applications requiring frequent field upgrades and reconfigurations.

In addition, the XC9500 family provides both performance and density by offering leading pin-to-pin propagation delays as fast as five ns and nine devices ranging in density from 800 to over 12,000 gates.

Product Life Cycle Support

The in-system programming capability can support all stages of the product life cycle. Unlike other competing products, the XC9500 device provides in-system programming capability throughout the full commercial operating range. This simplifies the programming requirements and allows more robust field upgrade operations. In addition to in-system programming, other product requirements are needed to support each of the product life cycle stages.

An editor's glance at the XC9500XL ISP CPLD family

Xilinx Ships First 0.35-micron 3.3-volt FLASH CPLDs

Leadership Speed, Cost, and Reliability Enable New Markets

The in-system programmable XC9500XL family is the first 3.3-volt CPLD family to offer substantially higher speed and lower cost than equivalent 5-volt devices. These features open new applications currently out of reach of CPLDs, such as communications and computing market segments, as well as penetrate new markets in consumer and automotive applications. The XC9500XL family has the fastest pin-to-pin performance, smallest die size, and highest level of in-system reliability of any CPLDs currently available. It is expected to further accelerate the CPLD industry technology switch to double-polysilicon FLASH technologies from the older single-polysilicon EEPROM technologies.

Process:

- highly scalable FastFLASH technology to 0.25-micron and 0.18-micron feature-sizes
- the first mainstream CPLDs to be shipping on a 0.35-micron feature-size technology
- FastFLASH technology employs 0.35-micron rules for the 4-layer metal as well as drawn transistor lengths, with 0.25-micron (L_{eff})

XC9500XL Product Features:

- first 3.3-volt CPLD product to deliver the highest available reliability characteristics available to JTAG ISP devices
  - ~ 20-year data retention and 10,000 endurance cycles—qualities normally associated with FLASH memory
  - ~ data retention that's twice as long and 100 times more reliable than other JTAG ISP CPLDs
- Highest performance: 4 nanoseconds pin-to-pin speed and 200 MHz system frequency
- Leading-edge CSP for small hand-held consumer applications; allows increased user programmability with the highest reliability at the lowest cost
- Ultra wide block fan-in of 54, for superior pin-locking characteristics
- Most product-terms per macrocell of 90
- Leading-edge I/O flexibility and compatible with 5-volt, 3.3-volt, and 2.5-volt signals
  - ~ input hysteresis on all pins and bus-hold circuitry for simple bus interfaces
- Most complete JTAG boundary-scan support with 8 instructions
- Fast concurrent programming times

Product availability:	**Macro cells**	**Maximum I/Os**	**Pin-to-pin delay (t_{PD})**	**System frequency (f_{SYS})**	**Price ***	**price per macrocell**
XC9536XL-10 (PC44)	36	34	4 ns	200 MHz	$1.20	$0.03
XC9572XL-10 (PC44)	72	72	5 ns	178 MHz	1.85	0.03
XC95144XL-10 (TQ100)	144	117	5 ns	178 MHz	5.65	0.04
XC95288XL-10 (TQ144)	288	168	6 ns	151 MHz	11.95	0.04

* Pricing for 100,000-plus unit quantities in mid-1999

Package options:

44-pin PLCC; 100-pin and 144-pin TQFP; 352-pin BGA; 208-pin PQFP; 48-pin and 144-pin CSP

Software support:

FastFLASH™ XC9500XL 3.3 V CPLD Family

December, 1997 (Version 1.0) Advance Product Information

Features

- Optimized for high-performance 3.3 V systems
  - 4 ns pin-to-pin logic delays, with internal counter frequency to 200 MHz
  - In-system programmable exceeding 10,000 program/erase cycles
  - Small footprint packages including VQFPs, TQFPs and CSPs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Six pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6,400 usable gates
- Advanced system features
  - Superior routability with FastCONNECT II™ switch matrix
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Flexible clock structure with 3 global clocks and individual product-term clocks
  - Individual output enable per output pin
  - User programmable ground pin capability
  - Input hysteresis on all user and boundary-scan pin inputs
- Fast concurrent programming of multiple XC9500XL devices in boundary-scan chain
- Slew rate control on individual outputs
- 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
- 3.3 V or 2.5 V output capability
- Enhanced data security and integrity features
- Advanced 0.35 micron CMOS FastFLASH™ technology
- Pin-compatible with 5 V-core XC9500 family in common package footprints

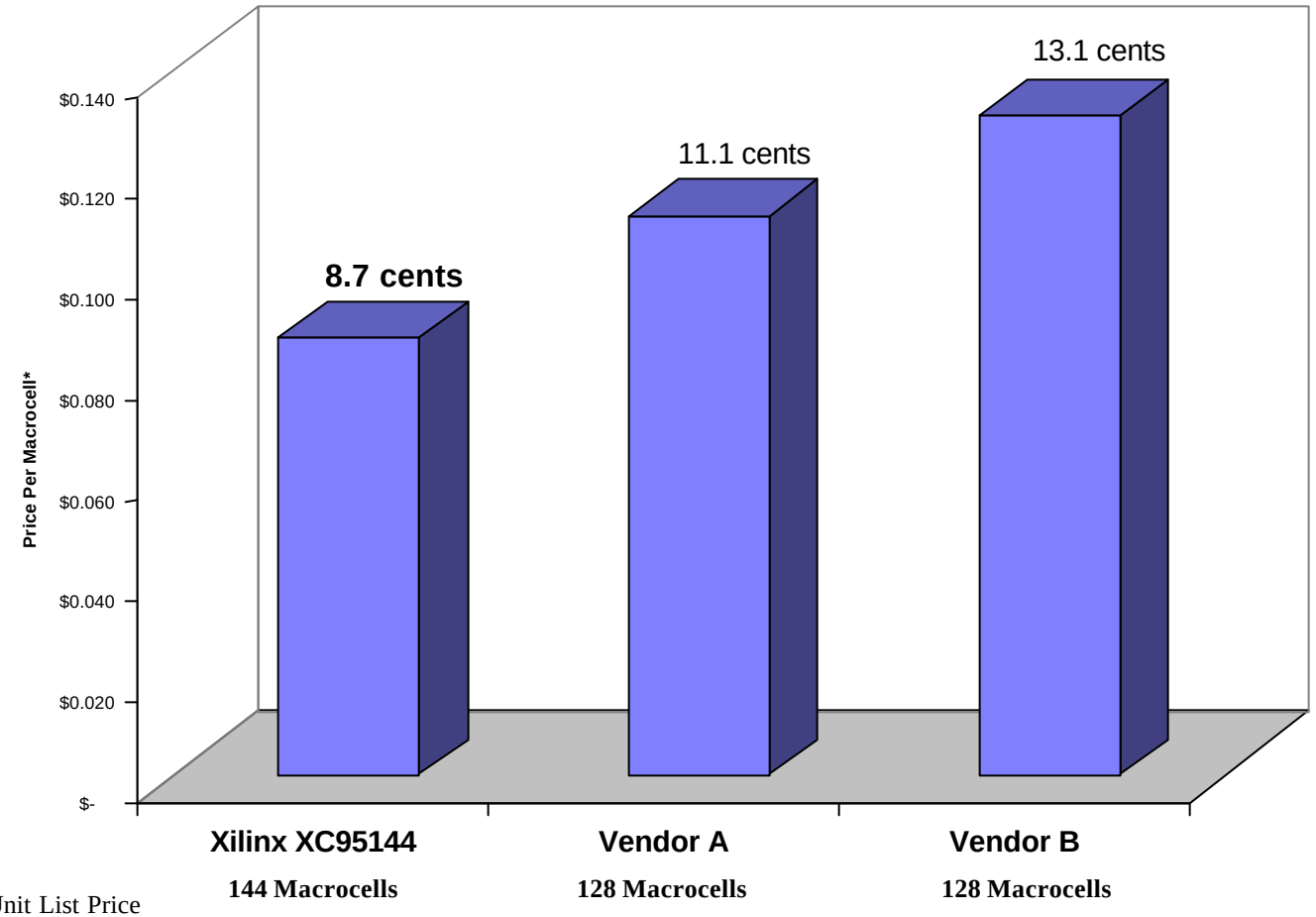
Family Overview

The FastFLASH XC9500XL family is a 3.3 V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where minimizing board space and power dissipation is important. Each XC9500XL device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XL family is designed to work closely with the Xilinx XC4000X and derivative FPGA families, allowing system designers to optimally partition logic between fast interface circuitry and high-density general purpose logic.

Architecture Description

The XC9500XL family is a 3.3 V-core derivative of the popular 5 V-core XC9500 family. Each XC9500XL device comprises versatile 18-macrocell Function Blocks (FB) interconnected by an enhanced FastCONNECT II switch matrix (see Figure 1). Each Function Block consists of an AND-array, which provides 90 product terms arranged as groups of five assigned to each of 18 macrocells. Flexible product term allocators allow product terms to be allocated to specific macrocells on an individual product-term basis, allowing any number of product terms (up to a maximum of 90) to drive a macrocell.

Lowest Price Per Macrocell In The Density Sweet Spot



*100+ Unit List Price

Source: Arrow Electronics Web Page, 4/29/98

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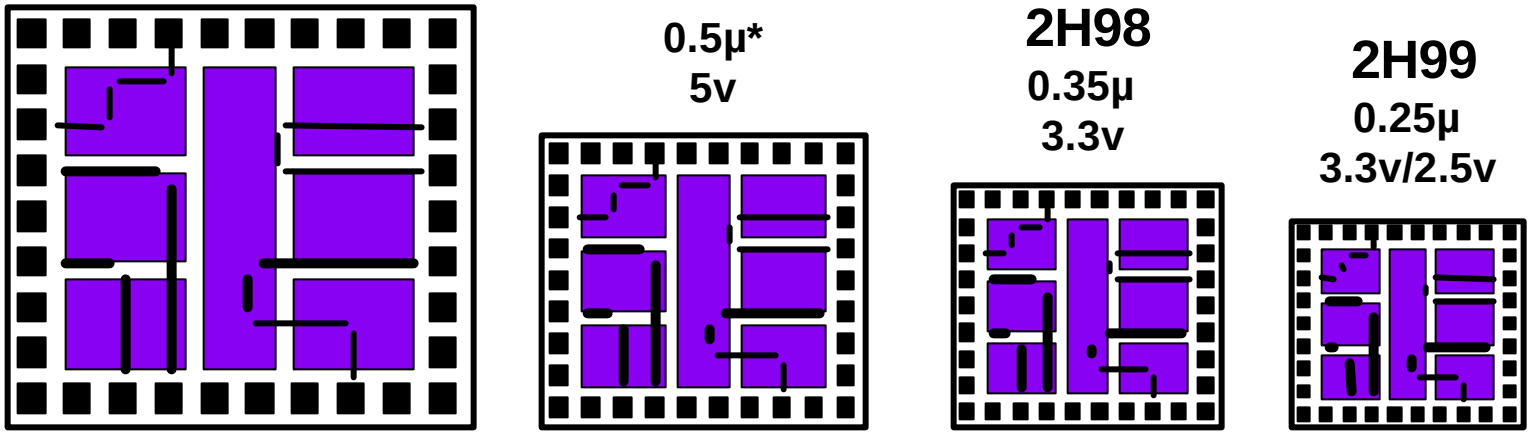
FLASH Technology Enables Rapid Die Size Reduction



Normalized Die Size:	**1.0**	**.5**	**.35**	**.26**

- 0.5µ transistor with 0.35µ interconnect

XILINX

Each macrocell can also select between global or product term signals for clocks, 3-state enable, set, and reset. The XC9500XL architecture also provides for a product term-based clock-enable signal into each register.

Small Footprint Packages

The XC9500XL family supports VQFPs, TQFPs and CSPs (Chip Scale Packages) to address tight space contraints. Boundary-scan capability allows superior solder ball contact check and internal node observability during system verification and debug.

Process Technology

The 0.35 micron FastFLASH process is used to fabricate all devices in the XC9500XL family. It supports 3.3 V program/erase, high-performance logic capability, and endurance of 10,000 program/erase cycles. The FastFLASH process is compatible with industry-leading flash processes for continued process scalability.

Development System

Like the current XC9500 family, the XC9500XL family will be supported in all Xilinx development systems, including the push-button Foundation series and versatile Alliance series of Xilinx development systems. Designers can create the design using schematics, equations, VHDL or other HDL languages, and run device and system simulations in a variety of software environments. Device programming can be done with the supplied cable, an embedded microcontroller, or automatic test equipment.

Additional Information

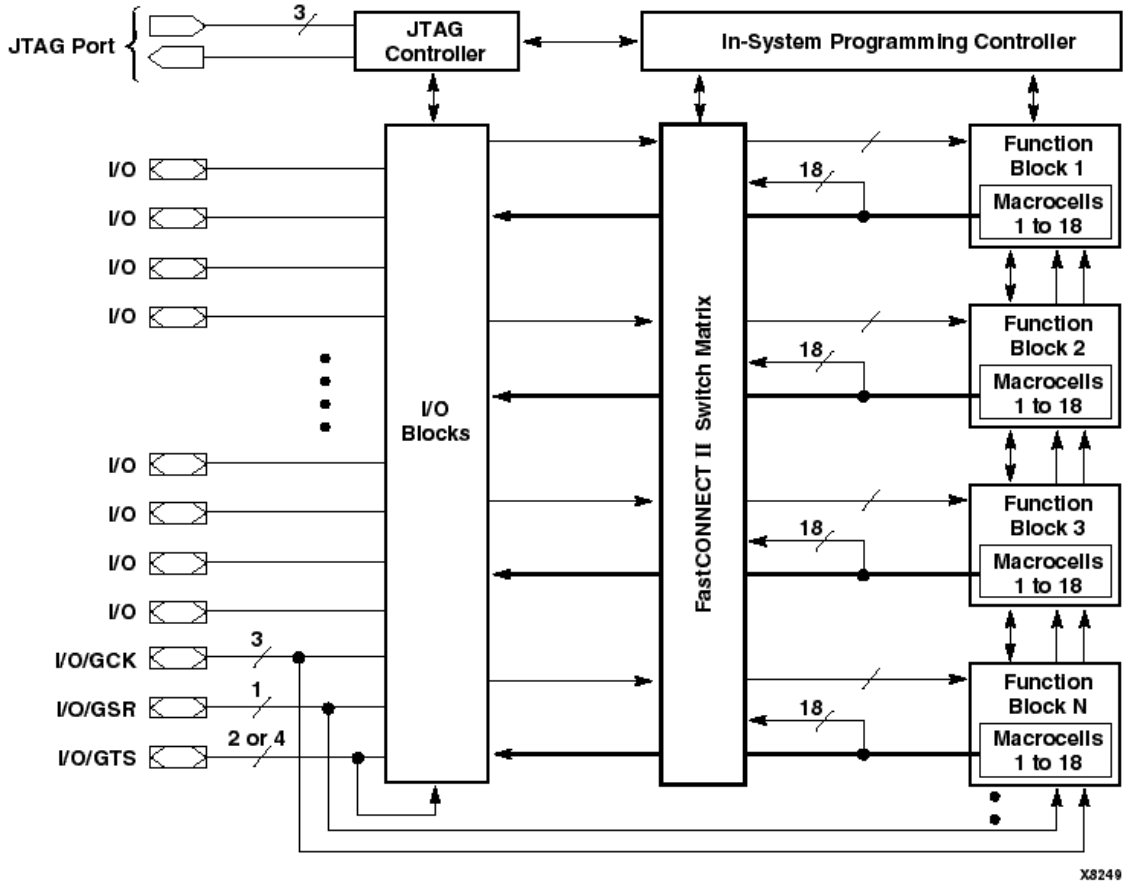
Please check the Xilinx home-page on World Wide Web for the latest information on this family: http://www.xilinx.com.

Table 1: XC9500XL Planned Device Family

	XC9536XL	XC9572XL	XC95108XL	XC95144XL	XC95216XL	XC95288XL
Macrocells	36	72	108	144	216	288
Usable Gates	800	1,600	2,400	3,200	4,800	6,400
Registers	36	72	108	144	216	288
Pin-to-pin Delay tPD (ns)	4	5	5	5	6	6
Planned QFPs	44-pin VQFP 64-pin VQFP	44-pin VQFP 64-pin VQFP 100-pin TQFP	100-pin TQFP 144-pin TQFP	100-pin TQFP 144-pin TQFP	144-pin TQFP 208-pin TQFP	208-pin TQFP
Planned CSPs* (body dimension in mm)	48-pin CSP (7mm x 7mm)	160-pin CSP (10 x 10)	160-pin CSP (10 x 10)	160-pin CSP (10 x 10)	240-pin CSP (14 x 14)	240-pin CSP (14 x 14)

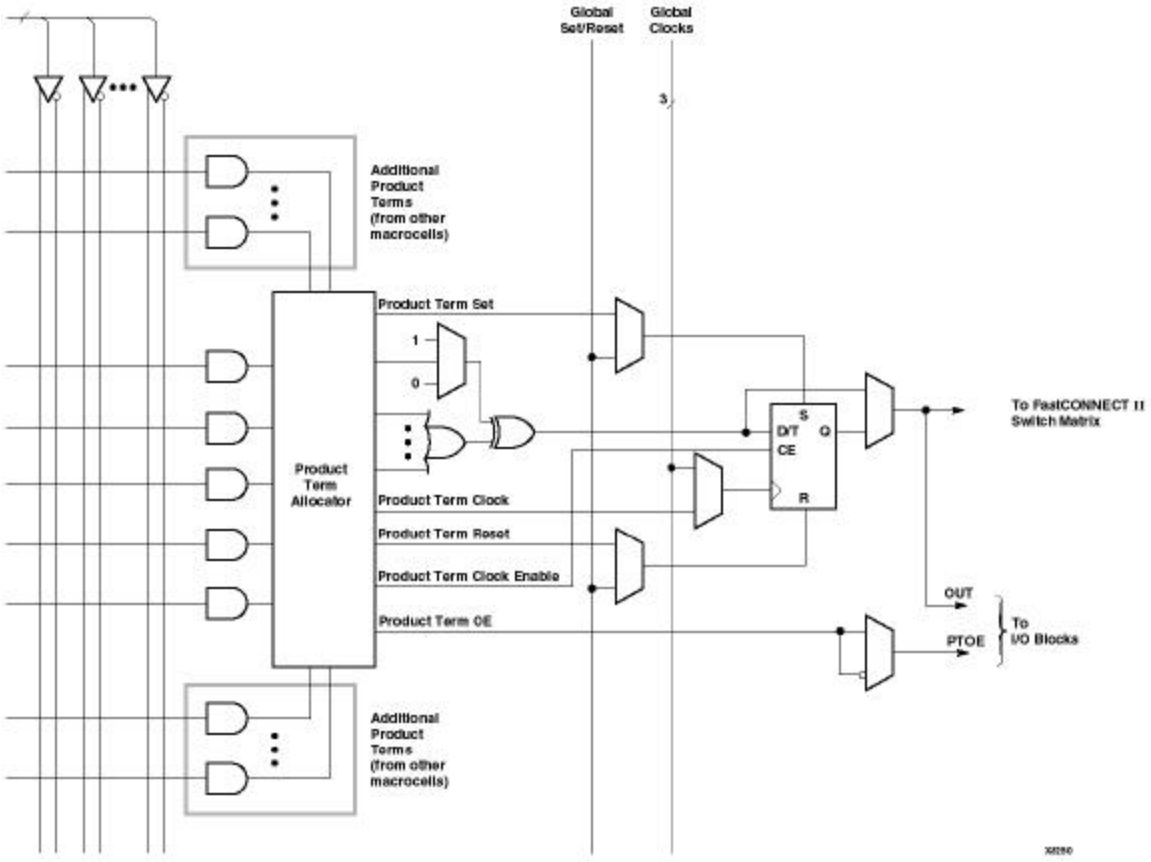
*Note: Please contact your sales representative for additional information on the availability of chip-scale packages.

Figure 1: XC9500XL Architecture
Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.



(OMIT THIS FIGURE)

Figure 2: XC9500XL Macrocell Within Function Block



The XC9500XL family is supported in the Foundation and Alliance Series Software version 1.5. Device programming can be done with the supplied cable, and embedded controller, or automatic test equipment.

Prototyping

During initial prototyping, a printed circuit board (PCB) is built to accommodate the CPLD's assigned pinouts. A blank device is soldered on the PCB, and a pattern is programmed into the device. During this time, the device may be reprogrammed many times using the same pinout. If the pinout cannot be locked by the architecture, an expensive and time-consuming re-layout of the PCB must be done. A device may be reprogrammed 10 or more times per day during the prototyping stage. If the entire prototyping stage lasts several weeks, the device may be reprogrammed hundreds of times. By providing industry-leading pin-locking capability and a guaranteed endurance of 10,000 program/erase cycles, the XC9500 fully supports the prototyping stage.

System Integration

When individual subsystems are operational, the entire system is assembled for overall testing and optimization. During system integration, the entire system is tested and debugged. All important logic states should be easily accessible, and internal logic implementations within each CPLD should be capable of being checked. When multiple CPLD designs are used within a system, the ability to track pattern revision becomes an issue. Each XC9500 device supports the IEEE 1149.1 INTEST and USERCODE instructions, which are used to access and debug user logic, and track pattern revisions, respectively. In addition, superior pin-locking and high endurance provides design iterations during system debug.

Manufacturing

Once the development is completed, the system design is transferred to the manufacturing and test teams to put into production. Test programs must developed to fully test the operation of the board and to program the CPLDs. Each XC9500 device may be programmed using the IEEE 1149.1 standard interface, which simplifies the generation of the test and programming vectors. The HIGHZ instruction allows a simple mechanism to float device outputs to allow a easier test flow for "bed of nails" board testing. In addition, the IDCODE and USERCODE

instructions provide electronic signatures for automatic inventory control and pattern revision tracking. By providing the capability to program all XC9500 devices concurrently within the system, the programming overhead during board test is minimized.

Field Upgrades

A system shipped to customers may need to be upgraded in the future. Design changes in the field can occur from fixing bugs, adapting to changing standards, or adding new capability. Systems with remote field upgrade capability have built-in circuitry to reprogram parts of the system internally, by using a microprocessor or other means to program a new pattern into the CPLD. The XC9500 devices support field upgrade capability by providing pin-locking capability and high endurance to accommodate the changes.

Pin-Locking Capability

The XC9500 architecture provides industry-leading pin-locking capability by incorporating the three neceesary elements.

1) 100 percent interconnect of all pins and function block outputs to function block inputs with the FastCONNECT™ switch matrix;
2) wide function block fan-in with 36 total inputs;
3) flexible product term allocation capability whereby additional product terms may be added to any macrocell without affecting adjacent macrocells.

The FastCONNECT switch matrix ensures that the path between any input or function block output to another function block is not blocked by existing routing constraints. (See Figure 1.) There is no need to require the software to re-assign pins in order to free up necessary routing connections.

By providing wide function block fan-in, additional signals may be routed into a function block when needed. (See Figure 2.) This increases the chance that a design change requiring additional signals can be made to each function block.

Finally, the XC9500 architecture allows logic to be optimally allocated as needed to each macrocell within the block. In current architectures that lack this capability, macrocells next to full macrocells may not be able to accommodate new logic changes. This in turn causes their output pins to become reassigned unexpectedly. By eliminating adjacency restrictions, the XC9500 helps to maintain a stable pinout assignment. The macrocell is shown in Figure 3.

FastFLASH™ Technology

FastFLASH technology is the first five volt flash technology for CPLDs. The proprietary 0.6 micron double-poly, double-metal flash process was jointly developed by Xilinx and technology partner Seiko-Epson (Fujimi, Japan) specifically for high-performance in-system programmable CPLDs. By providing process capabilities beyond that of the competing EEPROM technologies, FastFLASH technology enables new CPLD capabilities previously not available.

For instance, FastFLASH technology offers significant advantages over EEPROM technology used in the current generation of in-system programmable CPLDs. By providing a guaranteed endurance of 10,000 program/erase cycles, FastFLASH technology provides up to 100 times the endurance of EEPROM-based CPLDs. The enhanced endurance arises from three key differences over EEPROM technology. First, the tunnel oxide is 100 Angstroms thick (vs. 80 Angstroms for EEPROM). This allows better process control of oxide quality—a key factor in endurance. Second, the program and erase operation requires only 10 MV/cm, compared with 15-20 MV/cm for EEPROM. The lower electric field makes FastFLASH immune from tunnel oxide breakdown, which is the major cause of endurance failure in EEPROM cells. Finally, the programming time of 100 microseconds is substantially less than the five to ten milliseconds required for EEPROM. This lessens the exposure of high electric fields to the FastFLASH cell.

In addition, the FastFLASH cell size is three times smaller than the comparable EEPROM cell, which allows significantly more routing switches in less die area. CPLD EEPROM cells require separate programming device structures in addition to the control transistor. In contrast, the

FastFLASH technology allows a single merged flash transistor that performs the functions of the separate programming structures, resulting in a small cell area. This contributes to the superior routing characteristics of FastCONNECT over other switch matrix architectures. The FastFLASH cell is shown in Figure 4.

FastFLASH technology is compatible with the industry-leading flash memory processes and is optimized for high-performance logic circuitry. The FastFLASH programming cell was specially developed to provide high switching performance as well as built-in "erase Vt control" to simplify on-chip programming and erase. By including a select transistor to limit the cell Vt, the over-erase problem is eliminated. (See Figure 5.) The result is a high yielding, high performance CPLD technology with enhanced endurance compared with existing EEPROM technologies.

The XC9500 Family

The XC9500 architecture was developed to accommodate the needs of leading-edge applications in telecom, industrial control, and data processing applications. Pin-to-pin propagation delays as fast as five ns.

The XC9500 family consists of nine members ranging in density from 800 to over 12,000 usable gates. (See the table below.) All devices within the family are pin-compatible. This allows user flexibility in selecting the optimal density in each package type.

Device	Macrocells	Usable Gates	Tpd	Registers	Availability
XC9536	36	800	5	36	1Q96
XC9572	72	1,600	7.5	72	2Q96
XC95108	108	2,400	7.5	108	Now
XC95144	144	3,200	7.5	144	3Q96
XC95180	180	4,000	10	180	3Q96
XC95216	216	4,800	10	216	1Q96

XC95288	288	6,400	10	288	2Q96
XC95432	432	9,600	12	432	4Q96
XC95576	576	12,800	15	576	4Q96

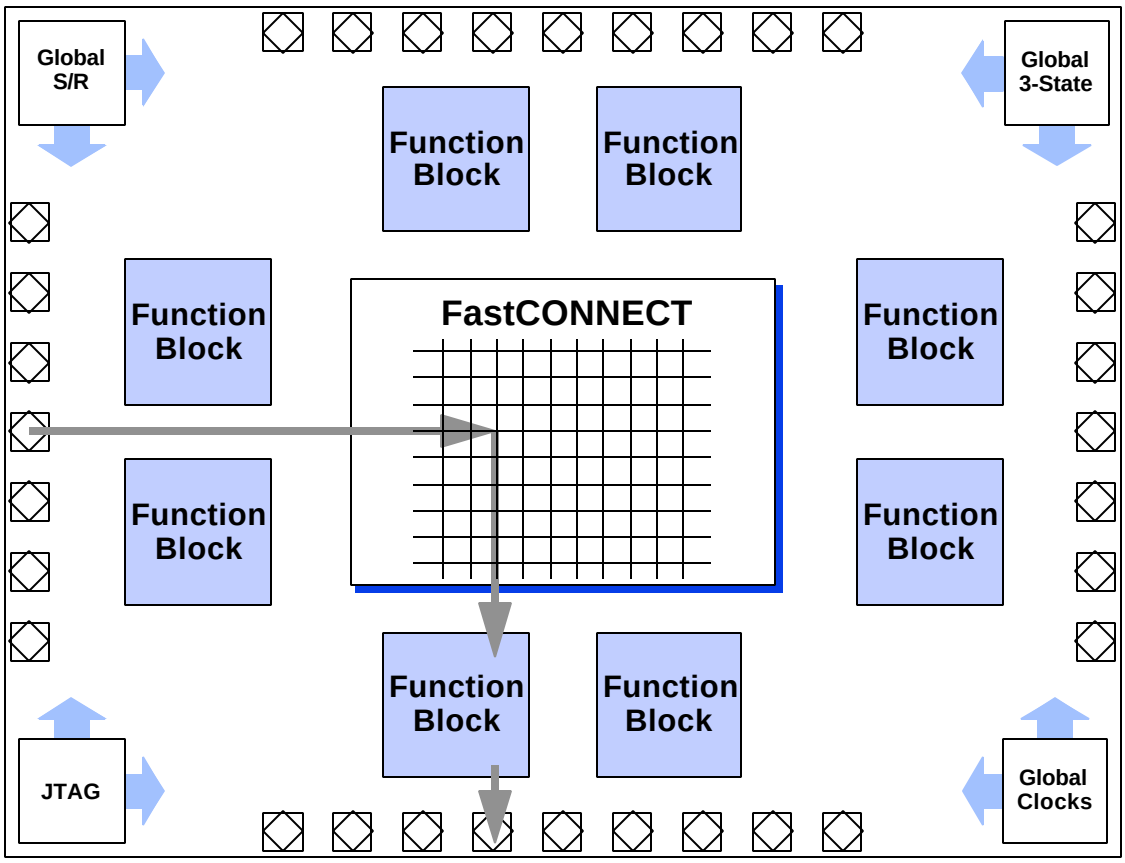


Figure 1. FastCONNECT switch matrix.

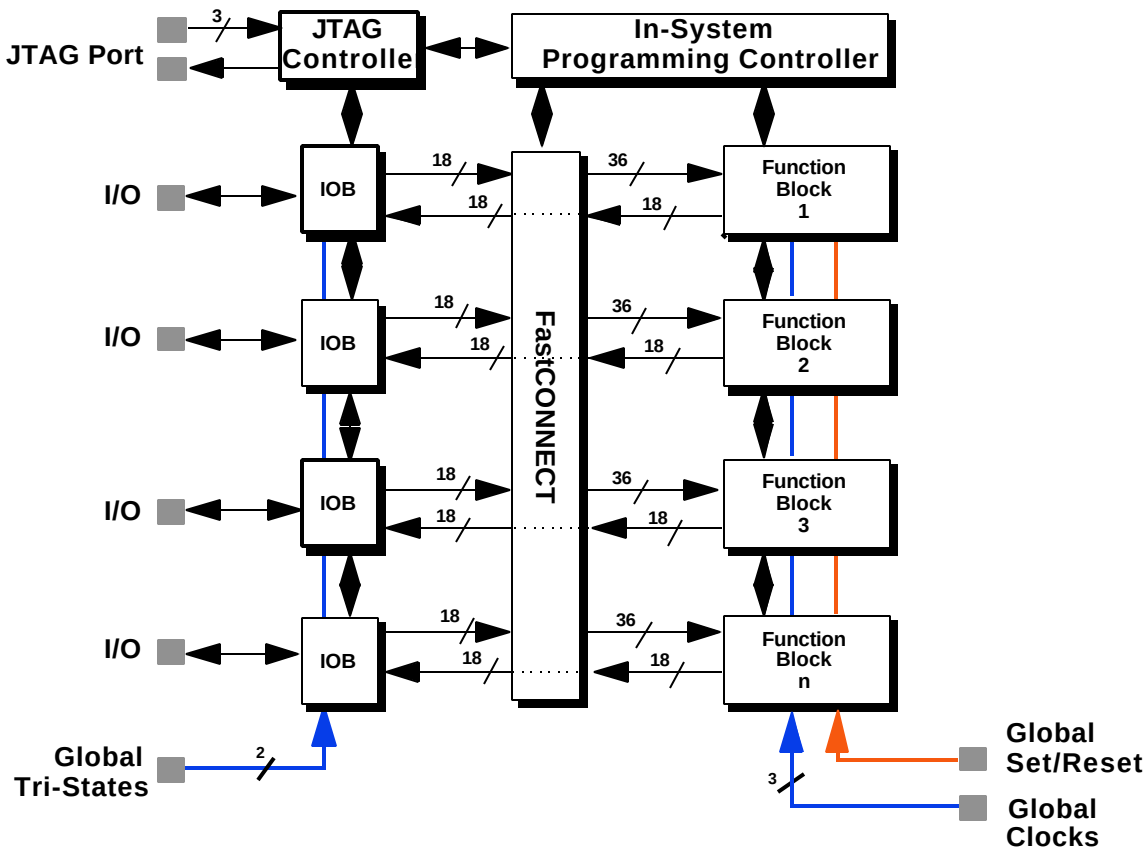


Figure 2. XC9500 block diagram.

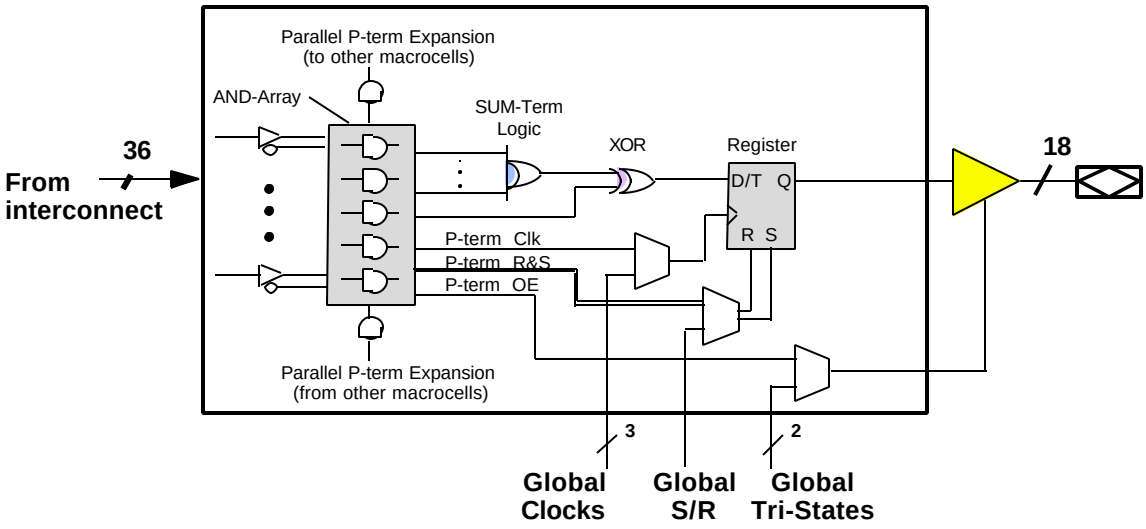


Figure 3. XC9500 macrocell.

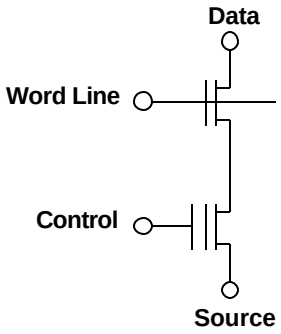


Figure 4. FastFLASH cell.

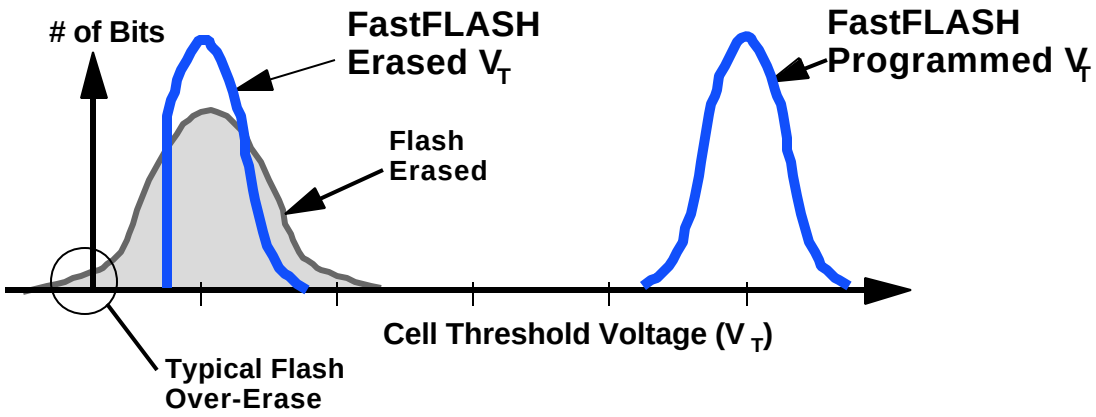


Figure 5. Threshold voltage distribution.

or revising parts that already have been programmed. Moreover, in the area of product life-cycle management, the in-system programming capability of the XC9500 family allows manufacturers to design equipment that can be maintained or diagnosed remotely in the field, eliminating the need to physically change out parts.

Pricing, **Availability, and Software Support**

Pricing for the XC95288 device begins at $65.50 in 100-unit quantities of the HQ208 package. High-volume quantity pricing is projected to be $1.50 by the end of 1998 for the XC9536 PC44 package. A variety of software is available to support the new XC9500 devices through Xilinx's easy-to-use Foundation tools and third-party packages from members of the Xilinx Alliance Partner Program. Prices for the software packages begin at $495 for complete XC9500 support.

Device	**XC9536**	**XC9572**	**XC95108**	**XC95144**	**XC95216**	**NEW XC95288**
Macrocells	36	72	108	144	216	288
T_{PD} (ns)	5	7.5	7.5	7.5	10	15
Maximum User I/O	34	72	108	133	166	192
Availability	*NOW*	*NOW*	*NOW*	1Q98	*NOW*	*NOW*
Packages	44VQ 44PC	44PC 84PC 100TQ 100PQ	84PC 100TQ 100PQ 160PQ	100PQ 160PQ	160PQ 208HQ 352BG	208HQ 352BG

Founded in 1984, Xilinx is the world's largest supplier of programmable logic solutions comprising industry leading device architectures and world class design software. Headquartered in San Jose, Calif., the company pioneered the market for field programmable gate array (FPGA) semiconductor devices that provide high integration and quick time-to-market for electronic equipment manufacturers in the computer, peripherals, telecommunications, networking, industrial control, instrumentation, consumer electronics and high reliability/military markets. For more information on Xilinx, access the World Wide Web site at http://www.xilinx.com.

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and low cost benefits of Xilinx ISP CPLDs. Despite its size, Xilinx CSP still maintains excellent thermal transfer characteristics for better heat dissipation in portable products.

The XC9536 CSP device will be available in –7 and –10 speed grades. The XC9536-10CS48 device is priced at $3.35 in 100-piece quantities. Samples are available now with production volumes by June.

A variety of software is available to support all XC9500 devices, including the Xilinx Foundation Series software, available for only $95, and the Xilinx Alliance Series software with third-party interfaces from leading EDA partners.

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented the field programmable gate array (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to reduce significantly the time required to develop products for the computer, peripheral, telecommunications, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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Scottsdale, Ariz., a product design company providing related services. “The devices operate exactly as indicated in the specifications and we’ve been spoiled by the easy in-system programming!”

The new member completes the XC9500 CPLD family with densities ranging from 36 to 288 macrocells in a variety of packages. The XC9500 family features an architecture optimized for pin-locking, a necessity for designers who want to take advantage of in-system programming (ISP) for easier prototyping, simpler manufacturing, and remote equipment upgrades.

Industry’s Best Value

Following suit on last year’s price reductions, the XC95144 device is available at $12.50 in 100-piece quantities in the 100-pin plastic-quad flat pack (PQFP) package, with high-volume quantities in mid-1999 priced at $6.95. This represents the best cost-per-macrocell in the industry for a CPLD offering industry-leading ISP capabilities. The Xilinx Foundation Series software and third-party interfaces from the Xilinx Alliance Partner program fully support the entire XC9500 family.

COMPLETE XC9500 SERIES

				new		
Device	**XC9536**	**XC9572**	**XC95108**	**XC95144**	**XC95216**	**XC95288**
Macrocells	36	72	108	144	216	288
T_{PD} (ns)	5	7.5	7.5	7.5	10	15
Maximum User I/O	34	72	108	133	166	192
Packages	44VQFP	44PLCC	84PLCC	100TQFP	160PQFP	208HQFP
	44PLCC	84PLCC	100TQFP	100PQFP	208HQFP	352BGA
	48CSP	100TQFP	100TQFP	160PQFP	352BGA	
		100PQFP	160PQFP			

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented the field programmable gate array (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to reduce significantly the time required to develop products for the computer, peripheral, telecommunications, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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