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FOR IMMEDIATE RELEASE

XILINX SHIPS THE REAL 64/66 PCI,

INDUSTRY'S FIRST GENERAL-PURPOSE 64-BIT, 66 MHZ PCI SOLUTION

Virtex FPGA family meets demand for fastest available PCI compliance, flexibility and performance - before standard chips, ASICs and specialized FPGAs

SAN JOSE, Calif. – March 22, 1999 – In a move that brings programmable logic to the forefront of high-performance system level integration, Xilinx, Inc. (NASDAQ:XLNX) today announced the immediate availability of The Real 64/66 PCI™ solution. The Real 64/66 PCI core is the first complete solution that enables customers to design fully compliant yet flexible single-chip 64-bit, 66 MHz PCI bus interface systems. In addition to the new software core, Xilinx also announced a faster Virtex FPGA, the –6 speed grade, for 64-bit, 66 MHz PCI designs. The Real 64/66 PCI from Xilinx:

- Is available as a commercial product today
- Offers full compliance with the v2.2 PCI bus interface specification
- Provides 64-bit, 66 MHz performance throughout the complete design
- Gives customers the flexibility to build a single-chip design using standard FPGAs

"Xilinx PCI solutions provided us a great deal of latitude to customize our advanced networking and communications products," said Jennifer Hergert, engineering manager at Cisco Systems, San Jose, Calif. "The predefined and fully compliant Xilinx PCI core has both provided flexible solutions for our designs and aided Cisco in getting our routers to market."

"With the Real-PCI 64/66 products from Xilinx, we were able to implement a fully compliant PCI interface in our new Mx2/PCI product family plus other functions such as direct memory access (DMA), four dual-port FIFOs, and 200,000 gates of our own unique design in a single device," said John Beck, principal engineer at DOME imaging systems, Inc., Waltham, Mass.

-more-

The logo features the text "The Real-PCI™" in a bold, black, sans-serif font. Below "Real-PCI" is a yellow and red swoosh graphic. Underneath the swoosh, the text "64/66" is written in a red, italicized font. The entire logo is centered between two horizontal blue lines.

The **Real-PCI**™
64/66

Xilinx is Shipping The Real 64/66 PCI™

Industry's First General-Purpose
64-bit, 66MHz PCI Solution

Publication Embargo Date: March 22, 1999

Questions and Answers:

The Real 64/66 PCI from Xilinx

What does Xilinx mean by The Real 64/66 PCI?

PCI 64-bit, 66MHz is an extremely difficult interface to implement, not only in FPGA technology, but also in ASIC technology. Several companies – FPGA vendors and standard-chip vendors – have announced that they will have products in the future, or that they can meet the stringent 66MHz PCI timing, but all have yet to prove that they have a real solution. Xilinx is the first company to actually ship a complete, general-purpose solution for 64-bit, 66MHz PCI.

The Xilinx solution is "real" because it provides:

- **Real compliance** by providing a fully PCI v2.2 compliant core with guaranteed 66MHz PCI timing. No other company provides a soft core with guaranteed timing.
- **Real flexibility** by providing a standard, off-the-shelf FPGA that meets all timing requirements of a fully compliant, 64-bit, 66MHz PCI interface.
- **Real performance** by providing a PCI core that supports zero wait-state burst and scalable on-chip dual-port FIFOs. As a result, the designer can achieve up to the theoretical maximum throughput of 528 MBytes/second.
- **Real availability because** only Xilinx ships the 64-bit, 66MHz PCI solution today. Moreover, Xilinx has had an early access program with more than a dozen customers since September last year, all designing for 66MHz PCI.

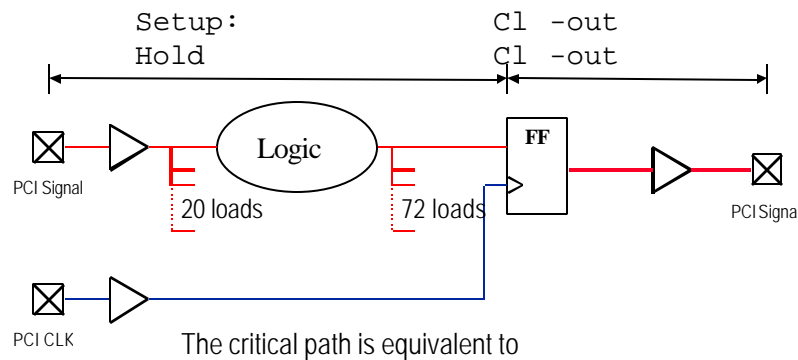
Why is 66 MHz PCI so difficult to do?

There are several reasons why PCI is such a challenge:

- PCI is an extremely complex protocol for which almost an infinite number of transaction combinations can occur. The PCI Special Interest Group (PCI-SIG) provides a checklist which all PCI vendors must comply with. However, this checklist only covers a small subset of all the possible combinations of transactions that can occur, hence, it is not good enough to only adhere to the checklist. As a result, many of the standard PCI interface chips are released with a long errata list of known issues and limitations. Xilinx has an internal testbench that runs more than six million test vectors to verify its PCI core designs.
- Meeting the stringent 66MHz PCI timing is a challenge in any technology. The 66MHz PCI v2.2 specification calls for a 3 ns (nanosecond) max setup-time, 0 ns hold-time, 6 ns max clock-to-out, and 2 ns min clock-to-out. For example, to achieve zero wait-state burst with a fully compliant behavior, a number of PCI control signals must be decoded live during the 3 ns setup-time. In a 64-bit 66MHz interface, those signals must go through an input buffer and fan out to more than 20 loads, go through one level of logic to 74 registers, in 3 ns or less. The following illustrations provides details.

Attaining 200MHz Plus:

The Critical Path for Zero Wait-state PCI64/66



Xilinx supports this path in its Virtex FPGA family, and it is implemented and guaranteed in Xilinx Real 64/66 PCI core design. Furthermore, Xilinx guarantees the 0 ns hold-time and both the 6 ns max clock-to-out and 2 ns min clock-to-out.

How can Xilinx guarantee the timing in its soft Real 64/66 PCI design?

Xilinx spends significant effort to fully verify its PCI interface cores through extensive simulation, and through characterization of both the core and the FPGA device. The verification includes both functional behavior and timing. When all timing parameters are met, placement constraints and routing constraints are applied to the core. The constraints ensure that the PCI core behaves correctly and meets timing every time a user implements it with a unique back-end design. The user's back-end design doesn't affect the PCI timing as long as the user follows the design rules described in the product documentation. To maintain the correct implementation constraints, the PCI core is parameterized through an easy-to-use graphical user interface available on the Xilinx web site. This technology is known as Smart-IP Technology and is only available from Xilinx. Because other FPGA vendors do not provide Smart-IP technology, their users must account for tuning the implementation and verifying the timing in order to claim full PCI compliance.

How does an FPGA with a PCI core compare to a standard PCI-bridge chip?

First, there are no general-purpose standard 64-bit, 66MHz PCI-bridge chips available yet. Second, a standard PCI-bridge chip is designed for a specific application, with a specific feature set, bridging from PCI to a given local bus. In an FPGA, a user can integrate a fully compliant PCI interface with customized FIFOs, DMA, and other functions in up to one

million gates of user logic. The result is higher integration, higher performance, and lower system cost.

How does a standard FPGA with a soft PCI core compare to a specialized FPGA with a PCI interface embedded in silicon?

FPGAs have become a very popular device for integrating glue logic – and lately entire logic systems – because it is a broad-based standard component. FPGAs come in a variety of sizes and packages, they are flexible to use, offer fast time-to-market, require short lead-times and simplify inventory logistics. Creating a specialized FPGA with a PCI interface violates the fundamental benefits of an FPGA – flexibility to change – that made the device so popular in the first place. Furthermore, since PCI is such a difficult application to get right the first time, suppliers of specialized PCI FPGAs will face the same quality issues and limitations as standard PCI chip vendors have for several years.

The benefits of using standard, rather than specialized FPGAs, for PCI applications are numerous:

- With a standard FPGA solution, users can choose from a range of device sizes and packages. For example, Xilinx offers 5,000 – one million system gates for user applications for the company's various PCI 32-bit and 64-bit solutions. Only one specialized PCI FPGA has announced to date.
- With a standard FPGA solution users can implement PCI features, DMA configurations and FIFO sizes that are required for their specific applications, and users do not have to pay for unused features. As with standard PCI-bridge chips, a specialized FPGA comes with a fixed set of features.
- With a standard FPGA and soft PCI core solution, users can adapt to future PCI revisions and add requirements that may be revealed when new PCI chip sets or PCs are introduced.

Isn't a specialized FPGA with embedded PCI a lower cost solution?

A PCI interface embedded in silicon may occupy less silicon area. However, this saving is offset by increased manufacturing costs resulting from lower manufacturing volume and more complex testing. Moreover, a standard FPGA with its regular architecture will be migrated more aggressively to new process technologies, which over time will result in both lower cost and higher performance.

So Xilinx PCI products are delivered over the Internet. How does that work?

A customer purchases the The Real 64/66 PCI products as regular software product. Xilinx will ship the "physical" product, not including any design files, with a unique serial number. The user then registers on Xilinx web site to get access to the PCI configuration tool, all the design files, reference designs, and online documentation. The unique serial number will be used to authenticate a new user. All customers will have instant access to new The Real 64/66 PCI releases, new reference designs and other updates.

What tools do I need to design with Xilinx PCI products?

The customer receives all design files required for a VHDL and Verilog design flow, including wrappers for instantiation, simulation models and a basic test bench. Xilinx tests and documents the Synopsys FPGA Compiler and FPGA Express tools for design entry, and Model Technology and Verilog XL for simulation.

Additionally, Xilinx has announced support for the Synplify tools from Synplicity, which has tested and documented the flow.

How many PCI designs has Xilinx supported to date?

Xilinx customers have completed more than 1,000 designs with the PCI32 cores, of which many have been tested at the PCI-SIG's Plug-fest for full compliance. Xilinx currently has more than a dozen customers using the new The Real 64/66 PCI products.

How can I order the The Real 64/66 PCI solution from Xilinx, and what is the price?

- Order part number DO-DI-PCI64
- Price \$14,995
- Available now from Xilinx local sales representatives. See the Xilinx web site for details (www.xilinx.com)

Xilinx PCI Customer Classes

What prerequisites are necessary to attend a Xilinx PCI course?

Attendees should have Xilinx design experience and some knowledge of PCI. The students need to have the following:

- Working experience with digital design
- Basic knowledge of Verilog or VHDL
- Some experience of Xilinx Foundation and FPGA Express including writing UCF files
- Some knowledge of PCI (Xilinx will provide PCI basics online before hand)

What topics will be covered?

The focus will be on design usage of Xilinx PCI products with hands-on participation during the lab session. In addition, the following topics will be covered:

- Basic PCI concepts
- Xilinx PCI solution
- Designing with Xilinx PCI - Configuration, Integration, and Verification
- Design debug

What will students have learned on completion of the course?

The goal of Xilinx Customer Education is to help customers successfully complete a PCI design. After completing this course, customers will be able to:

- Describe the basics of the PCI specification
- Select the appropriate PCI solution for a specific application
- Register for Xilinx PCI lounges on Xilinx web site, where all design files are configured and downloaded.
- Configure and download a The Real 64/66 PCI design
- Integrate the The Real 64/66 PCI design with a back-end design
- Verify and debug a PCI design with Xilinx tools

How can I order the PCI training course, and what is the price?

- Order part number TC-PCI-2DY
- The 2 day course is \$1,000
- For more information, see the web site <http://support.xilinx.com> – under Education, click Courses

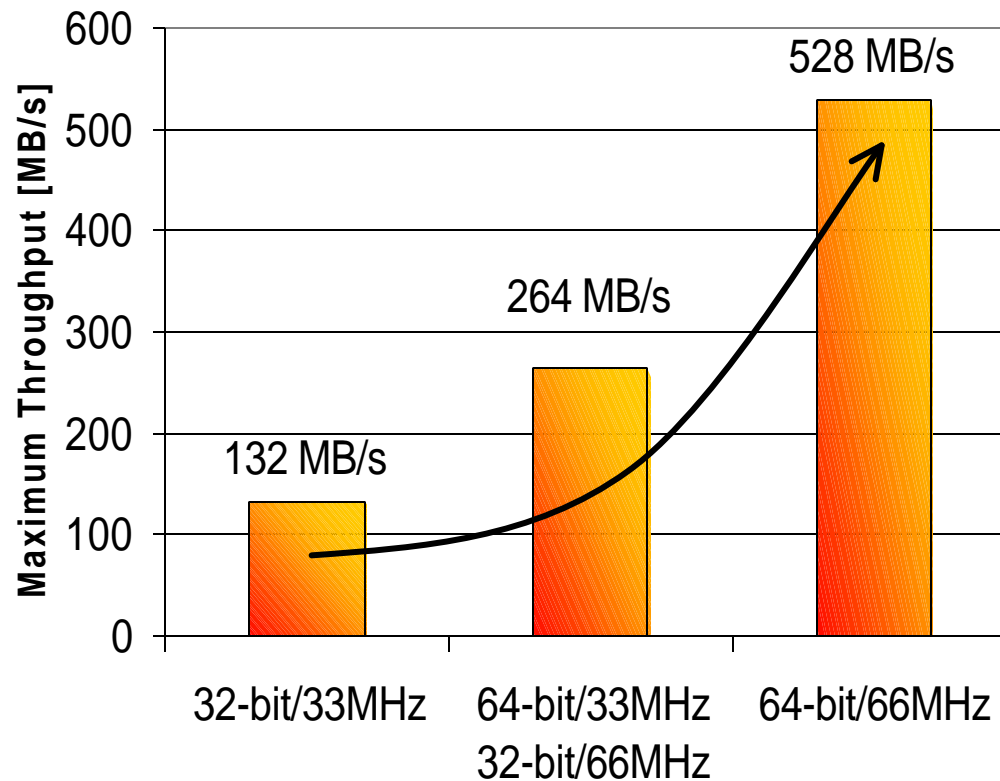
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A Complete Solution for 64-bit 66MHz PCI

- ◆ New *64/66 PCI core* implemented in Xilinx standard Virtex FPGA family
- ◆ New *PCI customer classes* from Xilinx
- ◆ *Synplicity adds support* for The Real 64/66 PCI™ from Xilinx (in addition to Synopsys)
- ◆ Third party *design services*

Emerging Applications Require Higher PCI Bandwidth

PCI Performance



- ◆ Gigabit Ethernet
- ◆ ATM, Fibre Channel
- ◆ DSP/Imaging
- ◆ Mass-Storage/RAID
- ◆ High-end Printer I/Fs

Requirements on a Commercial 64-bit 66MHz PCI Product

1. *Full compliance*

- PCI design must be proven
- Timing & electrical spec must be guaranteed

2. *Full flexibility*

- Ability to customize and integrate PCI & user logic
- Ability to adopt future changes and requirements

3. *Full performance*

- Up to maximum 528 Mbytes per second sustained throughput

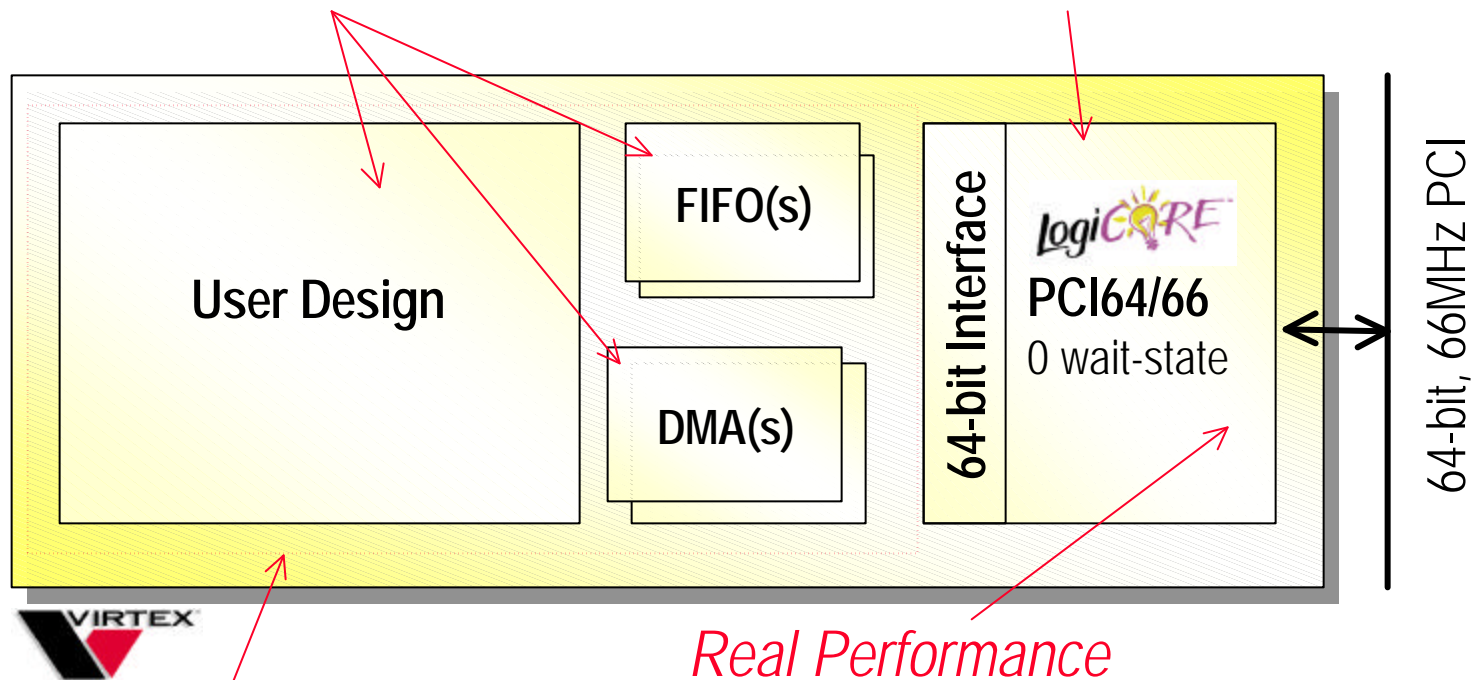
The Real 64/66 PCI from Xilinx

Real Flexibility

- Uses standard Virtex FPGA
- Back-end de-coupled from core

Real Compliance

- PCI v2.2 Initiator and Target
- Guaranteed timing



260,000 gates in V300
1 million gates in V1000

Real Performance

- Compliant 0 wait-state at 66MHz
- Full 64-bit data path

The **Real-PCI™**
64/66



Downloadable Today



PRODUCTS

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THE HOME PAGE FOR PROGRAMMABLE LOGIC

XILINX®

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- ◆ All design files are released on WebLINX
- ◆ Instant access of new releases and updates
- ◆ Intuitive GUI generates guaranteed design files
- ◆ Verified for
 - Synopsys
 - Synplicity **NEW!**
 - MTI

Virtex Configuration Space Header XPCI Virtex64

31	16	15	0	
Device ID: 0300h		Vendor ID: 10EEh		00h
Status		Command		04h
Class Code: 0B4000h		Rev ID: 00h		08h
BIST	Header Type	Latency Timer	Cache Ln Size	0Ch <input checked="" type="checkbox"/> Latency Tmr Enable
Base Address Register 0: 01000000h 10h <input checked="" type="checkbox"/> BAR 0 Enable				
Base Address Register 1: 01000000h 14h <input checked="" type="checkbox"/> BAR 1 Enable				
Base Address Register 2: 01000000h 18h <input checked="" type="checkbox"/> BAR 2 Enable				
Base Address Register 3 1Ch				
Base Address Register 4 20h				
Base Address Register 5 24h				
Cardbus CIS Pointer 28h				
Subsystem ID: 0000h		Subsystem Vndr ID: 0000h		2Ch <input type="checkbox"/> External Subsystem
Expansion ROM Base Address 30h				
Reserved			CLst Ptr: 80h	34h <input checked="" type="checkbox"/> Cap List Enable
Reserved 38h				
Max_Lat: 80h	Min_Gnt: 80h	Irpt Pin: 01h	Irpt Line: FFh	3Ch <input checked="" type="checkbox"/> INTA Enable
Reserved 40h-7Ch <input checked="" type="checkbox"/> User Config Space				

Defaults Hide Download Help

Programming
 Log

Real Availability

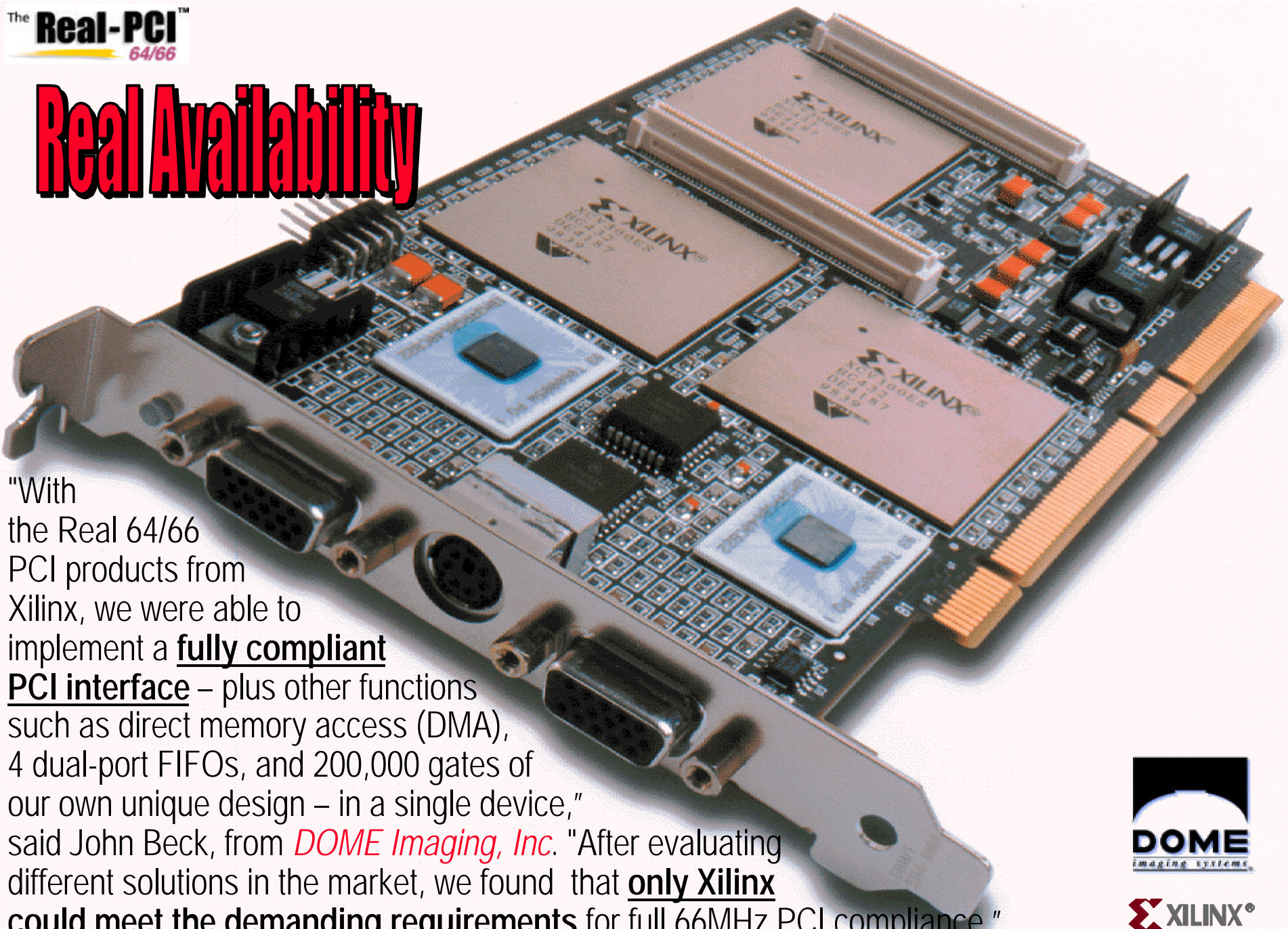
Xilinx 64/66 PCI Beta Program Since September

- ◆ Fifteen customers have actively been designing 64-bit 66MHz PCI systems with the products from Xilinx
 - Customer examples: Ascend, Dome Imaging, and Kodak
- ◆ Allowed us to *secure critical design wins* and get *customer feedback* early in the development

Real Availability

The **Real-PCI™**
64/66

Real Availability



"With the Real 64/66 PCI products from Xilinx, we were able to implement a **fully compliant PCI interface** – plus other functions such as direct memory access (DMA), 4 dual-port FIFOs, and 200,000 gates of our own unique design – in a single device," said John Beck, from *DOME Imaging, Inc.* "After evaluating different solutions in the market, we found that **only Xilinx could meet the demanding requirements** for full 66MHz PCI compliance."



Full 528 MB/s Sustained Throughput

- ◆ Compliant *zero wait-state* burst at 66MHz
- ◆ Full *64-bit data path* on PCI side and back-end interface
- ◆ *On-chip dual-port FIFOs* can be added to support maximum performance

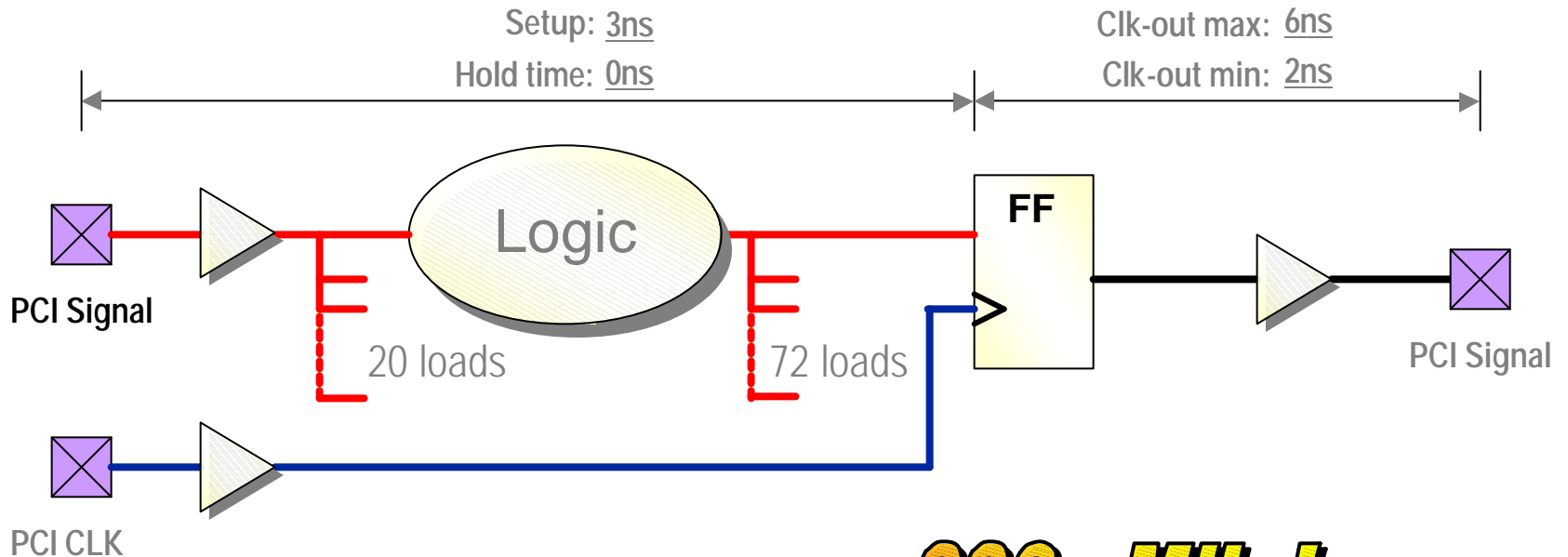
Real Performance

New PCI64/66 Core Based on Proven PCI32 Design

- ◆ PCI32 has been used in *over 1,000 customer designs*, of which many are fully compliant add-in boards
- ◆ PCI protocol verified with internal testbench simulating over *6 million PCI cycles*
- ◆ Automatically sets up correct *64-bit or 32-bit transactions* depending on the target

Real Compliance

The Real 64/66 PCI Guarantees *The Critical Path*



◆ The critical path is equivalent to **220+ MHz!**

◆ Uses Xilinx unique Smart-IP technology to guarantee *min, max & hold* time

— Core and silicon characterized together

Real Compliance

Real Flexibility

Implemented in Xilinx Standard Virtex FPGAs

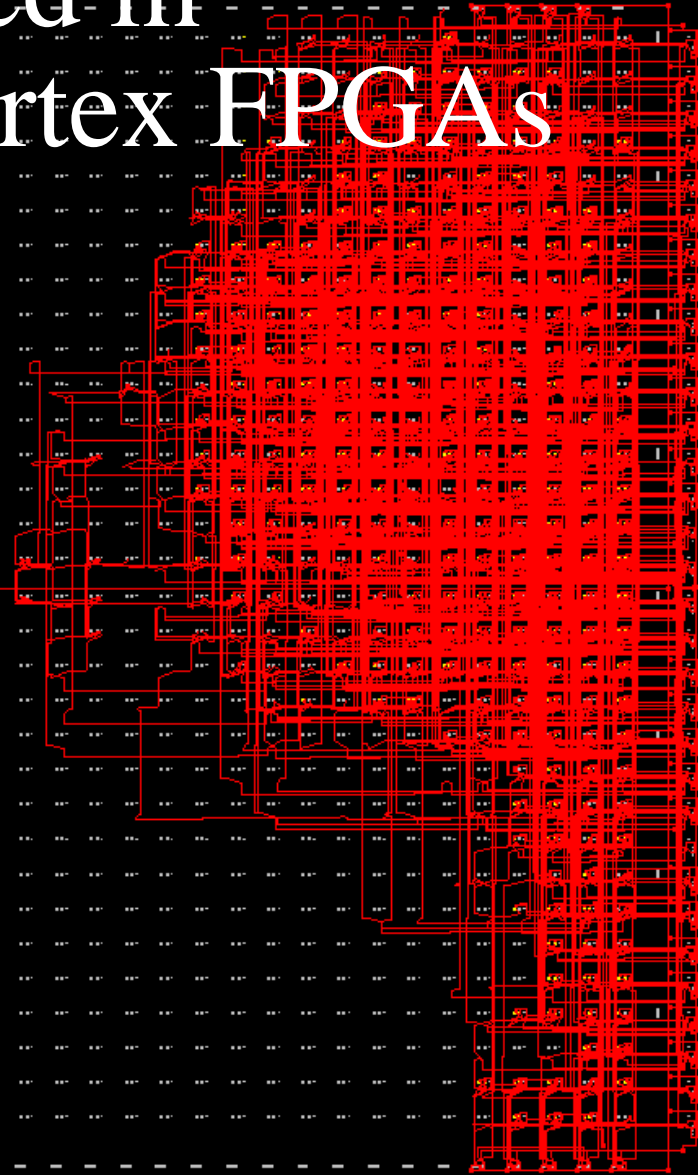
- ◆ Up to 300,000 system gates on one XCV300 FPGA

- PCI
- Dual-port FIFOs
- DMA
- Customer design

- ◆ Usage

- 12% of an XCV300 BG432
- 3% of an XCV1000 FG680

- ◆ Design can be adopted to future changes and requirements



Picture shows the EPIC view of PCI64/66 implemented in XCV300



Real Flexibility

Implemented in Xilinx Standard Virtex FPGAs

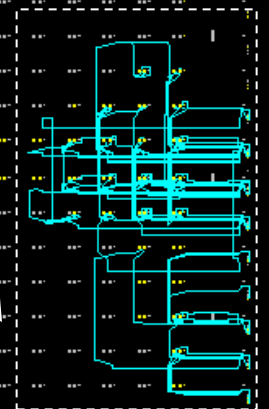
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- ◆ Design can be adopted to future changes and requirements



Section with
guaranteed timing

Picture shows the EPIC view of the pre-implemented section in XCV300

New PCI Training Classes

- ◆ Two day PCI course
 - Basic PCI concepts
 - Xilinx PCI solution
 - Designing with Xilinx PCI
 - Design debug
- ◆ Starting in May 1999 in US



SUPPORT & TRAINING

support.xilinx.com

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XILINX®

PCI Expertise

- ◆ Provide worldwide access to certified PCI experts that can provide:
 - Support for targeting additional devices
 - Implementation of additional features
 - Complete turnkey integration



MULTI VIDEO DESIGN



Xilinx Has a Rich PCI Heritage

- 01/96: LogiCORE PCI v1.0 - First PCI core for FPGAs
- 04/97: PCI v1.2 & First web-based core configuration tool
- 12/97: PCI V2.0 - First fully-compliant 0 wait-state core
- 05/98: Xilinx PCI - First complete design kit for FPGA-based PCI
- 01/99: PCI32 Spartan XL - Industry's lowest cost PCI solution
- 03/99: *The Real 64/66 PCI - Industry's First General-Purpose 64-bit, 66MHz PCI Solution*

Real Availability



The Real 64/66 PCI Summary

- ◆ *Real Compliance* - guaranteed timing
- ◆ *Real Flexibility* - implemented in standard Virtex FPGAs
- ◆ *Real Performance* - full 528 Mbytes per second
- ◆ *Real Availability* - downloadable from Xilinx web-site now

Reference Slides

The Real 64/66 PCI™ Products

- ◆ LogiCORE™ PCI64/66
 - Includes all design files and documentation required to do a 64-bit 66MHz PCI core
 - Supports XCV300 now
 - Part no: DO-DI-PCI64
 - Price: \$14,995
 - *Available now*

U.S. Partners



Memec Design Services
1819 S. Dobson Rd, Ste. 203
Mesa, Arizona 85202, USA



Comit Systems
1250 Oakmead Pkwy, Suite 210
Sunnyvale, CA 94088, USA

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Shenzhen, P.R.China

The Dome Mx2/PCI is the first in a new family of high resolution display controllers for the medical imaging market that can handle transfers of over 500 MBytes/second from the host. "After evaluating different solutions in the market, we found that only Xilinx could meet the demanding requirements for full 66 MHz PCI compliance."

"The Real 64/66 PCI represents the first time that an FPGA supplier has delivered a general purpose solution before manufacturers of standard chip-sets," said Wim Roelandts, Xilinx president and CEO. "This is a significant milestone that underscores the inherent benefits of standard FPGAs produced with the most advanced silicon processes. More important, The Real 64/66 PCI solution allows designers to integrate very high-performance, high-density 66 MHz PCI systems tailored to their specific needs."

Real availability

More than a dozen Xilinx customers have been actively engaged in a beta program since September using The Real 64/66 PCI core to design high-performance applications such as Gigabit Ethernet, ATM and Fiber Channel adapters, DSP and imaging boards, disk drive arrays and high-end printer interfaces. Beta customers include Ascend Communications, Westford, Mass.; Cisco Systems, San Jose, Calif.; Dome imaging systems; and Kodak, Rochester, N.Y.

Real compliance

The Real 64/66 PCI solution provides true timing, functional and electrical PCI v2.2 compliance by using Xilinx Smart-IP technology to guarantee critical minimum, maximum and hold timing required for a true zero wait-state burst operation at 66 MHz. Compliance is verified through hardware testing, device characterization and regression testing using an internal test bench that simulates more than six million unique combinations of PCI transactions.

"Xilinx released its first PCI core more than four years ago, and our PCI products to date have been used in more than 1,000 customer designs," said Rich Sevcik, senior vice president of software, cores and support at Xilinx. "This rich PCI heritage has given Xilinx experience with PCI that is unmatched in the industry. It has allowed us to develop the design and verification processes necessary to build and support high-quality PCI products. The Real PCI 64/66 core, which can be downloaded from the Xilinx Web site, reinforces our on-going Silicon Xpresso initiative to use the Internet to increase the productivity of designers."

Real performance

The Virtex FPGAs are manufactured on a state-of-the-art 0.22 micron process that meets all timing requirements for 64-bit, 66 MHz performance, up to the theoretical maximum throughput of 528 Mbytes per second.

Xilinx 64/66 PCI Core

Page 3 of 3

The Real 64/66 PCI solution is fully verified by Xilinx for the Virtex XCV300-6 BG432 and XCV1000-6 FG680 devices, which offer densities of 300,000 and one million system gates, respectively.

Real flexibility

Implemented in Xilinx standard Virtex FPGAs, The Real 64/66 PCI solution allows customers to benefit from real flexibility provided only by standard, off-the-shelf FPGAs. For example, a designer can choose Virtex device size and package type, customize the PCI feature set, and adapt the design later to future changes in the PCI standard or new PCI requirements. Both Synopsys and Synplicity support The Real 64/66 PCI core in their design flows.

"The Real 64/66 PCI solution will allow FPGA customers to implement the logic for high performance bus designs using the familiar Synopsys FPGA design flow," said Jay Michlin, vice president and general manager of the FPGA business unit at Synopsys. "Our FPGA Compiler II and FPGA Express synthesis tools aid designers incorporating this new state-of-the-art intellectual property for FPGAs into very demanding design situations."

Xilinx PCI Training

To further complete the Xilinx PCI solution, Xilinx will offer a two-day PCI course beginning in May for customers who are planning PCI systems. The course will give an introduction to the PCI standard, cover configuration and integration of The Real 64/66 PCI core, system integration, verification and debug. In addition to Xilinx classes, PCI design services are available from a number of partners in the worldwide Xilinx XPERTS design consulting program.

Pricing and Availability

The Real 64/66 PCI core for the Virtex XCV300 BG432 device and the Virtex -6 speed grade FPGAs are available now from Xilinx. The Real 64/66 PCI product is priced at \$14,995.

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented the field programmable gate array (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to reduce significantly the time required to develop products for the computer, peripheral, telecommunications, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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