Editorial contact:
Ann Duft
Xilinx, Inc.
(408) 879-4726
publicrelations@xilinx.com

Kathy Keller
Oak Ridge Public Relations
(408) 253-5042
kathy.keller@oakridge.com

Product Marketing contact:
Bruce Jorgens
Xilinx, Inc.
(408) 879-5236
bruce.jorgens@xilinx.com

FOR IMMEDIATE RELEASE

XILINX BREAKS ONE MILLION-GATE BARRIER

WITH DELIVERY OF NEW VIRTEX SERIES

Next generation architecture couples unparalleled performance and

unprecedented system integration capabilities in a broad density range family

SAN JOSE, Calif., October 26, 1998—Dramatically expanding on the traditional uses for programmable logic, Xilinx, Inc. (NASDAQ: XLNX) today announced the first delivery of the Virtex FPGA series as a new FPGA platform to truly address system-level design issues. Starting at $10, the family encompasses a robust feature set across a full density range from 50,000 to one million system gates. The million-gate Virtex FPGAs—an industry first at this density—and a 300,000 gate device are available now.

The Virtex FPGA has built-in capabilities to solve designers' challenges throughout the system: solutions for chip-to-chip communication needs amidst multiple I/O standards, numerous clock signal synchronization inside and outside the device, and management of a variety of memory needs. No other FPGA solves these system-level problems that designers face. Moreover, these features are available at new lower industry price points, offering ASIC-competitive performance advantages at densities as low as 50,000 system gates.

Xilinx has worked with several customers worldwide, including Adtech, Hawaii; Hughes Space and Communications Company, Calif.; and NDS (News Data Services) Ltd., UK. Software support for Virtex FPGAs has been available since November 1997, allowing customers to have working systems today based on Virtex FPGAs.

"The Virtex FPGAs are not merely a collection of gates; they are intelligent devices that deliver a value beyond the socket, changing the way entire systems are designed," said Wim Roelandts, Xilinx president and CEO. "Systems architects will choose Virtex FPGAs not just because of the unmatched density, performance, and features, but because they address the breadth of their systems needs better

—more—

than any other alternative, programmable or ASIC. Because of this, we expect increased programmable content in our customers' applications."

Million-gate device shipping to customers now

The Virtex development transpired over several years. Key to the development was extensive research in which Xilinx engaged customers to find out what they consider to be their most important system design challenges for the next five years. As a result, Virtex FPGAs include pre-engineered system-level solutions addressing customers' needs for push-button, high-performance design with capabilities that exceed today's FPGAs.

"These million gate FPGAs enable our test modules to provide thousands of continuous measurements at telecom speeds up to 2.4 gigabits per second," said Carl Uyehara, vice president of engineering at Adtech, Inc., a leading supplier of broadband test systems. "We especially like the fact that Virtex FPGAs are programmable. This allows us to use a single test module for multiple transmission technologies such as ATM and frame relay, which provides huge cost savings and convenience for our customers plus future enhancement capability."

New applications redefine what is possible with an FPGA

Virtex FPGAs are designed-in as main system components previously addressed by ASICs, specifically standard cell-based devices. Some examples are 66 MHz/64 Bit PCI applications; OC-3, OC-12 and OC-48 telecommunication equipment; next generation (beyond gigabit) network equipment; satellite base stations; high-performance graphics editing machines; massively parallel compute engines; HDTV broadcast systems; and medical imaging machines.

Virtex technology serves as the ideal platform to redefine FPGA implementation

The Virtex technology is the combination of leading-edge process technology, a system-level feature set, and breakthrough software technology. To build a million-gate FPGA, specific design optimization of the technology was necessary. The Virtex architecture represents aggressive use of an advanced 0.22-micron process to pack one million gates and full utilization of five metal layers for an abundance of high performance routing tracks. The architecture is also easily scalable from 50,000 to one million system gates to offer the robust feature set across a wide range of densities in nine devices.

"The critical features of Virtex FPGAs, such as the segmented routing and 0.22 micron feature size, allowed new levels of performance for our high-speed digital designs. The lower voltage and higher performance logic of the Virtex process are unmatched by any other supplier," said Ted Pascaru,

senior staff engineer at Hughes Space and Communications Company, Los Angeles, the leader in satellite communications. "The level of support—from the design development to the hotline assistance—that Xilinx offered with the new family also impressed us."

Still, an abundance of high performance, routable gates is not enough for system level design. Virtex FPGAs incorporate new system-level features including high performance clocking, I/O, and memory functions critical to million-gate designs. While a product backgrounder is available to describe each of these functions more in-depth, brief descriptions are:

- *Multiple digital locked loops (DLL)*: Large clock skew limits performance by taking away valuable nanoseconds from a clock period. Multiple DLLs in Virtex FPGAs allow internal and external clock synchronization—removing clock skew from the entire system and delivering up to a 100 percent increase in system performance, at greater than 160 MHz.
- *SelectI/O technology*: Rapid process technology advancements have proliferated different I/O standards complicating data flow between devices. Virtex SelectI/O technology supports multiple standards simultaneously including LVTTL, LVCMOS2, PCI33, PCI66, GTL/GTL+, SSTL, HSTL, AGP, and CTT. The flexibility of the SelectI/O technology will also support future standards.
- *SelectRAM+ memory hierarchy*: High bandwidth memory is critical in data intensive applications. Virtex SelectRAM+ memory hierarchy provides high bandwidth for memory blocks sizes in bytes (distributed memory), kilobytes (block memory), and megabytes (SSTL3 interface to external DRAM and SRAMs) for 200 MHz access to any amount of external memory.

"Virtex FPGAs have allowed us to implement our next generation digital TV broadcast systems in record time," said John Simmons, project manager, of NDS, a world leader in digital broadcasting solutions. "A key time saver was the availability of multiple DLLs that allowed us to synchronize a 74 MHz clock to more than 30 devices including multiple FPGAs, SDRAMs, and other components. Designing a no-skew clock system from scratch would take months. Xilinx delivered a ready-made solution to us with Virtex FPGAs."

Industry's fastest compile times available in Alliance Series 1.5 software

Software solutions focused on highest quality synthesis results and very fast compile times round out Virtex technology. VHDL and Verilog synthesis from Xilinx and leading EDA vendors support Virtex FPGAs now and deliver new performance levels for FPGAs. Xilinx has also delivered a quantum

leap in productivity by delivering timing-driven place and route tools capable of compiling 200,000 gates per hour for Virtex FPGAs.

As previously announced, the 1.5 release of Xilinx software supports the Virtex series. Virtex designers benefit from the release's key elements: the new Xilinx AKA*speed* technology, a suite of algorithms and algorithmic strategies combined with advanced new feature sets and applications optimized to address the elements of Virtex designs. AKA*speed* technology provides minimum timing delays, voltage and temperature prorating, graphical constraints editor, and enhancements to the existing technology elements such as timing driven implementation, K-paths, advanced timing analysis algorithms, robust constraints language, incremental design capabilities and the industry's most complete intellectual property strategy.

Superior programmable logic capability at no extra cost

All the benefits of Virtex technology are offered at new industry price points for FPGAs. This is enabled by the Xilinx leadership in product development that is based on the industry's most advanced processes. Projected high volume pricing will start below $10 for 50,000 system gates. * In comparison to other FPGAs, Virtex FPGAs deliver more gates, higher performance, and unique features at a lower price. Packaging options for the Virtex family will include plastic quad flat packs (PQFP), ball grid arrays (BGA), 1.0-mm fine pitch BGAs, and 0.8-mm chip scale packages (CSP).

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented field programmable gate arrays (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enables customers to significantly reduce the time required to develop products for the computer, peripheral, telecommunication, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx website at www.xilinx.com.

—30—

*Prices based on 100,000 unit quantity at the end of 1999 for slowest speed grade, least expensive package offering.