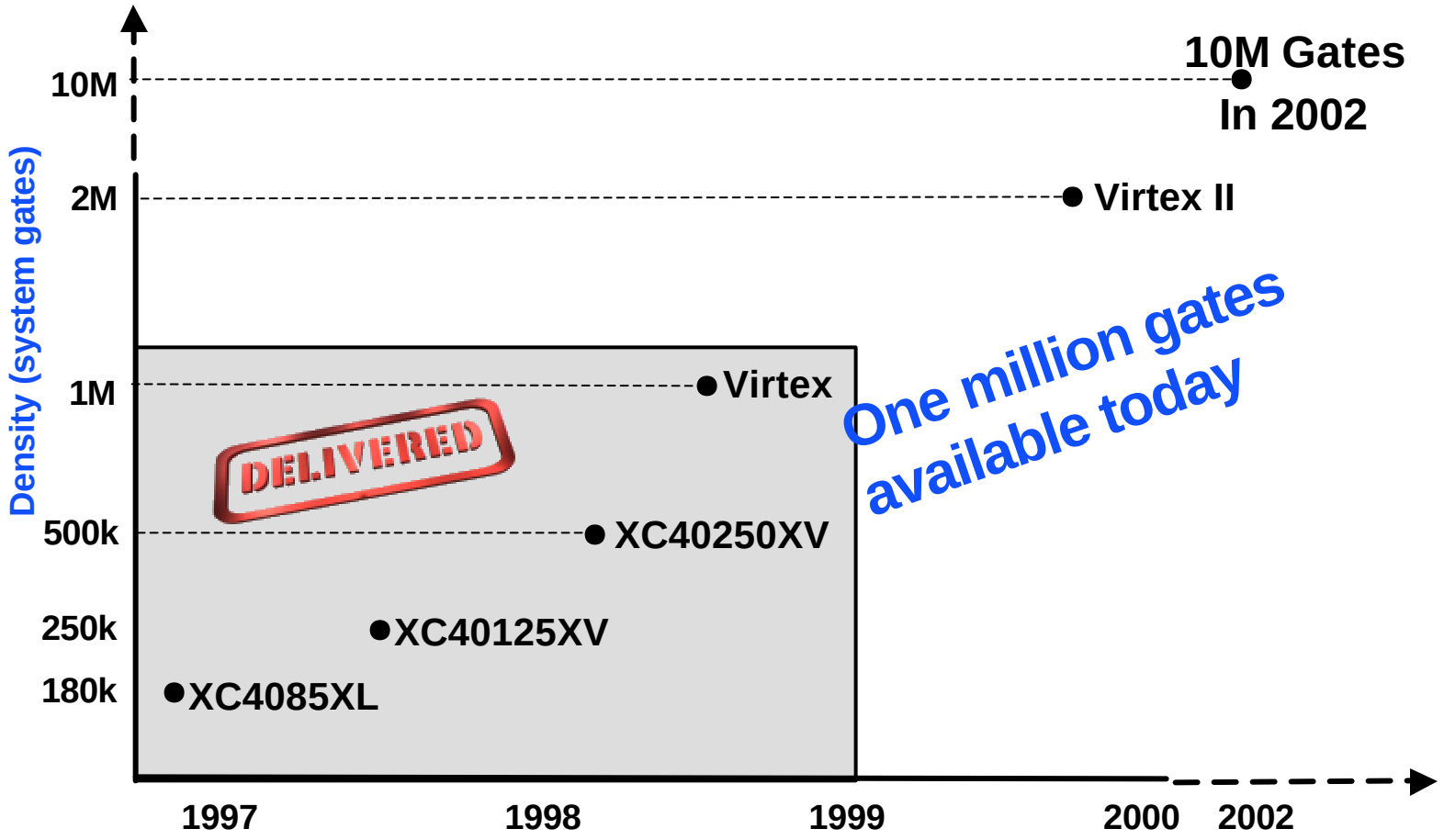
Redefining the FPGA

New FPGA platform first to offer system designers powerful board-level I/O, clock, and memory functions on a chip for under $10

XILINX®

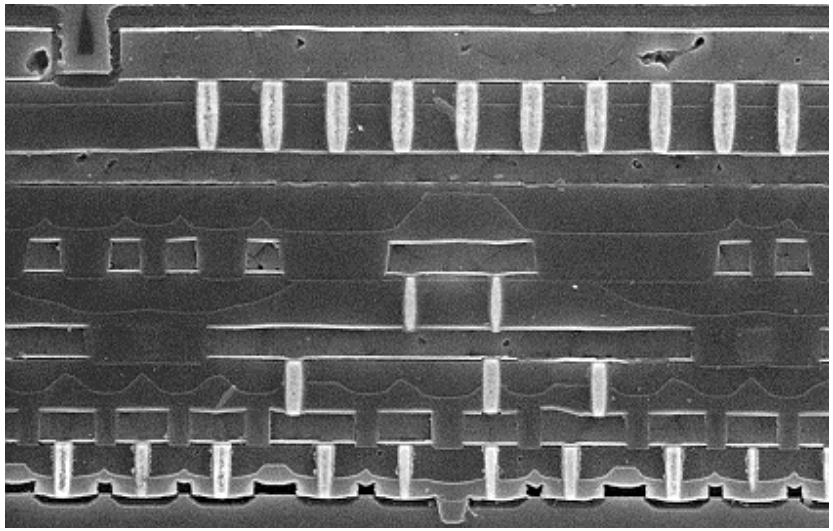
Virtex FPGAs Shipping Now



Continuing to Expand the FPGA Space

XILINX®

Process Leadership Delivers New Records



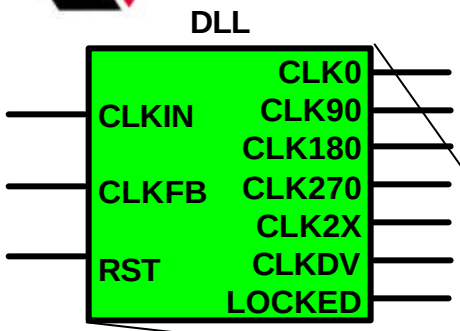
- **0.22 micron process**
  - One Million Gates
    - Four times nearest competitor
  - 27,648 Logic Cells
    - More than double nearest competitor
  - 75 million transistors
    - More than 10 times complexity of Pentium II
- **Five Metal Layers**
  - Massive Segmented Routing
    - predictably fast design

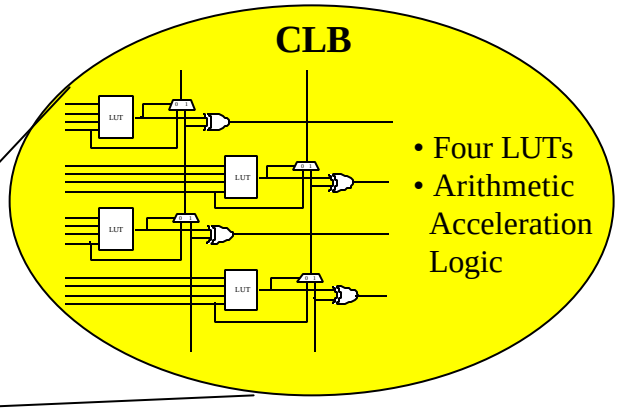
Virtex Architecture Designed to Solve System Level Design Problems

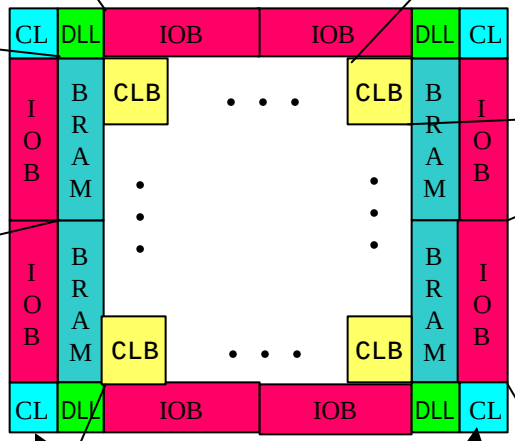
Extensive customer interviews exposed design challenges

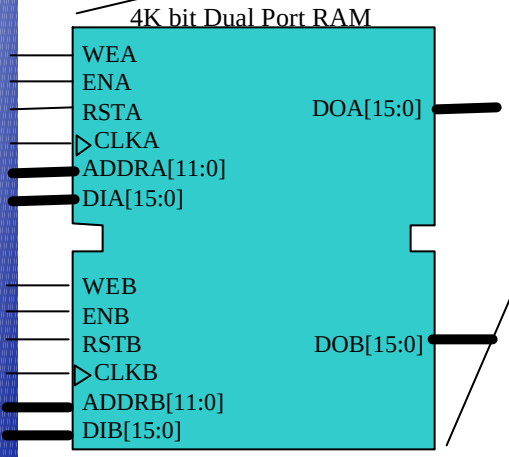
- System Timing
  - Chip to chip performance limits system speeds
  - Clock skew is the number one killer of system speed
- System Memory
  - Memory bandwidth is always key
  - Memory requirements vary in size and depth
- System Interfaces
  - Process technology leads to mixed voltage systems
  - High performance, low power signal standards emerging
- System Integration
  - Intellectual property is critical for high density design
  - Intellectual property must drop in easily

Virtex Technology







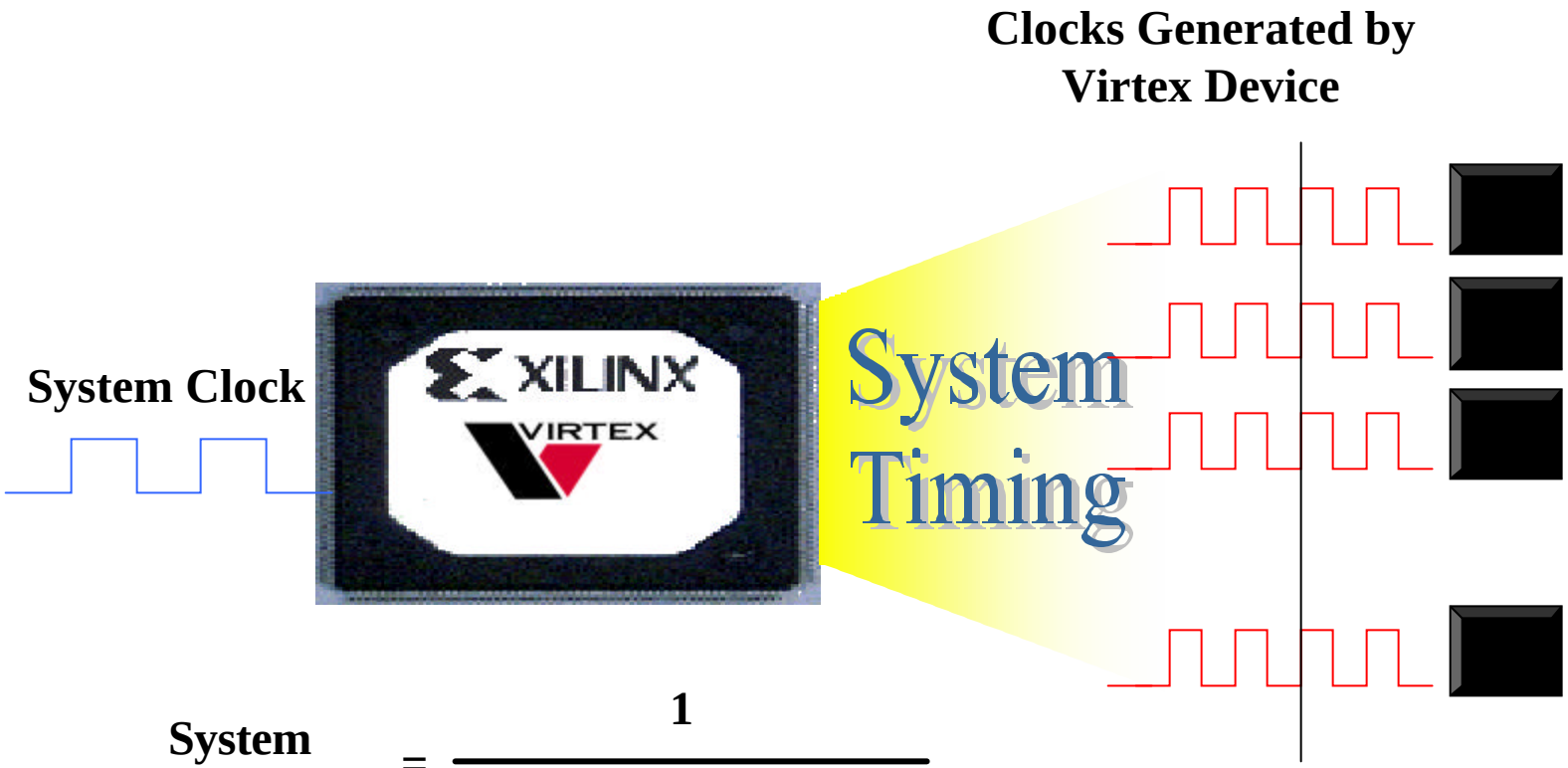


I/O Standard	Application
LVTTL	General Purpose
LVCMOS2	
PCI 33MHz 3.3V	
PCI 33MHz 5.0V	PCI
PCI 66MHz 3.3V	
GTL	Back-Plane
GTL+	
HSTL-I	
HSTL-III	Hitachi SRAM
SSTL3-I	
SSTL3-II	SDRAM
SSTL2-I	
CTT	Memory
AGP	Graphics

Thermal Management

SelectMAP
Advanced Configuration Technology

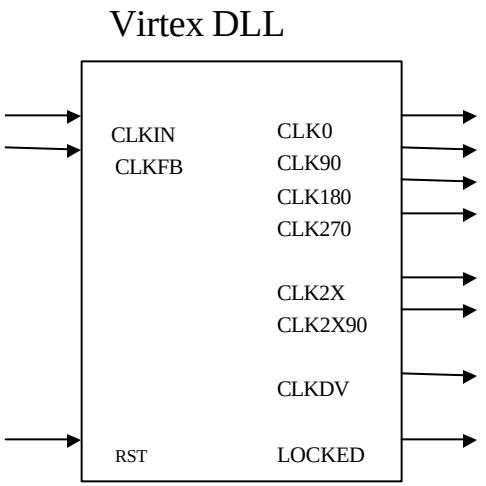
Pumping up System Performance



$$\text{System Performance} = \frac{1}{\text{Clock to Ouput} + \text{Input Setup} + \text{Clock Skew}}$$

Virtex Delay Locked Loop (DLL)

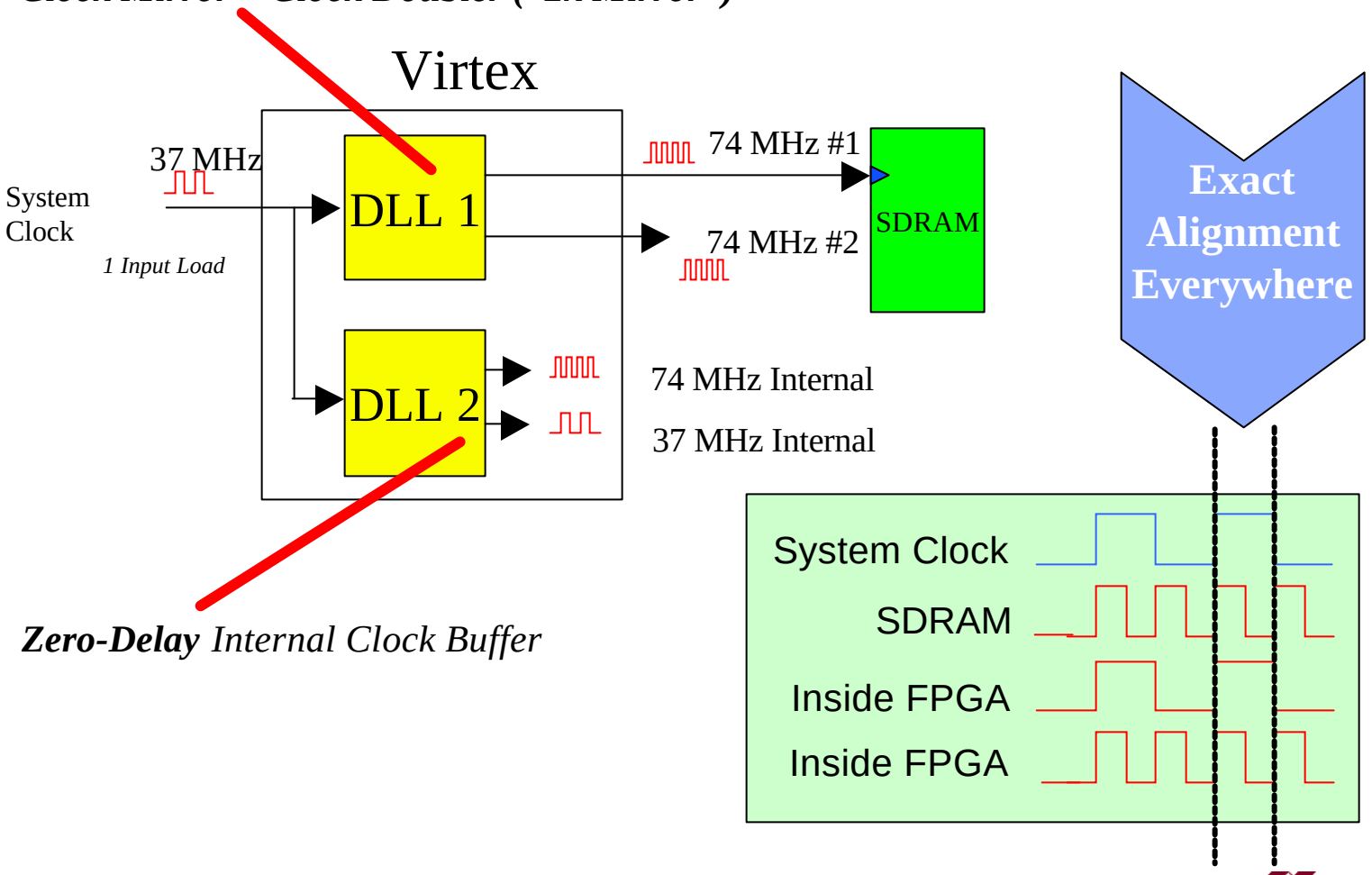
- Remove skew of multiple system clocks
  - 4 DLLs on every Virtex FPGA
  - Multiple outputs from each DLL
- Drive System Performance over 160 MHz
  - 2.5 ns Setup Time on all device
  - 0ns Hold Time on all devices
  - ***3.5 ns Clock-to-Out on all devices***
  - ***Less than 500ps skew across FPGA***
- Make clocks you need
  - Multiply clock frequency by 2
  - Divide clock frequency
  - Shift clock phase
- Generate clocks to other devices
  - Use multiple DLLs to remove internal and external clock skew



DLL Customer Design Example

HDTV Broadcast System

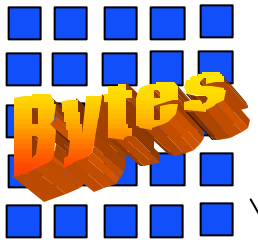
Clock Mirror + Clock Doubler ("2x Mirror")



***Zero-Delay** Internal Clock Buffer*

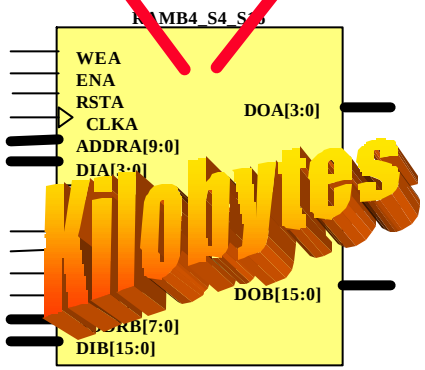
Building a Hierarchical Memory System

200 MHz Distributed SelectRAM+ Memory



System Memory

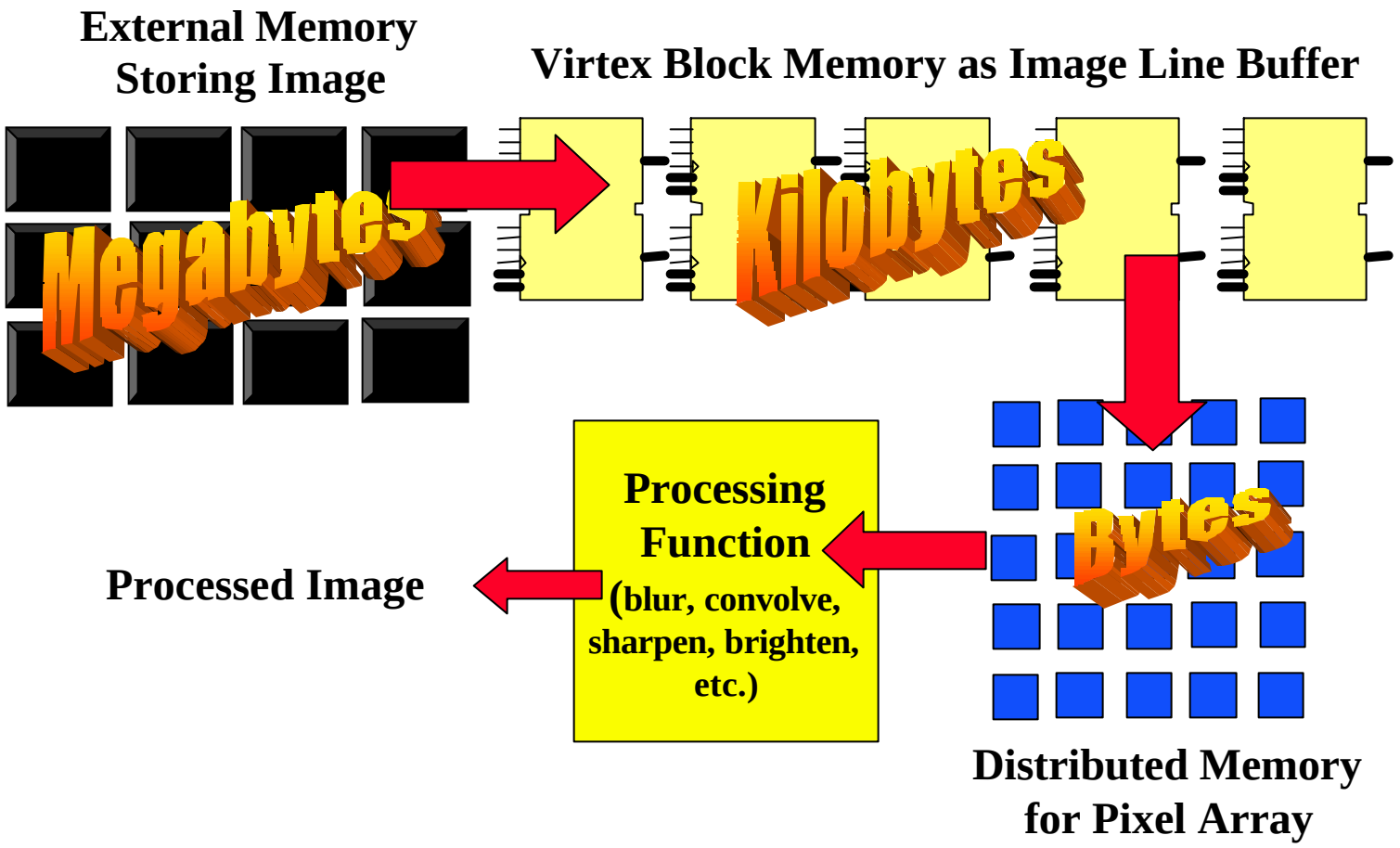
166 MHz Access to External Memory



200 MHz Block SelectRAM+ Memory

Memory Hierarchy Design Example

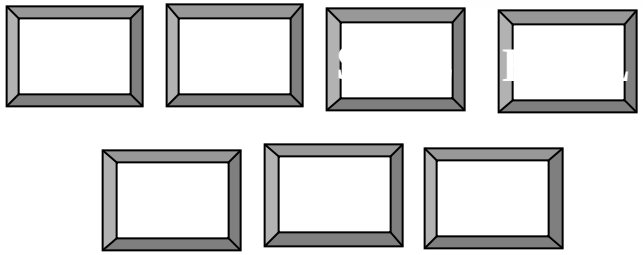
Photoshop Accelerator



Interface to any Device for Deep Sub-micron Era

Connect directly to external signals of varied voltages and swing points

System Interfaces



GTL GTL+ AGP

Backplanes

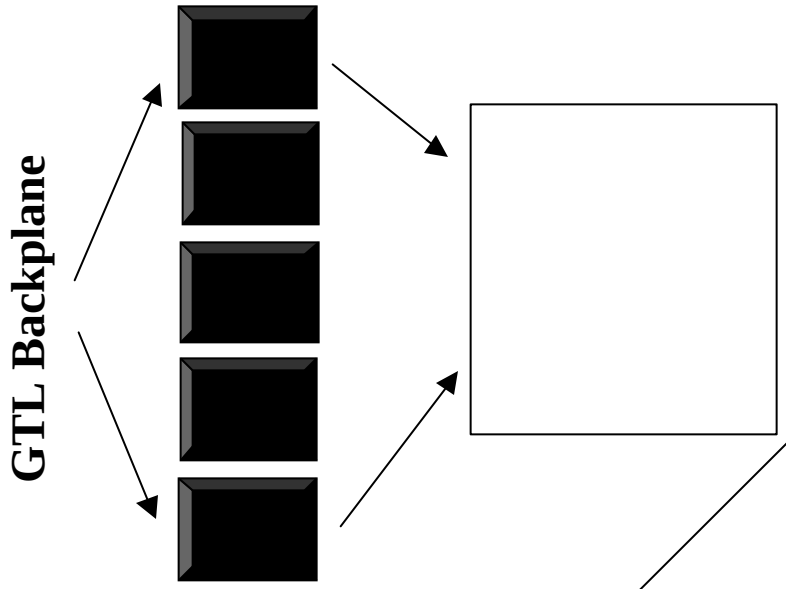
External Devices

Directly Interface to Virtex FPGA

Standard	Voh	Swing	Application
LVTTL	3.3	na	General purpose
LVCMOS2	2.5	na	General purpose
PCI 33MHz 3.3V	3.3	na	PCI
PCI 33MHz 5.0V	3.3	na	PCI
PCI 66MHz 3.3V	3.3	na	PCI
GTL	na	0.80	Backplane
GTL+	na	1.00	Backplane
HSTL-I	1.5	0.75	High Speed SRAM
HSTL-III	1.5	0.90	High Speed SRAM
HSTL-IV	1.5	0.75	High Speed SRAM
SSTL3-I	3.3	0.90	Synchronous DRAM
STTL3-II	3.3	1.50	Synchronous DRAM
SSTL2-I,II	2.5	1.10	Synchronous DRAM
AGP	3.3	1.32	Graphics
CTT	3.3	1.5	High Speed Memory

- ***Every I/O supports every standard***
- ***Device support multiple standards simultaneously***

SelectI/O Technology Cost Savings
Design Example

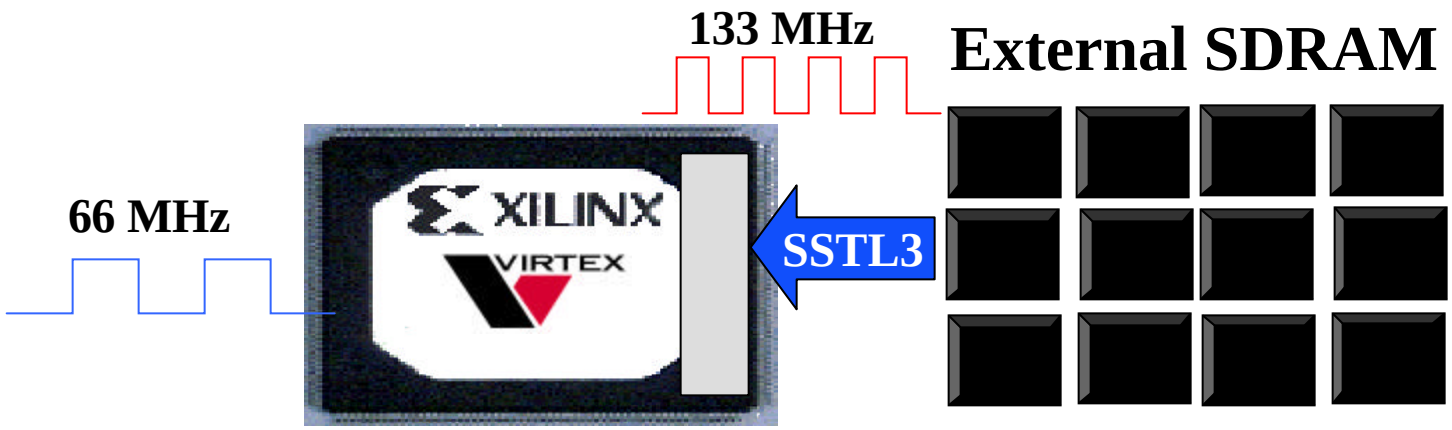


GTL to LVTTL Buffers

$200

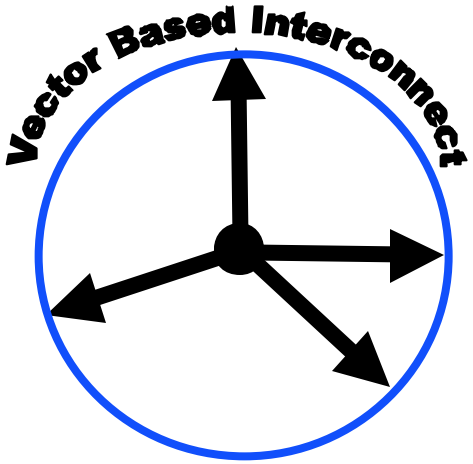
Buffers included

Combining System Level Features for High Speed Cache Memory



- Virtex DLL for 133 MHz clock synchronization of FPGA and SDRAM
- SSTL3 Interface to 133 MHz Fast SDRAM
- Virtex Block Memory for System Cache

Drop in Intellectual Property with Predictably Fast Performance



Delays are predictable as the straight line distance from source to destination

Core Friendly Architecture

System Integration

Available Virtex Cores

Building Blocks

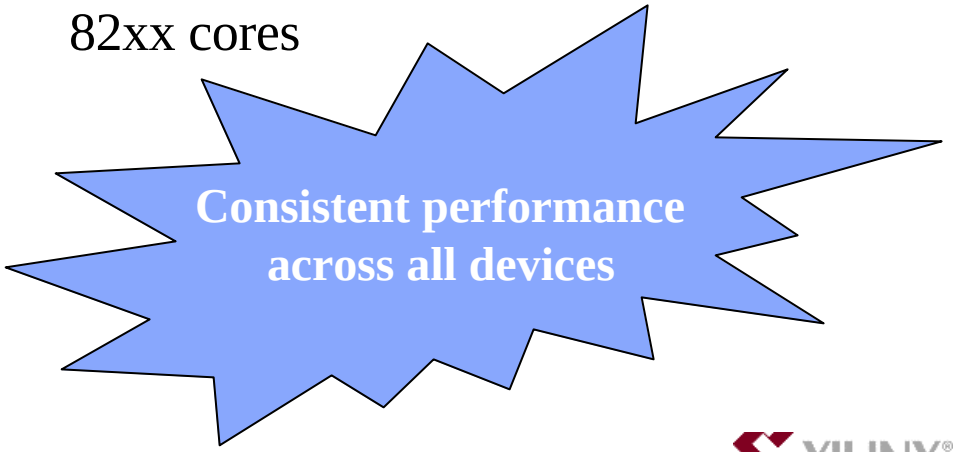
- Multiplexers
- Counters
- Registers
- Adders/Subtractors
- Accumulators
- Shift Registers
- Comparators
- Complementors

Memory

- Asynchronous FIFO
- Synchronous FIFO
- DMA controller
- Dual Port Block RAM
- Single Port Block RAM

Complex Cores

- Filters
- Reed Solomon - Encoder
- Reed Solomon - Decoder
- HDLC
- 622 MBPS SONET
- JPEG Encoder
- Video Streaming Core
- SDRAM Controller
- UART
- 82xx cores

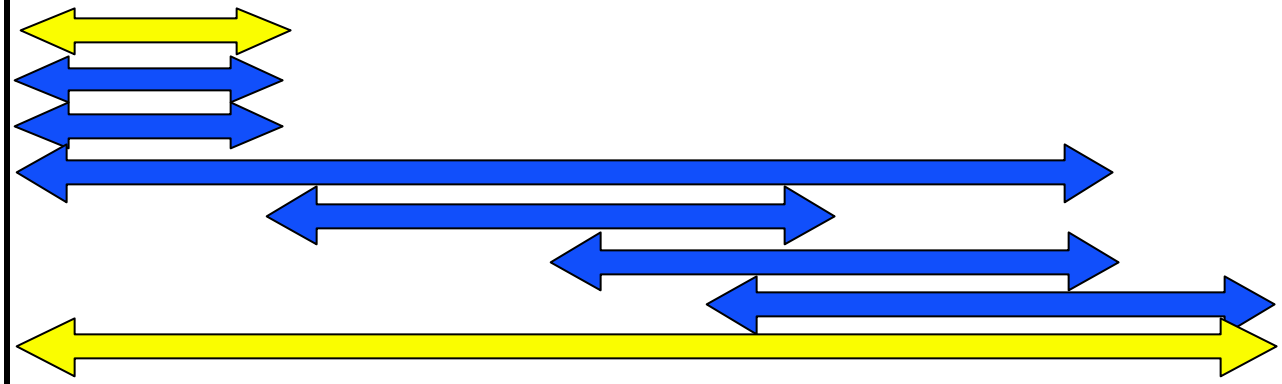


Virtex FPGA Family

Available now

Available now

Device	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
System Gates	50,000	100,000	150,000	200,000	**300,000**	400,000	600,000	800,000	**1,000,000**
Logic Cells	1728	2700	3888	5292	**6912**	10800	15552	21168	**27648**
Block RAM Bits	32,768	40,960	49,152	57,344	**65,536**	81,920	98,304	114,688	**131,072**
Packages									
0.8mm CSP									
VQ100									
TQ144									
PQ/HQ240									
BG352									
BG432									
BG560									
1.0mm BGA									



Industry Leading Price Points

Device	Volume Price
XCV50	$9.50
XCV300	$50.00
XCV1000	$350.00

End of 1999 pricing based on 100,000 units

Summary

- Virtex FPGAs shipping now and customers are completing designs today with it
- A powerful, unmatched combination of a robust feature set and expert technology to solve designers' challenges throughout the system—at industry leading price points
- Virtex FPGAs enable increased programmable content in existing and new applications