CUSTOMER TESTIMONIALS FOR VIRTEX

AdTech, Inc., Hawaii

"These million gate devices enable our test modules to provide thousands of continuous measurements at telecom speeds up to 2.4 gigabits per second. We especially like the fact that Virtex devices are programmable. This allows us to use a single test module for multiple transmission technologies such as ATM and frame relay, which provides huge cost savings and convenience for our customers plus future enhancement capability."

Carl Uyehara, vice president of Engineering

Hughes Space and Communication Company, Los Angeles, CA

"The critical features of Virtex, such as the segmented routing and 0.22 micron feature size, allowed new levels of performance for our high-speed digital designs. The lower voltage and higher performance logic of the Virtex process are unmatched from any other supplier. The level of support from the design development and the hotline assistance that Xilinx offered with the new family also impressed us."

Ted Pascaru, Senior Staff Engineer

News Data Services (NDS)

"Virtex FPGAs have allowed us to implement our next generation digital TV broadcast systems in record time. A key time saver was the availability of multiple DLLs that allowed us to synchronize a 74 MHz clock to more than 30 devices including multiple FPGAs, SDRAMs, and other components. Designing a no-skew clock system from scratch would take months. Xilinx delivered a ready-made solution to us with Virtex FPGAs."

John Simmons, Project Manager

Nortel Networks

"In our next generation networking product, we specifically needed block RAM with true dual-port capabilities. We investigated various programmable solutions available and found that no other vendor could provide a single chip solution containing block memory with the ability to read and write to one port and simultaneously read from the other. Additionally, the Virtex DLLs performance was required in order to interface directly to an ASIC running at 78 MHz. Not only do Virtex devices meet our 78 MHz internal performance requirements, they meet our external interface performance requirements by providing very fast 'clock-to-out' timing on even the slowest device."

Ranvir Chitkara, Director of Engineering