NEUTRON SINGLE EVENT UPSETS IN SRAM-BASED FPGAs*

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Abstract

SRAM-based FPGAs have been studied for their sensitivity to atmospheric high energy neutrons. FPGAs with the supply voltage 5V and 3.3V were irradiated by 0-11, 14 and 100 MeV neutrons and showed a very low SEU susceptibility.

I. Introduction

Programmable Logic Devices, and more specifically Field Programmable Gate Arrays (FPGA), are replacing traditional logic circuits by offering the advantages of high integration (small size, low power, and high reliability) without the disadvantages of custom ASICs (high non-recurring engineering cost and high risk, especially in limited production volume). FPGAs based on SRAM technology offer an additional unprecedented advantage, they can be reprogrammed an unlimited number of times, even in the end-user system. In these FPGAs, a multitude of latches, also called memory cells or RAM bits, define all logic functions and on-chip interconnects. Such latches are similar to the 6-transistor storage cells used in SRAMs, which has proved to be sensitive to single event upsets caused by high-energy neutrons. The faults have been observed as bit errors in memories. The phenomenon has been observed at both aircraft altitudes and on ground [1-3], and is now considered an issue in the dependability of airborne electronics.

Because of this similarity to SRAM technology, it is meaningful to test whether FPGAs also are susceptible to bit errors caused by high energy neutrons. For practical reasons, such investigations need to be made in stationary equipment at ground level. Different neutron sources can be used in order to test electronic devices, but a careful evaluation of the results is needed in order to make good predictions for the real atmospheric radiation environment [4]. Recently, field programmable devices based on different technologies have been studied using heavy ions and protons for space applications [5].

In this study, we have determined the sensitivity to neutron induced single event upsets in SRAM-based FPGAs. Three different high-energy neutron sources were used in the study. The results are evaluated to estimate the SEU frequency in the real radiation environment.

II. Experimental details

A. Neutron facilities

Three different neutron facilities were used for obtaining the experimental results;

- Risø National Laboratory, Denmark (Risø). The PuBe-source at Risø produce a neutron spectrum with energy E_n = 0-11 MeV.
- Chalmers Institute of Technology, Sweden (CTH). The $^2D+^3T$ reaction at CTH gives monoenergetic neutrons with E_n = 14 MeV.
- The Svedberg Laboratory, Sweden (TSL). Cyclotron produced neutrons from the $^7Li(p,n)^7Be$-reaction, gives a quasi-monoenergetic neutron spectrum with peak energy E_n = 100 MeV. The $^7Li(p,n)^7Be$ reaction use a 100-800 mg/cm^2 thick lithium target, enriched to 99.98% in ^7Li. The distance from the lithium target to the irradiation position was about 12 m, giving a neutron beam diameter of about 10 cm. This SEU test was performed simultaneously with a nuclear physics experiment at the same beam line. In that experiment, a large magnetic spectrometer was used, but only negligible amounts of material was present in the neutron beam before the irradiation position.

B. Device descriptions

The tested devices were XC4010E and XC4010XL, manufactured by Xilinx. The devices contain 178,096 (XC4010E) and 283,376 (XC4010XL) RAM-bits. In the latter only 253,704 bits were tested, due to limitations in the

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experimental setup. A summary of the tested devices are found in table 1.

Table1

Device	Package	Date	Process	Vcc
XC4010E-4	PLCC84	9612	0.60µm CMOS	5V
XC4010XL-4	PLCC84	9733	0.35µm CMOS	3.3V

The XC4010E uses 5V as supply voltage and is manufactured in a 0.60um Three Layer Metal (TLM) process, which is used for the military mask set of the device. The XC4010XL is a 3.3V device and is manufactured in a 0.35um Quad Layer Metal (QLM) process, which is also used for the military mask set.

C. Experimental setup

The experimental setup is based on four DUT-boards with four FPGAs on each board. Each FPGA were configured with a Serial Configuration Prom (SCP) external to the device. Configuration mode is Master Serial, i.e. each FPGA has their own SCP and the data transmission is serial. Because the configuration proms are manufactured in an EPROM-technology the configuration data in the SCP will not be affected by the neutron radiation.

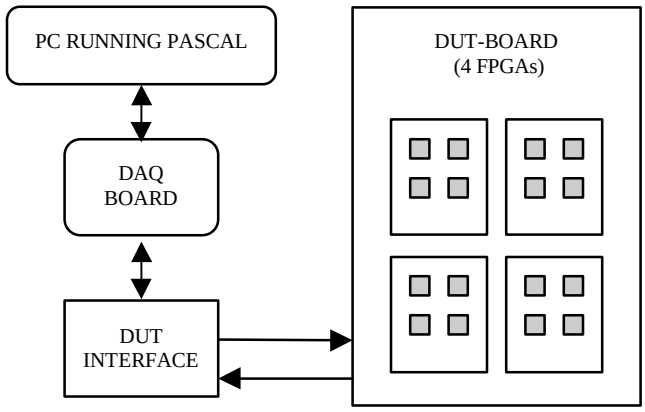

Figure 1: Schematic of experimental setup

D. Test Procedure

To detect bit errors in the devices, a dummy logic function was designed and the originally configuration bitstream was implemented in each FPGA from the SCP. Using the standard Readback feature, the bitstream was then continuously read back during ongoing irradiation, and this serial data was compared against the originally loaded bitstream. When an error was detected, time, device number, read data and expected data were logged in a text file. After the whole bitstream had been read out the entire FPGA was reconfigured.

This method of bit-error detection ensures a complete control of the FPGA storage cells content, better than executing logic functions and checking the FPGA's output. Note that Readback is a non-destructive operation that does not affect the content of the configuration storage cells.

III. Results and Calculations

A. Experimental results

In the first experiment at Risø (PuBe), 16 FPGAs (XC4010E) were irradiated for 261 hours with the neutron flux $5.6 \cdot 10^3$ $cm^{-2}s^{-1}$. No SEUs were detected. The neutron flux is corrected to contain only neutrons with energy above 5 MeV, which is a reasonable lower limit for neutron induced SEUs in silicon devices [3]. The onset of charged particle production in silicon is found in that range, and thus a very small cross section for SEU is expected below about 5 MeV.

In the second experiment, 4 FPGAs (XC4010E) were irradiated for 4 hours by 14 MeV neutrons, with the neutron flux $6 \cdot 10^6$ $cm^{-2}s^{-1}$ No SEUs were detected in this experiment either.

In the third experiment, 16 FPGAs (8 XC4010E and 8 XC4010XL) were irradiated for 9 hours with quasi-monoenergetic 100 MeV neutrons. The neutron flux was $9.3 \cdot 10^3$ $cm^{-2}s^{-1}$. During this experiment six SEUs were recorded. Five of these SEUs were detected in the XL-device (3.3V) and one SEU were detected in the E-device (5V). Five (4+1) of the SEUs were data errors, a single bit had changed but no other effects were detected. However, one SEU in one XC4010XL device disabled the Readback function such that, from a certain position in the bitstream on, no further data could be read back from the device. It is assumed that this SEU disturbed the state-machine register responsible for the internal parallel-to-serial conversion of the Readback bitstream. All six errors were soft errors, since reconfiguring each affected device rendered it fully functional again.

For the calculation of upset cross-sections for the devices, we need to take into account the shape of the neutron spectrum from the source. Being a quasi-monoenergetic neutron source, the $^7Li(p,n)^7Be$ reaction produces a peak and a low energy tail. At 100 MeV about half of the neutron flux is found in the peak and the remaining neutrons are in the tail [6, 7]. Since the whole spectrum (almost) contributes to the measured SEU cross section, we need to correct for the upsets caused by neutrons with energies below the peak. The corrections is made by unfolding a measured SEU cross section energy dependence with the spectrum of the neutron source. This gives correction factors to be applied to the quasi-monoenergetic values to obtain true monoenergetic cross sections. We

assume that these SRAM-based FPGAs follow the same energy dependence which is found for different types of SRAM memories [8], even thought we only have detected SEU at a single neutron energy. The obtained, corrected cross-sections are found in table 2.

Table 2

Device	Location	Neutron energy (MeV)	Neutron flux ($cm^{-2}s^{-1}$)	Irradiation time (h)	Number of devices	Number of SEUs	SEU cross section (cm^2/bit)
XC4010E	Risø	0-11	$5.6 \cdot 10^3$	261	16	0	0
XC4010E	CTH	14	$6 \cdot 10^6$	4	4	0	0
XC4010E	TSL	100	$9.3 \cdot 10^3$	9	8	1	1.3×10^{-15}
XC4010XL	TSL	100	$9.3 \cdot 10^3$	9	8	4+1	4.4×10^{-15}

B. SEU-rate calculation

An estimated SEU frequency at aircraft altitudes can be calculated. For the calculation of single event upset rate for the devices a simplified radiation environment model is used. In that mode the neutron flux dependencies of altitude, latitude and energy are considered to be fully separable. The energy dependence of differential neutron flux is described by

$$\frac{dN}{dE} = kE^{-0.9219} \exp\left[-0.01522(\ln E)^2\right] \quad (1)$$

in units of n/cm^{2}s MeV. The constant k then depends on altitude and latitude, and is here put to a value giving the total neutron flux 2 n/cm^{2}s in the energy range 5-1000 MeV. The upset rate is calculated using the assumption that these devices have the same SEU energy dependence as CMOS SRAM devices is found to possess [8]. The upset rate is calculated straightforward as

$$f_{SEU} = \int_{5MeV}^{1000MeV} s_{SEU,monoenergetic}(E)\frac{dN}{dE}dE \quad (2)$$

The calculated upset rates at 10 km altitude at 60ºN (Sweden), are found in table 3.

Table 3

Device	SEU-rate at 10 km altitude (60ºN) [upset/h·device]
XC4010E	$7.6 \cdot 10^{-7}$
XC4010XL	$3.6 \cdot 10^{-6}$

The SEU frequency for the XC4010E is approximately average 1 bit error per $1.3 \cdot 10^6$ flight hours, while the XC4010XL has an estimated SEU frequency of 1 bit error per $2.8 \cdot 10^5$ flight hours at 10 km altitude.

IV. Discussion

We compare these results to those obtained for SRAM-devices (memory circuits). In general, SRAM-devices have SEU cross sections in the range 10^{-14}-10^{-12} cm^2/bit [9]. These FPGAs show cross sections that are about one order of magnitude below the lower limit reported for SRAMs.

A possible explanation might be found in the design of the FPGA storage cells. Since configuration storage is not the dominant feature in an FPGA, the storage cell need not be as small, nor as fast as required in typical SRAM devices. The FPGA storage cell consists of two cross-coupled inverters with active pull-down and active pull-up transistors, each with an on-impedance of about 5 kΩ, similar to the 6-transistor cells found in smaller SRAMs. Typical modern SRAMs often use a 4-transistor cell with active pull-down transistors, but very high-impedance pull-up poly-silicon resistors of about 5 GΩ. That may make conventional SRAMs more susceptible to soft errors.

V. Conclusion

The FPGAs show a very low susceptibility to single event upsets caused by neutrons. No permanent effects were detected, reconfiguration of the device was sufficient to regain full functionality after the occurrence of a single event upset.

We conclude that these SRAM-based FPGAs can be used without limitation in the atmospheric radiation environment, contrary to SRAM memories were precaution in the use is necessary because of neutron induced SEU.

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