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Features

- Drop-in module for Virtex, Virtex™-E and Spartan™-II FPGAs
- Supports buses of up to 64 bits wide
- 1 to 64 inputs
- Incorporates Xilinx Smart-IP technology for maximum performance
- To be used with version 2.1i and later of the Xilinx CORE Generator System

Functional Description

The BUFE-based multiplexer slice is a member of the BaseBLOX series of building blocks for the Virtex architecture. The only option is to select the size of the input bus. Combining the outputs of multiple BUFE-based multiplexer slices allows the creation of larger tristate multiplexers.

Pinout

Signal names for the schematic symbol are shown in Figure 2 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
I[N:0]	Input	Multiplexer slice input bus
OE	Input	Output enable control
O[N:0]	Output	Multiplexer slice output bus

Note:

All control inputs are Active High. Should an Active Low input be required for a particular control pin an inverter must be instantiated in the path to the pin. The inverter will be absorbed during mapping.

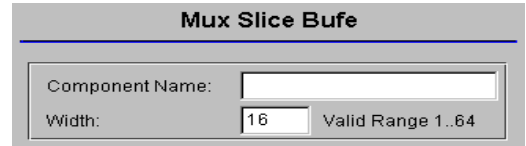


Figure 1: BUFE-based Multiplexer Slice Parameterization Screen

CORE Generator Parameters

The main CORE Generator parameterization screen for this module is shown in Figure 1. The parameters are as follows:

- **Component Name:** The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and "_".
- **Bus Width:** Select the width of the inputs buses (and hence the width of the output bus). The valid range is 1 to 64. The default value is 16.

Parameter Values in the XCO File

Parameters and their values in XCO files are based upon the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case insensitive.

Table 2 shows the XCO file parameters and values, as well as summarizing the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET width = 16
CSET component_name = c_mux_slice_bufe
```

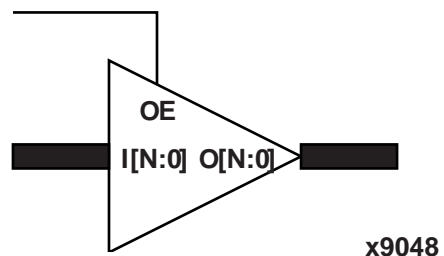


Figure 2: Core Schematic Symbol

Core Resource Utilization

This module uses one BUFE primitive per input bit.

Ordering Information

It is important to set a maximum period constraint on the core's clock input. Table 3 and Table 4 show speeds that can be achieved when this is done.

Information on Virtex slice count and RPM dimensions is listed in Table 3 for several Virtex multipliers.

Table 2: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and "_"	blank
width	Integer in the range of 1 to 64	16