Multiplier Accumulator V1.0

November 3, 2000 Product Specification

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Features

- Drop-in module for Virtex™, Virtex™-E, Virtex™-II, and Spartan™-II FPGAS
- Parallel multiplier accumulator module
- Performs fixed or programmable-length accumulations
- Input (A) uses unsigned or signed data up to 32 bits wide
- Input (B) uses unsigned or signed coefficients up to 32 bits wide
- Coefficient may be set in one of three modes:
  - Constant mode for a fixed coefficient value
  - Dynamic Constant mode allowing new coefficients to be loaded when needed
  - Dynamic mode where coefficients are loaded in parallel with input data
- Pipelining with user-selectable effort levels
- Truncation and rounding of the multiplier output
- Accumulator size can be in the range 1 to 65 bits
- Accumulator supports addition or subtraction, selected by an input pin
- Accumulation saturation option
- Optional carry in, carry out, and overflow pins
- Selectable input and output registers
- Configurable hand-shaking signals allow easy interfacing with other modules
- High performance and density by using Xilinx relational placed macro (RPM) mapping and placement technology

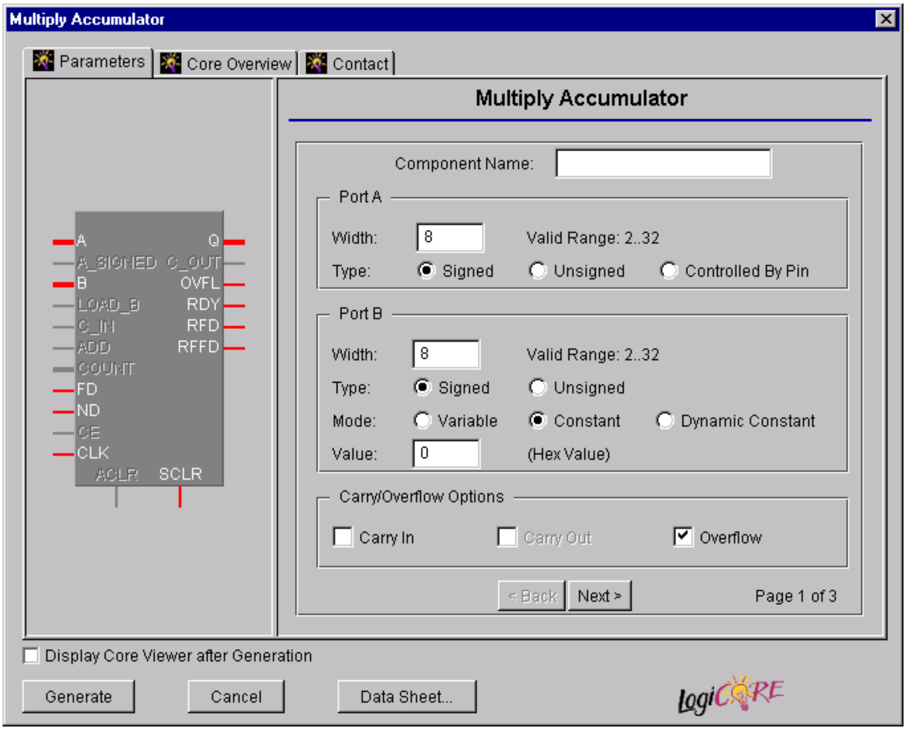

Figure 1: Main MAC Parameterization Screen

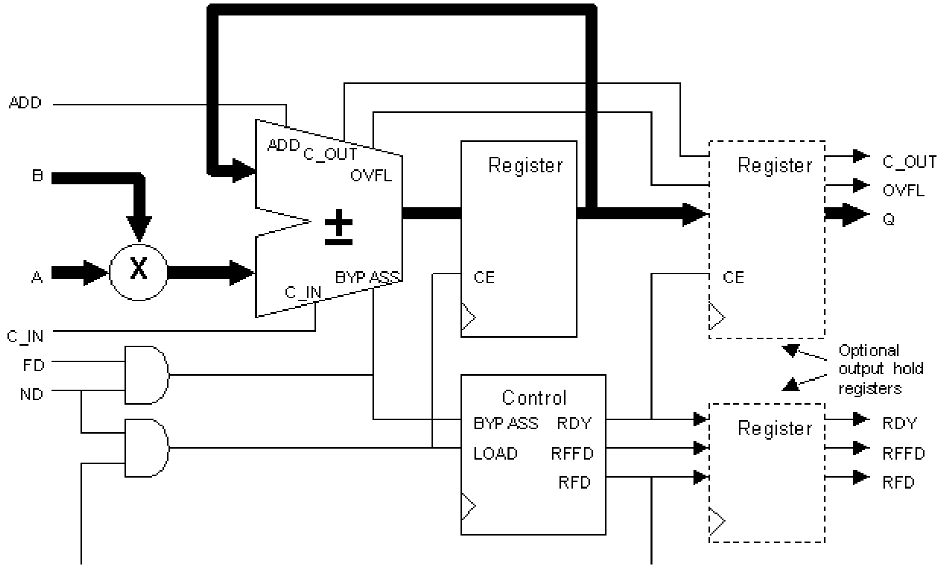

Figure 2: MAC Block Diagram

Functional Description

The overall function of the Multiplier Accumulator (MAC) is shown by the following Equation:

Equation 1:
$$Q = \sum_{n=0}^{count-1} (\pm 1) * A(n) * B(n)$$

'Q' is the primary data output of the core. 'A' and 'B' are multiplied together and the product added or subtracted from the current result. A simplified schematic of the core is shown in Figure 2.

The *count* value in Equation 1 is set to a fixed value by a parameter. An alternative configuration allows this value to be set at the start of each new accumulation using the optional 'COUNT' input port. A *count* value of 0 is interpreted as infinity.

Multiplier

A(n) is a data input to the module which is sampled on the rising clock edge when 'ND' (New Data) is asserted and the module is ready to accept New Data.

B(n) is configurable in one of three modes as follows:

- **Constant Mode:** *B(n)* is a pre-defined constant parameter.
- **Dynamic Constant Mode:** *B(n)* has a pre-defined value, as with **Constant** mode, but the value may be re-loaded at any time from the 'B' input port. This is done by asserting the 'LOAD_B' input. The load operation takes 16 clock cycles to complete.
- **Variable Mode:** *A(n)* and *B(n)* are sampled simultaneously.

The data formats for ports 'A' and 'B' are shown in Table 1 and Table 2 respectively. The maximum input width of 'B' depends on the **Port B Mode.**

Table 1: Port 'A' Input Format

Port A Type	Port A Width	
	Min	Max
Unsigned	1	32
Signed	2	32
Pin	2	32

Table 2: Port 'B' Input Format

Port B Mode	Port B Type	Port B Width	
		Min	Max
Variable	Unsigned	1	32
	Signed	2	32
Dynamic Constant	Unsigned	1	26
	Signed	2	26

Table 2: Port 'B' Input Format

Constant	Unsigned	N/A	N/A
	Signed	N/A	N/A

Multiplier Pipelining

The module can be optionally pipelined. If pipelined, the critical paths within the core are reduced and the latency is increased.

Pipelining and latency are controlled using the **Pipelining Level** pull-down menu. In this version of the core, only the multiplier is pipelined. The effect of parameter choice on the latency is explained in the Latency section later in this datasheet.

If **Port B Mode** is **Constant** or **Dynamic Constant,** the level of pipelining may be "0" or "MAX." If **Port B Mode** is **Variable,** three levels of pipelining are available: "0," "1," and "MAX."

The effect of each pipeline level is as follows:

- "0" – Multiplier is combinatorial
- "1" – Multiplier is combinatorial with output registers
- "MAX" – Multiplier has internal pipeline and output registers

Accumulator

The accumulator can be used in one of two modes: Adder or Adder/Subtractor. In the latter case, an 'ADD' input pin selects addition or subtraction.

The accumulator has an optional carry input. An optional carry or overflow output can also be specified. The availability of carry and overflow signals depends on the input data types as shown in Table 3.

Table 3: Accumulator Carry and Overflow Options

Port A Type	Port B Type	Carry In	Carry Out	Overflow
Unsigned	Unsigned	Yes	Yes	No
Signed	Unsigned	Yes	No	Yes
Pin	Unsigned	Yes	No	Yes
Unsigned	Signed	Yes	No	Yes
Signed	Signed	Yes	No	Yes
Pin	Signed	Yes	No	Yes

Table 4 shows the accumulator type resulting from all possible data input types.

Table 4: Input and Accumulator Data Types

Port A Type	Port B Type	Accumulator Output
Unsigned	Unsigned	Unsigned
Don't Care	Signed	Signed
Signed	Don't Care	Signed
Pin	Don't Care	Signed

The module has an option to round the output of the multiplier prior to accumulation.

The first input data to an accumulation is multiplied and the result truncated. For the remainder of the Multiply-Accumulate operation, the multiplier output can be rounded. Rounding can be used only if the number of **Significant Multiplier Output Bits** is less than the multiplier width.

As an example of rounding, consider an 8-bit multiplier result of "10011000." Assume that the result is truncated to 4 bits. If rounding is not selected, the result will be "1001." If rounding is selected, the MSB of the discarded portion equals "1" so the result is "1001" + "1" = "1010." If the multiplier result was truncated to 5 bits, the MSB of the discarded portion would be "0" so the result would be "10011."

The module can be configured to perform saturation during accumulation. If the result of the accumulation exceeds the range of the accumulator, the accumulator result register is set to a predefined value according to Table 5.

Table 5: Saturation Option

Type of Accumulator Output	MAC Result	Accumulator Output
Unsigned	$> Q_{max}$	All bits = '1'
Signed	$> Q_{max}$	MSB = '0', all other bits = '1'
Signed	$< Q_{min}$	MSB = '1', all other bits = '0'

Interface and Control

A number of control signals allow interfacing with external logic.

There are two control input signals, 'FD' (first data) and 'ND' (new data). 'FD' is asserted for the first input to a new accumulation. 'ND' indicates that new data is available to the module at port 'A'.

The output status signal, 'RFD' (ready for data) is high when the module is ready to accept new data. 'RFFD' (ready for first data) indicates that the module is ready to accept data for a new accumulation.

The interaction between the control signals 'FD', 'ND', 'RFD' and 'RFFD' is illustrated in Figure 3. In this example, the MAC is configured to multiply and accumulate four values (**MAC Count** = 4). The output, 'Q', is registered (**Output Hold Registers** = 1).

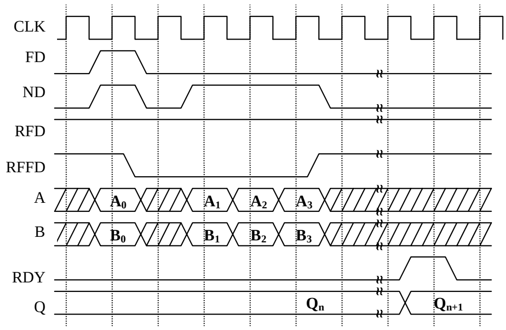

Figure 1: Control Timing Example – MAC Count =3

In Figure 4 below, ‘FD’ is asserted before the MAC Count value is reached causing the partially accumulated result to be output.

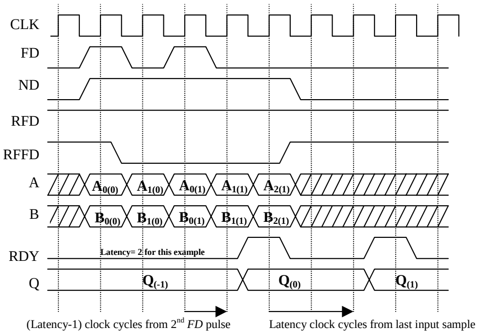

Figure 1: Control Timing Example – FD asserted before MAC Count is reached. MAC Count = 3

The ‘LOAD_B’ control pin is included when the **Dynamic Constant** input mode is used. The value on port ‘B’ is loaded into the multiplier when ‘LOAD_B’ is asserted as illustrated in Figure 5. ‘RFD’ is low while loading (16 clock cycles).

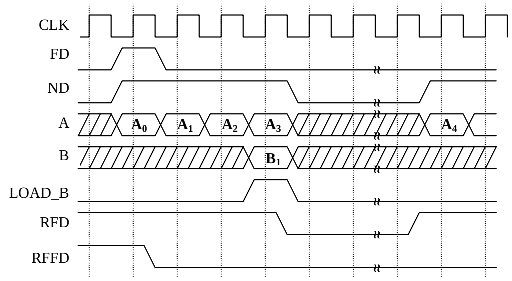

Figure 1: Dynamic Constant ‘B’ Input Timing Example

The optional ‘COUNT’ input bus can be used to set the number of Multiply-Accumulate operations. Its width is defined by the parameter **Count Width**. A timing example is shown in Figure 6. A new *count* value is always loaded when ’FD’ is high.

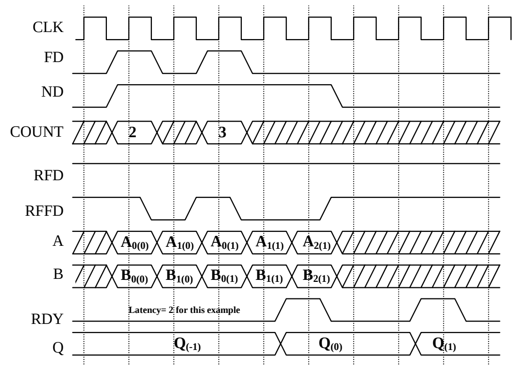

Figure 1: Count Value Load Timing Example

Pinout

A representative symbol with signal names is shown in Figure 7. Optional ports are illustrated with dotted lines.

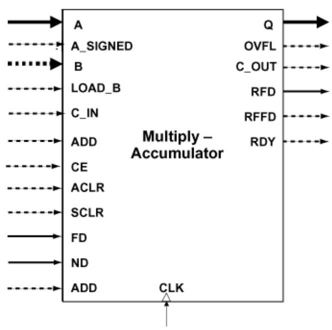

Figure 7: Schematic Symbol

Signal functions are summarized in Table 6 and Table 7. They are described in more detail in the remainder of this section. The mandatory ports are essential to the core; optional ports depend on the parameters used.

Table 6: Mandatory Ports

Port Name	Direction	Description
CLK	Input	Clock, active on the rising edge
A	Input	Primary multiplier data input bus
Q	Output	MAC data output bus
FD	Input	First Data; indicates the start of a new MAC operation (active high)
ND	Input	New Data: indicates that new input data is present (active high)
RFD	Output	Ready For Data: indicates that the core is ready for new input data (active high)

Table 7: Optional Ports

Port Name	Direction	Description
B	Input	Secondary multiplier data input bus
LOAD_B	Input	Load new *B(n)* coefficient (active high)
ADD	Input	Select addition or subtraction from accumulator (active high)
OVFL	Output	Overflow: indicates that the accumulator has overflowed (active high)
C_IN	Input	Carry Input to accumulator
C_OUT	Output	Carry Output from accumulator
CE	Input	Clock Enable
A_SIGNED	Input	Defines ‘A’ input data sign. If high, data is signed.
RFFD	Output	Ready For First Data: indicates that the module is ready to begin a new MAC operation
RDY	Output	Signals that a new result is available on ‘Q’
COUNT	Input	MAC Count value, loaded when ‘FD’ is high
ACLR	Input	Asynchronous Clear
SCLR	Input	Synchronous Clear

The following is a short description of each pin and GUI parameters that affect its operation.

A Input

The input port for *A(n)* data. The width is set by the **Port A Width** parameter and has a range of 1 to 32 for unsigned values and 2 to 32 for signed values.

B Input

The input port for *B(n)* data. In **Variable** mode the data is sampled on the rising edge of the clock if the module is ready to accept new data. In **Dynamic Constant** mode, a new value may be loaded using the ‘LOAD_B’ input.

Q Output

The output port for the resulting accumulation. The width is defined by the parameter **Significant Accumulator Output Bits** and must not be greater than the accumulator width. If the width is less than that of the accumulator, the most significant accumulator bits are selected.

The type of ‘Q’ depends on ‘A’ and ‘B’ as shown in Table 4.

FD (First Data) Input

The ‘FD’ input indicates the start of a new Multiply-Accumulate operation. Data for a new accumulation is sampled on port ‘A’ when this signal is high and the module is ready to accept new data.

ND (New Data) Input

The ‘ND’ input signifies that new data is available for accumulation. New data is loaded from port ‘A’ when this signal is high and the module is ready to accept new data.

RFD (Ready For Data) Output

The ‘RFD’ output is asserted high when the core is ready to accept new data.

RFFD (Ready For First Data) Output

The optional ‘RFFD’ output is asserted high when the core is ready to begin a new accumulation

RDY (Ready) Output

The optional ‘RDY’ output is asserted high when the result of an accumulation is ready. ‘RDY’ indicates that ‘Q’, ‘C_OUT’ and ‘OVFL’ signals are valid.

LOAD_B Input

This pin is included when the **Dynamic Constant** input mode is used. The value on port ‘B’ is loaded into the multiplier when ‘LOAD_B’ is asserted. ‘RFD’ is low while loading (16 clock cycles).

ADD Input

This is an optional input allowing the accumulator to add or subtract during accumulation if 'ADD' is high or low, respectively.

OVFL (Overflow) Output

'OVFL' is an optional output that is asserted high if the accumulator overflows. 'OVFL' is associated with the 'Q' output and is valid when 'RDY' is high. Overflow is available if the MAC produces a signed result (Table 4).

C_IN Input

'C_IN' is an optional input pin that is sampled at the same time as the input data, 'A'. The carry input is added to the result of the multiplication of 'A' and 'B'. 'C_IN' is available if the MAC produces an unsigned result (Table 4) and multiplier rounding is not used.

'C_IN' is ignored while 'FD' is asserted.

C_OUT Output

'C_OUT' is an optional output pin that is available if the MAC has an unsigned result (Table 4). 'C_OUT' is associated with the 'Q' output and is valid when 'RDY' is high.

CE Input

An optional Clock Enable input. CE enables the clock to the accumulator, output and control registers in the module. When CE is low, the clock may not change the state of the module.

A_SIGNED Input

Optional pin for selecting the sign of the input data port, 'A'. When 'A_SIGNED' is high, data is treated as signed two's complement. When low, data is treated as unsigned.

ACLR Input

This optional Asynchronous Clear input is active high. When asserted, the content of the accumulator is cleared to zero.

SCLR Input

This optional Synchronous Clear input is active high. When asserted, the content of the accumulator is cleared to zero.

COUNT Input

The optional 'COUNT' bus input is used to set the number of Multiply-Accumulate operations. The width of this is defined by the parameter **Count Width**. The count value is loaded when 'FD' is asserted.

Parameters

The core GUI provides a number of parameters to allow a wide selection of MAC modules to be generated. This section describes the function and range of each parameter.

- **Component Name:** The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and "_".
- **Port A Input Options:**
  - **Port A Width:** The width of the 'A' input. The valid range is 1 to 32 for unsigned inputs and 2 to 32 for signed inputs.
  - **Port A Type:** The type of 'A' input data. The default value is **Signed**. 'A' may be **Unsigned**, **Signed**, or **Controlled By Pin**.
- **Port B Input Options:**
  - **Port B Width:** The width of the 'B' input. The valid range is 1 to 32.
  - **Port B Type:** The type of 'B' input data. The default value is **Signed** and may be changed to **Unsigned**.
  - **Port B Mode:** The mode of operation of 'B'. **Constant** sets *B(n)* to a constant value as specified by the **Port B Value** parameter. **Dynamic Constant** initializes *B(n)* to the constant value specified. A new value may be loaded dynamically. **Variable** mode treats port 'B' in the same way as port 'A'. Input data is latched on the rising clock edge, if 'FD' is high and the module is ready to accept new data.
  - **Port B Value:** This is the value of *B(n)* in **Constant** mode. In **Dynamic Constant** mode this sets the initial value, *B(0)*. This parameter is unused in **Variable** mode.
- **Carry / Overflow Options:**
  - **Carry In:** Selects optional carry input pin.
  - **Carry Out:** Selects the optional carry output. This parameter is relevant if the accumulator is unsigned (Table 4).
  - **Overflow:** Selects the optional overflow output. This parameter is relevant if the accumulator is signed (Table 4).
- **Register Options**
  - **Output Hold Registers:** Allows selection of optional output registers. These registers hold the 'Q' and optional 'OVFL' and 'C_OUT' values as shown in Figure 2 on Page 2. The values are updated when a new Multiply-Accumulate result is ready. If output hold registers are not selected, the 'Q', 'OVFL' and 'C_OUT' values will be undefined while the accumulator is performing a MAC operation.
  - **Register Inputs:** Inputs 'A' and 'B' may be optionally registered.
- **Clear Options**
  - **Asynchronous Clear:** If selected, the accumulator contents and outputs 'Q' and 'RDY' may be reset to zero asynchronously by the 'ACLR' pin.
  - **Synchronous Clear:** If selected, the accumulator contents and outputs 'Q' and 'RDY' may be reset to zero synchronously by the 'SCLR' pin.

- **SCLR Overrides CE:** If selected, an active level on 'SCLR' will be acted upon regardless of the status of 'CE'.

- **Optional Pins**
  - **CE (Clock Enable):** If selected, the module is generated with an active high clock enable input.
  - **ADD:** If selected, this allows either addition or subtraction to be performed during accumulation. An 'ADD' input pin is provided which is sampled with the input data, 'A'. If 'ADD' is high, the product of 'A' and 'B' is added to the accumulator. If 'ADD' is low, the product of 'A' and 'B' is subtracted from the accumulator.
  - **RFFD (Ready For First Data):** If selected, the 'RFFD' pin is provided. This output is asserted high when the module is ready to begin a new Multiply-Accumulation.
  - **RDY (Ready):** If selected, the module is generated with a Ready output, 'RDY'. 'RDY' is high for the first clock cycle when the result of an accumulation is available.
  - **COUNT:** This option determines whether the module is to have a 'COUNT' input bus to select the number of Multiply-Accumulate cycles in a complete MAC operation.
  - **COUNT Width:** Used if the module has programmable MAC counter (**COUNT** is true) and specifies the width of the 'COUNT' bus. The valid range is 1 to 32 bits.
  - **MAC Count:** The number of Multiply-Accumulate cycles in a complete MAC operation. This parameter is used if the module has a fixed MAC counter (**COUNT** is false) and 'RFFD' and/or 'RDY' output pins have been specified.
- **Accumulator Options**
  - **Accumulator Width:** The accumulator width must be greater than or equal to the **Significant Multiplier Output Bits** parameter. The maximum value permitted is 65.
  - **Accumulator Saturates:** If this option is selected, the accumulator performs saturation. Saturation is available for signed and unsigned results.
- **Output Options**
  - **Significant Multiplier Output Bits:** This parameter sets the number of significant multiplier output bits used by the accumulator. The value must be in the range 1 to (**Port A Width** + **Port B Width**).
  - **Round Multiplier Output:** This option selects rounding of the multiplier output. Rounding may be used if the number of **Significant Multiplier Output Bits** is less than the multiplier width. If selected, the 'C_IN' optional input port is not available.
  - **Significant Accumulator Output Bits:** Selects the number of significant accumulator bits to be output from the module. This parameter also sets the width of the output bus 'Q'. The allowable range is between 1 and the accumulator width.
- **Pipelining Level**
  - Selects the level of pipelining to be applied to the multiplier portion of the module. The parameter is selected from a pull-down menu. The number of pipeline stages depends on **Port B Mode** and the width of the 'B' data input as shown in Table 8 on Page 8. If the **Port B Mode** is **Constant** or **Dynamic Constant** the level will be "0" or "MAX"**.** If **Port B Mode** is **Dynamic** the level will be "0", "1" or "MAX".
- **Create RPM**
  - When this box is checked, the module is generated with the relative location attributes attached. The resulting placement of the module is a rectangular area on the device. The default operation is to create an RPM. Note that when a module is created as an RPM, it is possible that one or more of the module dimensions may exceed those of the device being targeted. If this is the case, mapping errors will occur and the mapper will fail. In this case, the module should be re-generated with the **Create RPM** checkbox unchecked.

Parameter Values in the XCO File

Names of XCO parameters and their parameter values are identical to the names and values shown in the GUI, except that the underscore character, "_," is used in place of spaces. The text in an XCO file is case insensitive.

Table 11 shows the XCO file parameters and values and summarizes the GUI defaults.

The following is an example of an XCO file:

```
CSET Port_A_Width = 8
CSET Port_B_Width = 8
CSET Port_A_Type = Signed
CSET Port_B_Type = Signed
CSET Port_B_Mode = Variable
CSET Port_B_Value = 0
CSET carry_in = False
CSET carry_out = False
CSET overflow = False
CSET Output_Hold_Registers = False
CSET Register_Inputs = False
CSET COUNT = False
CSET COUNT_Width = 1
CSET MAC_Count = 4
CSET RFFD = True
CSET RDY = True
CSET Significant_Multiplier_Output_Bits = 16
CSET Round_Multiplier_Output = False
CSET Accumulator_Width = 20
CSET Accumulator_Saturates = False
CSET Significant_Accumulator_Output_Bits = 20
CSET Pipelining_Level = 0
CSET ADD = False
```

CSET Asynchronous_Clear = True
CSET Synchronous_Clear = True
CSET CE = True
CSET CE_Override_for_SCLR = False
CSET Create_RPM = True

Latency

The total latency (number of clock cycles required to get the first output) is a function of the width of the 'B' input and the pipelining and input/output register selections. The latency of the multiplier portion of the module is shown in Table 8.

Table 8: Multiplier Latency

Port B Mode	Pipelining Level	Port B Size	Latency
Variable	0	1 to 32	0
	1	1 to 32	1
	MAX	1 and 2	1
		3 and 4	2
		5 to 8	3
		9 to 16	4
		17 to 32	5
Constant/ Dynamic	0	1 to 32	0
	MAX	1	1
		2 to 8	2
		9 to 16	3
		17 to 32	4

The latency of the accumulator, input registers and output registers is shown in Table 9. The **Register Inputs** and **Output Hold Registers** parameters define the register options for the module. The overall latency of the MAC is achieved by adding the latency from Table 8 to the latency from Table 9.

Table 9: Accumulator and I/O Latency

Register Inputs	Output Hold Registers	Latency
No	No	1
No	Yes	2
Yes	No	2
Yes	Yes	3

Performance and Size Characteristics

When running the map and par implementation tool, it is important to set a maximum period constraint on the core clock input. Table 10 illustrates the achievable performance for a selection of 'A' and 'B' port widths. This assumes the default parameter options (Table 11 on Page 9). The Virtex slice count and RPM area values provide an approximate indication of module size.

Note that the maximum operating speed has a small dependency on the seed values used in the Place and Route software.

Table 10: Performance and Size Examples

Virtex MAX Parameter Settings (A Width x B Width) (XCV300-6-PQ240)	Performance	
	Speed	Slice Count (RPM Area)
8 x 8 Maximum Pipelining	MHz (nS)	(RxC)
16x16 Maximum Pipelining	MHz (nS)	(RxC)
32x32 Maximum Pipelining	MHz (nS)	(RxC)
8x8 No Pipelining	MHz (nS)	(RxC)
16x16 No Pipelining	MHz (nS)	(RxC)
32x32 No Pipelining	MHz (nS)	(RxC)

Core Resource Utilization

Input Selection

If **Port B Mode** = **Dynamic**, care should be taken selecting the 'A' (multiplicand) and 'B' (multiplier) inputs. To reduce the number of stages and therefore the size and latency of the multiplier, connect the smaller bit size input to 'B'. However, each stage will contain a larger carry chain. Therefore, to get maximum speed performance between stages, connect the larger input size to 'B'. Generally, keep the 'B' input as small as possible.

Clear and Clock Enable Options

The module supports both synchronous and asynchronous clear inputs. When both types of clear are selected, the synchronous clear is implemented using logic in the Look Up Tables (LUTs) preceding the output register.

If the **SCLR Overrides CE** is selected, 'SCLR' will be acted upon regardless of the status of 'CE'. In this case, dedicated inputs on the flip-flop primitives are used. If not selected, 'CE' will force the synchronous control functionality to be implemented using logic in the Look Up Tables (LUTs) preceding the affected registers.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information, contact your local Xilinx sales representative, or email requests to coregen@xilinx.com.

Table 11: Default Values and XCO File Values

Parameters	XCO File Values	Default GUI Settings
component_name	ASCII text starting with the letter and based upon the following character set: a…z, 0…9 and "_"	blank
Port_A_Width	Integer in the range of 1 to 32 (unsigned) or 2 to 32 (signed)	8
Port_A_Type	One of the following key words: **Signed**, **Unsigned**, **Controlled By Pin**	Signed
Port_B_Width	Integer in the range 1 to 32 (unsigned) or 2 to 32 (signed)	8
Port_B_Type	One of the following key words: **Signed**, **Unsigned**	Signed
Port_B_Value	If **Port B Type** = **Unsigned**: Integer in the range 0 to $2^{(\text{Port B Width}) - 1}$ If **Port B Type** = **Signed**: Integer in the range $-2^{(\textbf{Port B Width} - 1)}$ to $2^{(\textbf{Port B Width} - 1)} - 1$	0
Carry_In	One of the following key words: true, false	false
Carry_Out	One of the following key words: true, false	false
Overflow	One of the following key words: true, false	false
Output_Hold_Registers	One of the following key words: true, false	false
Register_Inputs	One of the following key words: true, false	false
Asynchronous_Clear	One of the following key words: true, false	false
Synchronous_Clear	One of the following key words: true, false	true
SCLR_Overrides_CE	One of the following key words: true, false	false
ADD	One of the following key words: true, false	false
CE	One of the following key words: true, false	false
RFFD	One of the following key words: true, false	false
RDY	One of the following key words: true, false	true
COUNT	One of the following key words: true, false	false
COUNT_Width	Integer in the range 1 to 32	4
MAC_Count	Integer in the range 1 to $(2^{31} - 1)$	0
Accumulator_Width	Integer in the range **(Significant Multiplier Output Bits)** to 65	10
Accumulator_Saturates	One of the following key words: true, false	false
Significant_Multiplier_Output_Bits	Integer in the range 1 to (**Port A Width + Port B Width**)	10
Round_Multiplier_Output	One of the following key words: true, false	false
Significant_Accumulator_Output_Bits	Integer in the range 1 to (**Accumulator Width)**	10
Pipelining_Level	One of the following key words: "0", "1", "MAC"	0
Create_RPM	One of the following key words: true, false	true