



T1E1 Framer

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Product Specification



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Features

- Generates multiple frame structures
 - T1-D4 frames with 4- or 12-frame multiframes
 - T1-ESF frames with 24-frame multiframes
 - E1 frames with 16-frame CAS & CRC multiframes
- Fully compliant with CCITT Recommendation G.704 (G.706, G.732, G.733)
- Programmable Idle codes for data and signalling
- Provides support for CRC6 and CRC4 generation
- Provides bit location output signals
- Fully synchronous design

Applications

- ISDN Primary Rate Access
- Multiplexing equipment
- Satellite communications
- Digital PABX
- High speed computer links

General Description

The T1E1 Framer generates a complete T1 or E1 data stream containing a programmable Idle code in the data channels, and a programmable Idle code in the signalling bits. In addition, E1 frames can be generated with or without CRC and CAS multiframes.

Various common bit location, timeslot location and control signals are generated as follows:

- Frame Alignment Location (T1/E1)
- Data Location (T1/E1)
- Signalling Location (T1/E1)
- FAW Bit Location (T1/E1)
- A Bit Location (T1(ESF)/E1)
- CRC Bit Location (T1(ESF)/E1)

LogiCORE™ Facts	
Core Specifics	
Device Family	Virtex™, Virtex™-E, Spartan™ II
Slices Used	126
I/Os Used	87
CLKIOBs Used	1
System Clock fmax	>40MHz
Device Features Used	-
Provided with Core	
Documentation	Product Specification
Design File Formats	Targeted EDIF
Constraint Files	.ucf file
Verification Tool	ModelSim v5.4 Demonstration VHDL and Verilog test benches supplied
Schematic Symbols	-
Evaluation Model	Post-layout .vhd, .veri
Reference designs & application notes	-
Additional Items	-
Design Tool Requirements	
Xilinx Core Tools	Design Manager 3.2
Entry/Verification Tool	FPGA Express 3.4 ModelSim v5.4
Support	
Support provided by Xilinx	

- CRC Done Location (T1(ESF)/E1)
- M Bit Location (T1(ESF))
- F Bit Location (T1)
- S Bit Location (T1(D4))
- E Bit Location (E1)
- Sa Bit Location (E1)
- X Bit Location (E1(CAS))
- Y Bit Location (E1(CAS))
- CRC MF Bit Location (E1(CRC))
- CAS MF Bit Location (E1(CAS))

These allow additional circuitry to be added with minimal effort.

Delayed versions of most signals are also generated to allow efficient connections to blocks further down stream. These delayed output signals can be configured to occur an integer number of data bit cycles after the main signals, as set by the Output_Delay input.

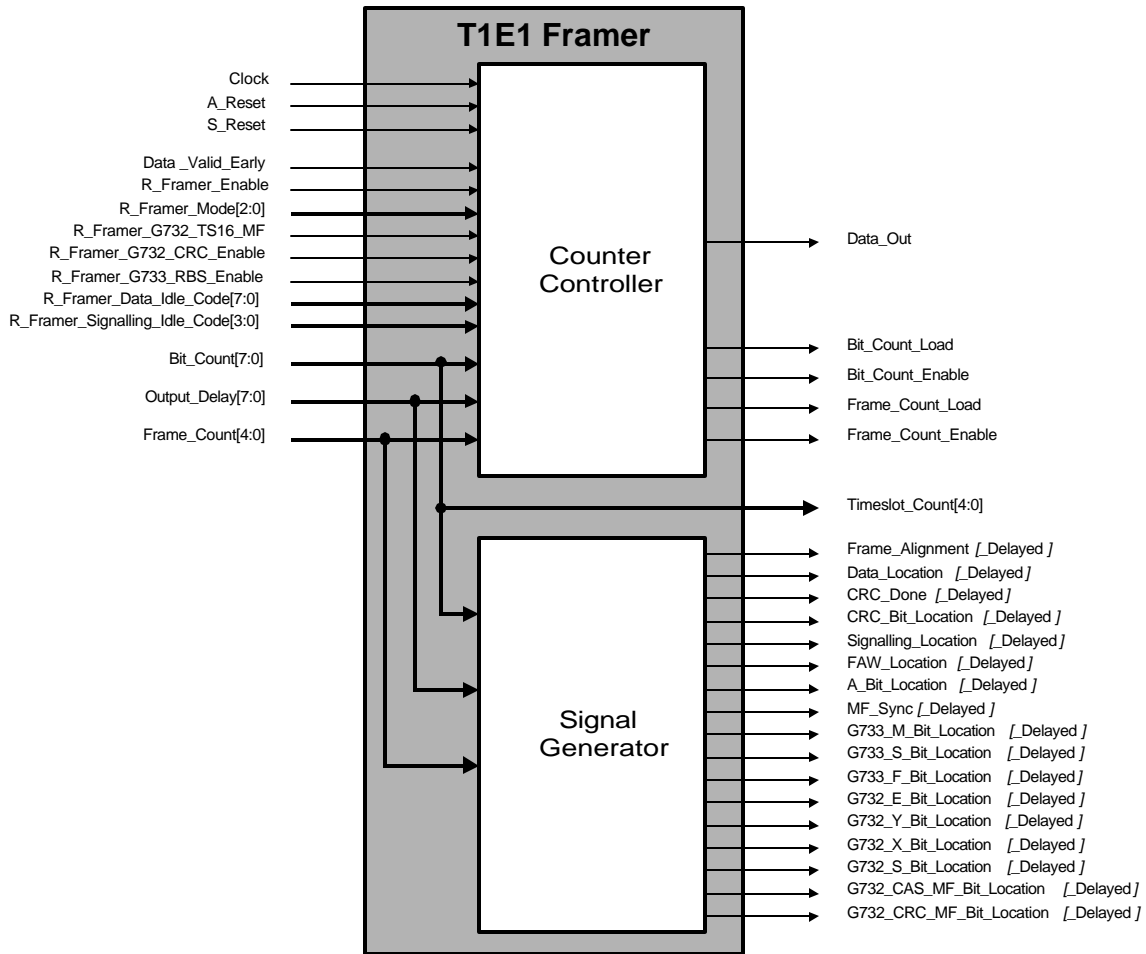


Figure 1: Core Schematic

Functional Description

The T1E1 Framer is comprised of two main blocks, a Controller block and a Signal Generator block.

The Controller block drives Bit and Frame counters to generate raw T1 or E1 multiframes. Into this structure, it places all the required framing bits and accessory bits. Timeslots are filled with the given Data Idle code: Signalling bits are filled with the given Signalling Idle code.

The resultant T1 or E1 multiframe is a valid data stream, but the CRC bits will be incorrect. If a CRC is required, a CRC generator must be added after the frame to calculate and insert the correct CRC bits.

The Signal Generator is driven by the same Bit and Frame counters that the Controller block uses. The Signal Generator outputs are unlatched simple asynchronous decodes of the Bit and Frame counter values. These counters are decoded to produce the Bit Location signals. A delayed set of Bit Location signals is also produced with all the signals delayed by an amount set through the Output_Delay input.

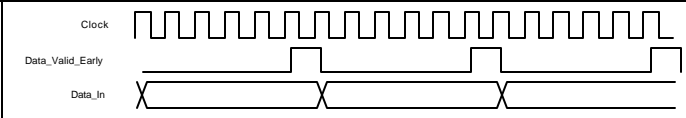
The Bit and Frame counters both count from zero up to the appropriate terminal count. For T1 systems, the Frame bit is decoded at bit count 192. This keeps the bit counts of the data timeslots the same for both T1 and E1 systems. However, this means that for each frame of a T1 system, the Frame Bit for that frame occurs as the last bit of the *previous* frame. You should also note that this numbering scheme does not match the CCITT numbering method.

Pinout

The following table summarizes the signal functions. Unless otherwise stated all signals are active high and bit 0 is the least significant bit.

Please Note: (i) The numbering scheme represents the value of the Bit_Count[7:0] and the Frame_Count[4:0] signals and thus differs from the CCITT system.

(ii) The Frame Bits of T1 systems are decoded as Bit_Count 192. This keeps the bit counts for the timeslot data the same for both T1 and E1 systems. It also means that the Frame Bit for a particular frame occurs as the last bit of the previous frame, making the Frame_Count for the Frame bit one more than that for the other bits in the frame.

Signal	Signal Direction	Description
Clock	I	Synchronous System Clock. This must have a minimum frequency of 1 times the bit rate clock. eg $\geq 1.544\text{MHz}$ or 2.048MHz .
A_Reset	I	Asynchronous Global Reset (Active Low).
S_Reset	I	Synchronous Global Reset (Active Low).
Data_Valid_Early	I	
Bit_Count[7:0]	I	Bit number within the current frame. This count changes at the data bit rate. It counts between: 0 - 192 for T1 systems 0 - 255 for E1 systems. For T1 systems, the Frame Bit occurs at bit count 192.
Bit_Count_Load	O	When high, causes the Bit counter to perform a parallel load of zero, as the load data inputs of the counter should be tied to 0.
Bit_Count_Enable	O	When high, causes the Bit counter to count.
Frame_Count[4:0]	I	Frame number within the current multiframe. This count changes at the frame rate. It counts between 0 - 23 for T1 ESF systems 0 - 11 for T1 D4 12-Frame systems 0 - 11 for T1 D4 4-Frame systems (the multiframe is repeated 3 times) 0 - 15 for E1 systems
Frame_Count_Load	O	When high, causes the Frame counter to perform a parallel load of zero, as the load data inputs of the counter should be tied to 0.
Frame_Count_Enable	O	When high, causes the Frame counter to count.
Output_Delay[7:0]	I	Required output delay as an integer number of data bit cycles. Note: Limited to 192 for T1 systems (R_Framer_Modes 1, 3 and 4) and to 255 for E1 systems (R_Framer_Mode 2).
Data_Out	O	The generated T1 or E1 data stream.
R_Framer_Enable	I	When high, enables the Framer. When low, the framer won't count or produce output.
R_Framer_Mode[2:0]	I	Sets the mode of the framer as follows: 0 0 0 disabled 0 0 1 T1 D4 4-frame mode 0 1 0 E1 mode 0 1 1 T1 D4 12-frame mode 1 0 0 T1 ESF mode

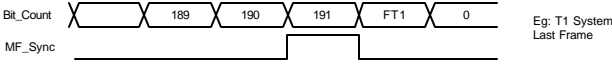
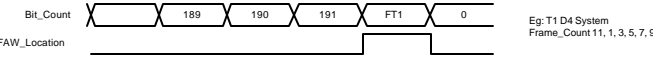
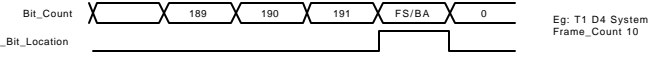
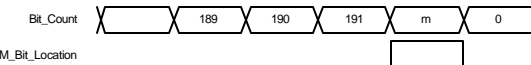
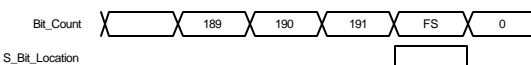
T1E1 Framer

Signal	Signal Direction	Description
R_Framer_G732_TS16_MF	I	When high, inserts a CAS multiframe in TS16 frame 0. When low, Signalling Idle nibbles are inserted in TS16 of all frames.
R_Framer_G733_RBS_Enable	I	Robbed Bit Signalling Enable for T1 systems. When high, enables the insertion on signalling frames in T1 systems of the Signalling Idle code as Robbed Bit Signalling into the LSB of the Data Idle code.
R_Framer_G732_CRC_Enable	I	CRC Enable for E1 systems. When high, puts a CRC word in bit 0 of TS0 of all frames (except for E bits). When low, forces bit 0 to a 1 to disable CRC.
R_Framer_Data_Idle_Code[7:0]	I	Data value which will be placed in all data timeslots. D7 is the first bit transmitted in the timeslot. The bit overwritten by robbed bit signalling in a T1 system will be D0.
R_Framer_Signalling_Idle_Code[3:0]	I	Data value which will be placed in all signalling timeslots. D3 corresponds to channel A and will be used in frame 5 of a T1 system; D2 corresponds to channel B and will be used in frame 9; and so on.
Timeslot_Count[4:0]	O	Timeslot number within the current frame. It is basically the top 5 bits of the bit count. For an E1 system, the first 8 bits of each frame is timeslot 0 and the FAW signalling occurs in timeslot 16.

Timing Signals

Note: The T1E1 Framer also produces versions of these signals that are delayed by an integer number of data bit cycles, set through the Output_Delay input. The amount of delay is limited to 192 for T1 frames (R_Framer_Modes 1, 3 and 4) and 255 for E1 frames (R_Framer_Mode 2).

Signal	Signal Direction	Description
Frame_Alignment	O	<p>Delimits the Frame structure by highlighting the last bit in a frame with respect to the Bit_Count. For T1 systems, this is on bit count 191; for E1 systems, it is on bit count 255.</p>
Data_Location	O	<p>Delimits each octet of data by highlighting the last bit of each octet with respect to the bit count.</p>
CRC_Done	O	Delimits the CRC data frame by highlighting the last bit in it. For T1 ESF systems, this is bit 191 of frame 23. For E1 systems, it is bit 255 of frames 7 and 15.
CRC_Bit_Location	O	<p>Indicates the position of the CRC bits. For T1 systems, this is on the Frame Bit of frames 1,5,9,13,17&21. For E1 systems, it is on bit 1 of timeslot 0 in even frames.</p>

Signal	Signal Direction	Description
Signalling_Location	O	Indicates the position of the Signalling bits. For T1 systems, this is on the last bit of each timeslot in frames 5,11,17 & 23. For E1 systems, it occurs during timeslot 16 (bit count 128 - 135).
MF_Sync	O	Indicates the position of the last bit in a multiframe. For T1 systems, this is on bit 191 of the last frame: for E1 systems, it is on bit 255 of frame count 15. 
FAW_Location	O	Indicates the position of the Frame Alignment Word Bit. For T1 ESF systems, this is on bit count 192 of frames 2,6,10,14,18&22. For T1 D4 systems, it is on bit count 192 of frames 11,1,3,5,7& 9. For E1 systems, it is on bit counts 1-7 of even frames (0, 2, ...). 
A_Bit_Location	O	Indicates the position of the A Bit. For T1 D4 systems, this is on bit count 192 of frame count 10. For E1 systems, it is on bit count 2 of odd frames. 
G733_M_Bit_Location	O	Indicates the position of the M or DL bits in T1 ESF systems. This is on bit count 192 of frame counts 23,1,3,5,7,9,11,13,15,17,19&21. 
G733_S_Bit_Location	O	Indicates the position of the FS signalling bits (D4 mode only). This is on bit count 192 of frames 0, 2, 4, 6, 8 & 10. 
G733_F_Bit_Location	O	Indicates the position of all the F bits (bit 192) in all frames of a T1 ESF systems.
G732_S_Bit_Location	O	Indicates the position of the S bits in E1 mode. These are on bits 3 to 7 of all odd frames.
G732_E_Bit_Location	O	Indicates the position of the E bits in E1 mode. These are on bit count 0 of frames 13 and 15.
G732_Y_Bit_Location	O	Indicates the position of the Y bits in E1 mode. This is on bit count 133 of CAS Multiframe Count 0.
G732_X_Bit_Location	O	Indicates the position of the X bits in E1 mode. These are on bit counts 132, 134 & 135 of CAS Multiframe Count 0.
G732_CAS_MF_Bit_Location	O	Indicates the position of the CAS multiframe word bits in E1 mode. This is on bits 128 - 131 of of CAS Multiframe Count 0.
G732_CRC_MF_Bit_Location	O	Indicates the position of the CRC multiframe bits in E1 mode. This is on bit 0 of frames 1, 3, 5, 7, 9 & 11.

Frame Contents

The generated frames have the following contents:

T1 D4 Frame Structure (4 Frame)

Bit Count	F_Bit 192	TS0 0 7	TS1 8 15	TS2 16 23	TS3 24 31	TS4 32 39	TS5 40 47	TS6 48 55	TS7 56 63
Frame 0	FT 1	Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 1	FS 0	Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 2	FT 0	Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 3	FS 0	Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Bit Count		TS8 64 71	TS9 72 79	TS10 80 87	TS11 88 95	TS12 96 103	TS13 104 111	TS14 112 119	TS15 120 127
Frame 0		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 1		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 2		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 3		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Bit Count		TS16 128 135	TS17 136 143	TS18 144 151	TS19 152 159	TS20 160 167	TS21 168 175	TS22 176 183	TS23 184 191
Frame 0		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 1		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 2		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle
Frame 3		Idle	Idle	Idle	Idle	Idle	Idle	Idle	Idle

FT - Frame Alignment Word bit FS - Signalling Frame Alignment (NOT to CCITT Numbering Scheme)

T1 D4 Frame Structure (12 Frame)

Bit Count	F_Bit 192	TS0 0 7	TS1 8 15	TS2 16 23	TS3 24 31	TS4 32 39	TS5 40 47	TS6 48 55	TS7 56 63
Frame 0	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 1	FS 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 2	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 3	FS 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 4	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 5	FS 1	CH1 A	CH2 A	CH3 A	CH4 A	CH5 A	CH6 A	CH7 A	CH8 A
Frame 6	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 7	FS 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 8	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 9	FS 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 10	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 11	FS/BA	CH1 B	CH2 B	CH3 B	CH4 B	CH5 B	CH6 B	CH7 B	CH8 B
Bit Count		TS8 64 71	TS9 72 79	TS10 80 87	TS11 88 95	TS12 96 103	TS13 104 111	TS14 112 119	TS15 120 127
Frame 0		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 1		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 2		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 3		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 4		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 5		CH9 A	CH10 A	CH11 A	CH12 A	CH13 A	CH14 A	CH15 A	CH16 A
Frame 6		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 7		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 8		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 9		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 10		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 11		CH9 B	CH10 B	CH11 B	CH12 B	CH13 B	CH14 B	CH15 B	CH16 B
Bit Count		TS16 128 135	TS17 136 143	TS18 144 151	TS19 152 159	TS20 160 167	TS21 168 175	TS22 176 183	TS23 184 191
Frame 0		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 1		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 2		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 3		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 4		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 5		CH17 A	CH18 A	CH19 A	CH20 A	CH21 A	CH22 A	CH23 A	CH24 A
Frame 6		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 7		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 8		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 9		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 10		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 11		CH17 B	CH18 B	CH19 B	CH20 B	CH21 B	CH22 B	CH23 B	CH24 B

FT - Frame Alignment Word bit FS - Signalling Frame Alignment FS/BA = 0 for FS, 1 for Back Alarm
 A, B - Robbed Bit Signalling bits (NOT to CCITT Numbering Scheme)

T1 ESF Frame Structure

Bit Count	F_Bit 192	TS0 0 7	TS1 8 15	TS2 16 23	TS3 24 31	TS4 32 39	TS5 40 47	TS6 48 55	TS7 56 63
Frame 0	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 1	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 2	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 3	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 4	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 5	CRC	CH1 A	CH2 A	CH3 A	CH4 A	CH5 A	CH6 A	CH7 A	CH8 A
Frame 6	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 7	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 8	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 9	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 10	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 11	FAW '1'	CH1 B	CH2 B	CH3 B	CH4 B	CH5 B	CH6 B	CH7 B	CH8 B
Frame 12	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 13	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 14	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 15	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 16	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 17	CRC	CH1 C	CH2 C	CH3 C	CH4 C	CH5 C	CH6 C	CH7 C	CH8 C
Frame 18	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 19	FAW '1'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 20	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 21	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 22	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 23	FAW '1'	CH1 D	CH2 D	CH3 D	CH4 D	CH5 D	CH6 D	CH7 D	CH8 D
Bit Count	TS8 64 71	TS9 72 79	TS10 80 87	TS11 88 95	TS12 96 103	TS13 104 111	TS14 112 119	TS15 120 127	
Frame 0	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 1	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 3	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 4	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 5	CH9 A	CH10 A	CH11 A	CH12 A	CH13 A	CH14 A	CH15 A	CH16 A	
Frame 6	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 7	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 8	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 9	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 10	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 11	CH9 B	CH10 B	CH11 B	CH12 B	CH13 B	CH14 B	CH15 B	CH16 B	
Frame 12	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 13	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 14	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 15	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 16	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 17	CH9 C	CH10 C	CH11 C	CH12 C	CH13 C	CH14 C	CH15 C	CH16 C	
Frame 18	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 19	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 20	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 21	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 22	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	
Frame 23	CH9 D	CH10 D	CH11 D	CH12 D	CH13 D	CH14 D	CH15 D	CH16 D	
Bit Count	TS16 128 135	TS17 136 143	TS18 144 151	TS19 152 159	TS20 160 167	TS21 168 175	TS22 176 183	TS23 184 191	
Frame 0	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 1	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 2	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 4	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 5	CH17 A	CH18 A	CH19 A	CH20 A	CH21 A	CH22 A	CH23 A	CH24 A	
Frame 6	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 7	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 8	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 9	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 10	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 11	CH17 B	CH18 B	CH19 B	CH20 B	CH21 B	CH22 B	CH23 B	CH24 B	
Frame 12	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 13	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 14	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 15	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 16	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 17	CH17 C	CH18 C	CH19 C	CH20 C	CH21 C	CH22 C	CH23 C	CH24 C	
Frame 18	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 19	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 20	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 21	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 22	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	
Frame 23	CH17 D	CH18 D	CH19 D	CH20 D	CH21 D	CH22 D	CH23 D	CH24 D	

DL - Data Link bit CRC - CRC bit FAW - Frame Alignment Word bit A,B,C,D - Robbed Bit Signalling bits (NOT to CCITT Numbering Scheme)

E1 Frame Structure (12 Frame)

Bit Count	TS0 0 7	TS1 8 15	TS2 16 23		TS16 128 135	TS17 136 143	TS18 144 151		TS31 247 255
Frame 0	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	0000 1011 (MMMM XYXX)	Idle	Idle	...	Idle
Frame 1	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 2	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 3	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 4	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 5	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 6	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 7	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 8	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 9	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 10	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 11	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 12	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 13	0 1011111 (E 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 14	0 0011011 (Cd FFFFFFFF)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle
Frame 15	0 1011111 (Cm 1ASSSS)	Idle	Idle	...	Signalling Idle	Idle	Idle	...	Idle

Ft - Frame Alignment Word bit Cm - CRC4 Multiframe Alignment bits Cd - CRC4 data bits E - CRC4 Error bits A - Remote Alarm bit S - Sa Spare bit X - Spare bit Y - Remote Alarm M - CAS Multiframe Alignment bits Note that Cm and Cd bits are set to '1' if CRC4 is not used and that TS16 of Frame 0 is set to Signalling Idle is CAS is not used (NOT to CCITT Numbering Scheme)

Related Information**Copyright Information**

The T1E1 Framer module and associated files are proprietary, confidential information of Mentor Graphics Corporation. It is distributed by Xilinx, Inc. under license from Mentor Graphics Corporation and may only be used, copied and/or disclosed according to the terms of a valid license agreement with Xilinx, Inc.

Assumed Knowledge

It is assumed that the user is familiar with all aspects of HDL-based design flows from component instantiation in either Verilog or VHDL (and all other aspects of Verilog/VHDL syntax) to HDL simulation using test benches and script-based synthesis.

It is also assumed that the user is familiar with the relevant telecommunication standards.

Installation Guidelines

To install the T1E1 Framer design into the Xilinx Core Generator, copy the whole of the delivered directory structure to your \$XILINX/coregen/ip/xilinx directory.

Then call up Core Generator and ensure that the Mentor Graphics T1E1 Framer module is listed among the Communications & Networking/Telecommunications modules.

This will give you a \$XILINX/coregen/ip/xilinx/t1e1_framer/com/xilinx/ip/t1e1_framer directory (hereafter referred to as your T1E1 Framer product directory). The detailed structure of the delivered files is described in the readme text file included in your T1E1 Framer product directory.

Note: While the cores based on Xilinx components can be generated in the same area as the source files, you are strongly recommended to create your project directory in a separate location. Similarly, if you want to use the supplied Chip Example, you should copy them out of the Core Generator tree before working on them.

Component Instantiation

The T1E1 Framer module may be included in user designs by instancing the module as a component.

Example declarations showing all the I/O port names are included in the templates provided in the virtex/templates directory within your T1E1 Framer product directory. The example VHDL declaration is provided in the

t1e1_framer.vho file. The example Verilog declaration is provided in the t1e1_framer.veo file.

Compilation Guidelines

An example compilation script is provided as the file xilrun.cmd (for Unix)/xilrun.bat (for DOS) in the virtex/chip_example/xilinx_run directory within your T1E1 Framer product directory. These example compilation scripts process the example chip-level EDIF netlist provided alongside the xilrun.cmd and xilrun.bat files for a range of Xilinx implementation tools (ngdbuild, map and par) and the 'trce' timing report generation tool.

Synthesis Guidelines

For synthesis, the core should be declared as a 'black box' which will then be incorporated into your design during the translation stage of the synthesis process (provided the relevant netlist file can be found on the search path).

An unpadding EDIF description of the core may be found as an .edn file in the virtex/implement directory within your T1E1 Framer product directory. Use this netlist along with the appropriate snippets from the t1e1_framer.vho/.veo files to integrate the T1E1 Framer into your design.

An example .ucf constraints file may be found in the virtex/chip_example/xilinx_run directory.

Simulation Guidelines

HDL test benches for use with the VHDL/Verilog descriptions of the core are provided, together with functional and post-layout simulation models and example compile-and-simulate scripts for use under ModelSim.

The functional simulation models are provided in the virtex/func_sim directory. Use the code snippets in the .vho/.veo template file to integrate these functional models into the functional simulation model for your design.

The post-layout simulation models, test benches and compile-and-simulate scripts are provided in the virtex/chip_example/verilog|vhdl directory, together with SDF files containing timing information. Each of these directories contains a modelsim.do file which runs the simulation test bench under ModelSim.

Test Bench and Test Data

The provided test benches do the following:

- Instantiate the core
- Generate input test vectors and apply them to the core
- Compare the output with expected 'golden' results
- Test the operation of reset and confirm that the expected values are selected
- Flag any mismatch between the actual output and the expected result of the simulation

Libraries

For simulation, it is assumed that the Xilinx-supplied 'simprims' and 'unisims' libraries have been compiled for use under ModelSim and stored in the \$XILINX/verilog|vhdl|mti directory. Using the Xilinx-supplied Perl scripts will cause the correct libraries to be compiled.

Ordering Information

Xilinx LogiCORE modules are provided under Xilinx LogiCORE standard license agreement. For price and availability information, please contact your local Xilinx Sales Representative.