32 Channel ADPCM V1.2

LogiCORE™

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ISS

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Features

- Optimized for Virtex™, Virtex™-E, Spartan™-II
- Up to 32 duplex channel encoding/decoding.
  or
  Up to 64 channel encoding and/or decoding.
- On-line configurable for different compression rates, PCM laws and standards.
- Coding (encode or decode) for one data sample completed in 16 clock cycles.
- Can work in both burst and continuous modes.
- Multiplications mapped onto a single multiplier for compact implementation.
- On-chip RAM used, via general RAM interface (4x70x32 bits).
- Conforms fully to ITU test vectors

General Description

ITU standard G.721, G.722 and G.726 specifies the requirements for the conversion of a 64 kbit/s pulse code modulation (PCM) channel to and from a 40, 32, 24 and 16 kbit/s channel, using an Adaptive Differential Pulse Code Modulation (ADPCM) transcoding technique.

The ADPCM core is compliant with the G.726 standard and supports multichannel encoding/decoding or duplex coding. The PCM input channel multiplexing and serial to parallel conversion circuitry may be added to suit the target system as required. The core is on-line configurable in terms of compression rate and PCM law. It allows 'on-the-fly' selection of PCM/uniform PCM input/output. It has been tested and verified to be fully compliant using the ITU standard test vectors.

Functional Description

Clock

All registers in the ADPCM core operate on the rising edge of the input clock CLK. Data inputs are latched on the clock rising edge and outputs are generated on the clock rising edge..

LogiCORE™ Facts

Core Specifics	
Device Family	Virtex™, Virtex™-E, Spartan™-II
Slices Used	1728
IOBs Used	61
CLKIOBs Used	1
System Clock fmax	>15MHz
Device Features Used	5 x Block RAMs
Provided with Core	
Documentation	Datasheet and User Guide
Design File Formats	Targeted EDIF
Constraint Files	ADPCM32.ucf
Verification Tool	Modelsim v5.3 VHDL and Verilog testbenches
Schematic Symbols	ADPCM32.xfs
Evaluation Model	post layout vhd, veri, edf
Design Tool Requirements	
Xilinx Core Tools	Design Manager 2.1
Entry/Verification Tool	FPGA Express 3.3 Modelsim v 5.3
Support	
Support:　www.support.xilinx.com	

Operating Mode

The ADPCM core has two operating modes, namely:

1. **Duplex mode**. In the duplex mode, the core supports up to 32 duplex channel encoding/decoding.

2. **Flexible mode**. In the flexible mode, the core allows a mixture of up to 64 channel encoding or decoding. The mode is selectable by a static input signal MODE.

Global Reset and Configuration

The global reset resets all the channels and configures them with the same compression rate and PCM law. A global reset is activated when the asynchronous global reset input, RST, is asserted. The core reset process starts on

the first rising clock edge after RST has been de-asserted, and continues for 128 cycles. The core busy output flag BSY is set to '1' during the reset period. Configuration of the core is performed using the CFG input. The configuration word CFG is sampled on the second rising clock edge after RST is de-asserted.

Channel Reset and Configuration

The channel reset resets a duplex channel or an encoding/decoding channel and configures for that channel with a specific compression rate and PCM law, depending on the operating mode. A channel reset is activated when the synchronous channel reset input CLR is asserted for at least one rising clock edge. The channel reset process starts on the first rising clock edge after CLR has been de-asserted, and continues for 8 cycles in the duplex mode, or 4 cycles in the flexible mode. In the duplex mode, a channel reset resets and configures both the encoding and decoding operation. In the flexible mode, a channel reset resets and configures the encoding or decoding operation. The core busy output flag BSY is set to '1' during the channel reset period. Configuration of the core is performed using the CFG inputs. The configuration word CFG is sampled on the rising clock edge when CLR is asserted.

Data Formats

8-bit PCM, 14-bit μ-law or 13-bit A-law two's complement uniform PCM input data is encoded to 2, 3, 4 or 5-bit ADPCM format and vice-versa.

Configuration Word Descriptions

Operation of the ADPCM core is controlled via the configuration control word input CFG(7:0). The function of each of the bits is summarized in the I/O description table and is described in detail below. It is noted that CFG[7:4] is only used in the duplex mode and specifies the law and compression rate for encoding.

CFG(7) selects either A law law (CFG(7)=1), or μ law (CFG(7)=0) for encoding in the duplex mode
CFG(6) controls whether even bit inversion on the 8 bit PCM input data is performed for A law encoding operations. Even bit inversion is performed when CFG(6) is '1'.
CFG(5:4) controls the number of bits in the ADPCM output word when encoding in the duplex mode.
CFG(3) selects either A law (CFG(3)=1), or μ law (CFG(3)=0) for decoding in the duplex mode, or encoding/decoding in the flexible mode.
CFG(2) controls whether even bit inversion is performed for A law decoding operations in the duplex mode, or encoding/decoding in the flexiblemode. Even bit inversion on the 8-bit PCM input data or the 8 PCM output data is performed when CFG(2) is '1'.
CFG(1:0) controls the number of bits in the ADPCM output word when encoding in the duplex mode or the

number of bits in the ADPCM input word and the ADPCM output word in the flexible mode. The various options are detailed in Table 2 below.

Table 1: Compression Rate Settings

CFG(1) or CFG(5)	CFG(0) or CFG(4)	ADPCM word length	ADPCM data rate (kpbs)
0	0	2	16
0	1	3	24
1	0	4	32
1	1	5	40

Encoding/Decoding

Coding (encoding or decoding) for one data sample is completed in 16 clock cycles. A memory block of 4*70*32 bits is required by the core for each coding operation (one duplex channel coding is regarded as being two channel coding inside the core). This RAM block is implemented on-chip.

Encode/Decode Control (DSS and EDC)

The input select signal EDC defines whether the core performs an encoding or decoding operation. When EDC is high, the core performs encoding and the input S is taken when data strobe signal (DSS) is active high. When EDC is low the core will decode, and the input ID is also taken when DSS is active high. The ADPCM core requires 16 clock cycles to complete an encoding or decoding operation for one sample data and the output indicator BSY is de-asserted after the rising edge of the 16th cycle. DSS can then be asserted after the rising edge of CLK to start the next operation and EDC defines the next operation as an encoding or decoding operation.

Channel Selection

The CHN input specifies the channel with which the input data is associated when the core is performing a coding operation, or with which the CFG word is applied when the core is performing channel reset. In the duplex mode, one channel coding includes both the encoding and decoding operations and the channel number is specified by the top 5 bits of CHN (the LSB is simply ignored by the core). In the flexible mode, one channel coding is either encoding or decoding and the channel number is fully specified by CHN. This CHN input is sampled on the cycle when BSY is low. CHN is also sampled when the core is being reset for an individual channel , i.e., when the channel reset signal CLR is active.

Pinout

A representative symbol, with the signal names, is shown in Figure 1 and described in Table 2. Unless otherwise

stated all signals are active high and bit(0) is the least significant bit..

Table 2: Core Signal Pinout

Signal	I/O	Width	Description
S	I	14	Input word for encoding. Uniform PCM input uses all 14 bits (13:0 μ-law) or 13 bits (13:1 A-Law). PCM input uses 8 bits, S(7:0)
ID	I	5	ADPCM input word ID(4) : bit no.1 the polarity ID(4:3) : 2 bit ADPCM word ID(4:2) : 3 bit ADPCM word ID(4:1) : 4 bit ADPCM word ID(4:0) : 5 bit ADPCM word
CFG	I	8	Configuration word CFG(7:4) for duplex mode only CFG(7) : Encoding law: 1 = A law; 0 = μ law CFG(6) : Encoding even bit inversion (A law): 1 = inverted, 0 = not inverted CFG(5:4) : Compression rate control. See Table 1 CFG(3) : Encoding/Decoding law: 1 = A law; 0 = μ law (A law) CFG(2) : Encoding/Decoding even bit inversion (A law) : 1 = inverted, 0 = not inverted CFG(1:0) : Compression rate control. See Table 1
EDC	I	1	Select encode or decode operation, 1: encoder, 0 : decoder
DSS	I	1	Data strobe signal, high active
PCM	I	1	PCM or uniform PCM control signal
CHN	I	6	Channel selection input signal
CLR	I	1	Synchronous channel reset input
RST	I	1	Global reset and configuration signals
CLK	I	1	Clock input – rising edge active
MODE	I	1	Operating mode control, static signal
I	O	5	ADPCM output word. I(4) : bit no.1 the polarity I(4:3) : 2 bit ADPCM output I(4:2) : 3 bit ADPCM output I(4:1) : 4 bit ADPCM output I(4:0) : 5 bit ADPCM output
SD	O	14	PCM output word. Uniform PCM uses all 14 bits (μ law) or 13 bits, S(13:1) (A law). PCM uses 8 bits, S(7:0).

Table 2: Core Signal Pinout

Signal	I/O	Width	Description
BSY	O	1	Busy indicator
ESI	O	1	Encoding status indicator
DSI	O	1	Decoding status indicator
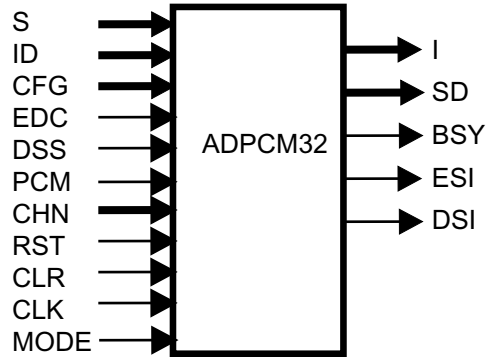
Figure 1: Core Schematic Symbol

HDL Entity Definition

The HDL entity/module declaration for the core is included with the deliverables. This shows the generic parameters that may be specified for the function, the default values if none are specified, and the I/O port names and allowable values. The module may be included in a user design by instancing the module as a component. A VHDL component declaration for the core is provided in the ADPCM32.vho file and a Verilog module declaration ADPCM32.veo in the /net/ directory located at $xilinx/core-gen/ip/xilinx/<modulename_vir>/com/xilinx/ip/<modulename_vir>/<product_family>/net.

G.721 Compatible Operation

G.721 ADPCM requires 32kbps operation, hence the core is set for G.726 mode, and 32kbps operation selected, CFG(1:0) {CFG(5:4) for Duplex mode} = 10.

G.723 Compatible Operation

G.723 ADPCM requires 24 and 40kbps operation, hence the core is set for G.726 mode, and either 24kbps, CFG(1:0) {CFG(5:4) for Duplex mode} =01, or 40kbps, CFG(1:0) {CFG(5:4) for Duplex mode} =11 is selected.

Timing Diagrams

The following timing diagrams (Figures 2, 3, 4 and 5) provide only the functional timing for the ADPCM core as the actual timings are dependent on the target implementation technology.
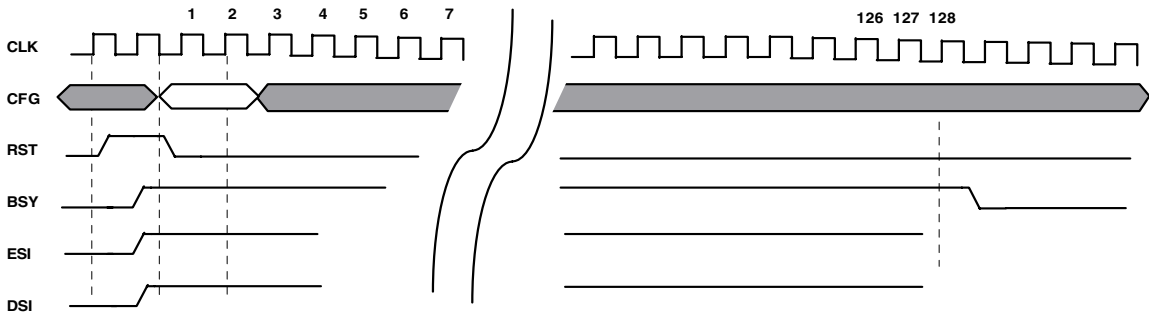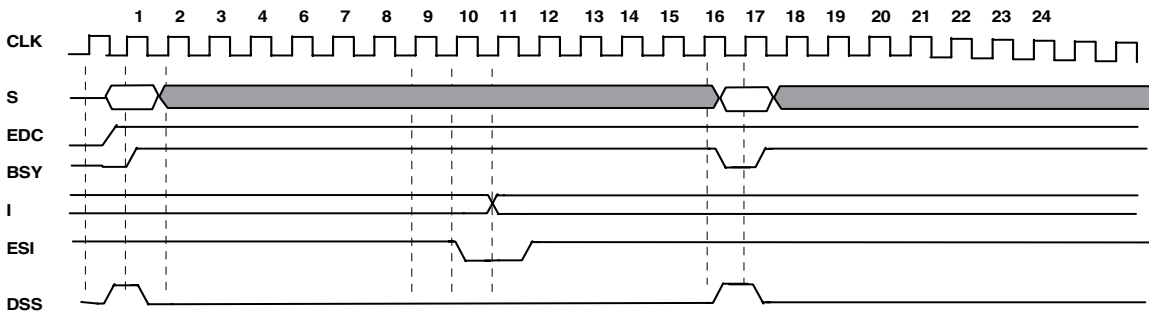
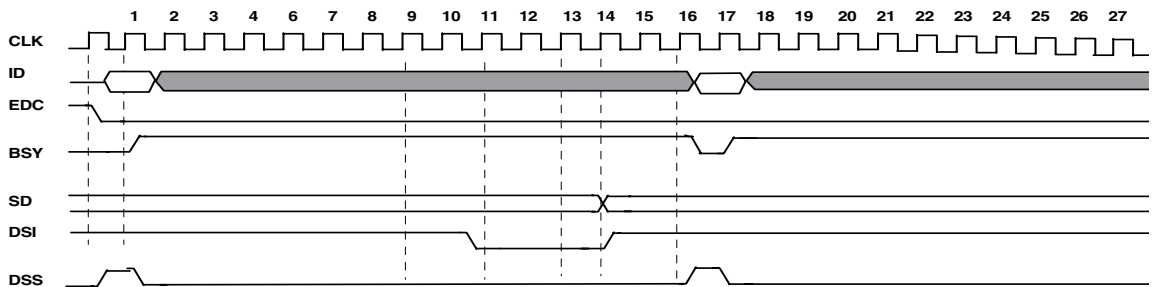**Figure 2: Reset Timing**

Figure 3: Encode Timing

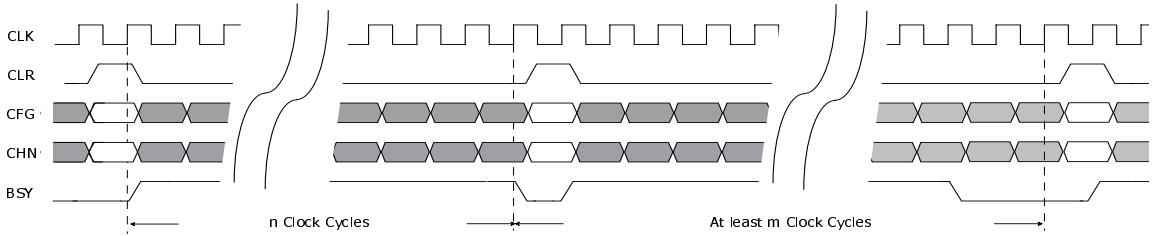**Figure 4: Decode Timing**

Note: In duplex mode n =8 and m =9. In flexible mode n = 4 and m =5.

Figure 5:   Duplex/Flexible Channel Reset

Recommended Experience

It is assumed that the user is familiar with HDL based design flows, including VHDL/Verilog language and syntax, component instantiation, synthesis based around the use of scripts, and HDL simulation using testbenches.

It is also assumed the user is familiar with ADPCM speech coding, specifically as described in ITU Q.726 recommendation Adaptive Differential Pulse Code Modulation. Further reading and reference material may be obtained by contacting:

International Telecommunications Union
Place des Nations
CH-1211Geneve 20
Switzerland

Phone: +41 22 730 51 11

Fax: +41 22 733 72 56

Related Information

Installation Guidelines

In order to install the delivered files into the users CoreGenerator tool integrated into Xilinx design flows, the user should follow installation instructions contained in the readme text file provided.

Libraries

The included modelsim.do file constructs the libraries required for simulation. It should be executed from within the /verif directory located at $xilinx/coregen/ip/xilinx/<modulename_vir>/com/xilinx/ip/<modulename_vir>/<product_family>/verif. It also requires that the simulation files remain organized in the delivered directory structure.

Component Instantiation

To use the ADPCM core the 'ADPCM32' component must be instantiated into the design file. This component defini-tion may be found in the "/net/ADPCM32.vho" and "/net/ADPCM32.veo" files located at $xilinx/coregen/ip/xilinx/<modulename_vir>/com/xilinx/ip/<modulename_vir>/<product_family>/net.

Simulation Guidelines

Testbenches, together with a set of test utilities, or tools, are provided as part of the core deliverables. A modelsim script, (/verif/modelsim.do) is also provided at $xilinx/coregen/ip/xilinx/<modulename_vir>/com/xilinx/ip/<modulename_vir>/<product_family>/verif.

Testbench and Test Data

The testbench does the following:

> instantiates the core
> reads the input test vectors from file and applies to the module
> generates reset and clock
> reads expected results from the file
> automatically checks the actual result from the module against the expected values
> flags any mismatch between the actual outputs and the expected results during simulation

The configuration of the testbenches is illustrated in Figure 6.
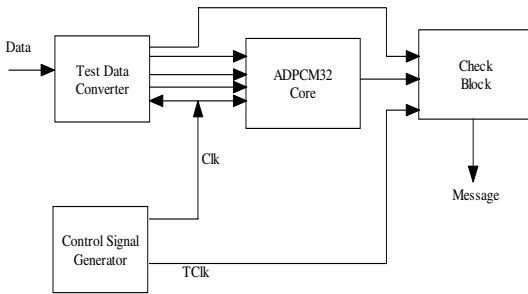
Figure 6: Architecture of ADPCM32 Testbench

The files from which the input test vectors and the expected result vectors are read are located in the '/verif/' directory. A link in the test directory to the directory above, i.e. the ADPCM top level directory must be included to enable the testbenches to locate the test data files.

The included test vectors were generated from the set of ITU standard G.726 standard inputs. The complete set of test vectors are available from:

International Telecommunications Union
Place des Nations
CH-1211Geneve 20
Switzerland

Phone: +41 22 730 51 11

Fax: +41 22 733 72 56

ITU Recommendation G.726: 40, 32, 24, 16 kbit/s Adaptive Differential Pulse Code Modulation (ADPCM).

Ordering Information

Xilinx LogiCORE modules are provided under Xilinx Logi-CORE standard license agreement. For price and availability information, please contact your local Xilinx Sales Representative.