Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

DC Specifications

All DC numbers are Preliminary for Commercial and Industrial devices, except the I_{CCINTQ} numbers for the XC2S15 and XC2S30 devices (DC Characteristics Over Operating Conditions, page 2) which are Advance.

Absolute Maximum Ratings(1)

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND(2)		–0.5	3.0	V
V_{CCO}	Supply voltage relative to GND(2)		–0.5	4.0	V
V_{REF}	Input reference voltage		–0.5	3.6	V
V_{IN}	Input voltage relative to GND(3)	5V Tolerant I/O(4)	–0.5	5.5	V
		No 5V Tolerance(5)	–0.5	V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O(4)	–0.5	5.5	V
		No 5V Tolerance(5)	–0.5	V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65	+150	°C
T_{SOL}	Soldering temp. (10s @ 1/16 in. = 1.5 mm)		-	+260	°C
T_J	Junction temperature		-	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. V_{IN} should not exceed V_{CCINT} by more than 3.6V over extended periods of time.
4. Spartan-II I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature (1)	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND (2)	Commercial	2.5 – 5%	2.5 + 5%	V
		Industrial	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND (3)	Commercial	1.4	3.6	V
		Industrial	1.4	3.6	V
T_{IN}	Input signal transition time (4)		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} –5%), all delay parameters increase by 3%.
3. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of V_{CCO}.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)		2.0	-	V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)		1.2	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (1)	XC2S15 (1)	-	30	mA
		XC2S30 (1)	-	30	mA
		XC2S50	-	50	mA
		XC2S100	-	50	mA
		XC2S150	-	50	mA
		XC2S200	-	75	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (2)		-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin		-	20	µA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)	VQ, CS, TQ, PQ, FG packages	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested) (3)		-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested) (3)		-	0.15	mA

Notes:
1. Advance information.
2. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
3. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

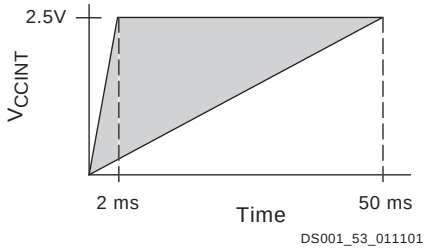
Supply Current Requirements During Power-up

Spartan-II FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power up. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. Use this approach to avoid inadvertently tripping crowbar and foldback supplies.

Symbol	Description		Min(3)	Max	Units
I_{CCPO}	Total V_{CCINT} supply current required during power-up	Commercial	500	-	mA
		Industrial	2	-	A
T_{CCPO}	V_{CCINT}(2,3,4)		2	50	ms

Notes:
1. The I_{CCPO} requirement occurs before V_{CCINT} reaches 1V.
2. The rise time is measured from GND to V_{CCINT} max on a fully loaded board.
3. V_{CCINT} must not dip in the negative direction during power on. It is acceptable for V_{CCINT} to flatten out during the peak power-on current draw.
4. For guaranteed power-up, the V_{CCINT} ramp must stay in the shaded area of the graph below.



DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	N/A	40	N/A
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	N/A	36	N/A
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.5	V_{REF} + 0.5	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.5	V_{REF} + 0.5	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

All -5 timing numbers are Preliminary for both Commercial and Industrial XC2S50, XC2S100, and XC2S150 devices. All -5 timing numbers for the XC2S15, XC2S30, and XC2S200 devices, Commercial and Industrial, are Advance. All -6 timing numbers are Advance.

Global Clock Input to Output Delay for LVTTL, *with* DLL(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min.	Max.	Max.	
$T_{ICKOFDLL}$	Global Clock Input to Output Delay using Output Flip-Flop for LVTTL, 12 mA, Fast Slew Rate, *with* DLL.	XC2S15	0	3.3	3.3	ns, max
		XC2S30	0	3.3	3.3	ns, max
		XC2S50	0	3.3	3.3	ns, max
		XC2S100	0	3.3	3.3	ns, max
		XC2S150	0	3.3	3.3	ns, max
		XC2S200	0	3.3	3.3	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables **Constants for Calculating T_{IOOP}** and **Delay Measurement Methodology**, page 10.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in **IOB Output Delay Adjustments for Different Standards**, page 9.

Global Clock Input to Output Delay for LVTTL, *without* DLL(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min.	Max.	Max.	
T_{ICKOF}	Global Clock Input to Output Delay using Output Flip-Flop for LVTTL, 12 mA, Fast Slew Rate, *without* DLL.	XC2S15	0	4.5	5.4	ns, max
		XC2S30	0	5.6	5.4	ns, max
		XC2S50	0	4.6	5.4	ns, max
		XC2S100	0	4.6	5.5	ns, max
		XC2S150	0	4.6	5.5	ns, max
		XC2S200	0	4.7	5.6	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables **Constants for Calculating T_{IOOP}** and **Delay Measurement Methodology**, page 10.
3. For data *output* with different standards, adjust delays with the values shown in **IOB Output Delay Adjustments for Different Standards**, page 9.

Global Clock Setup and Hold for LVTTL Standard, *with* DLL

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
T_{PSDLL} / T_{PHDLL}	Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard, no delay, IFF,(1) with DLL	XC2S15		1.9 / 0	ns, min
		XC2S30		1.9 / 0	ns, min
		XC2S50		1.9 / 0	ns, min
		XC2S100		2.0 / 0	ns, min
		XC2S150		2.0 / 0	ns, min
		XC2S200		2.1 / 0	ns, min

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. A "0" Hold Time listing indicates no hold time or a negative hold time.
5. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards**, page 7.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
T_{PSFD} / T_{PHFD}	Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard, full delay, IFF,(1) without DLL	XC2S15		2.7 / 0	ns, min
		XC2S30		2.7 / 0	ns, min
		XC2S50		2.7 / 0	ns, min
		XC2S100		2.8 / 0	ns, min
		XC2S150		2.9 / 0	ns, min
		XC2S200		3.0 / 0	ns, min

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A "0" Hold Time listing indicates no hold time or a negative hold time.
4. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards**, page 7.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Delay Adjustments for Different Standards**, page 7.

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
Propagation Delays					
T_{IOPI}	Pad to I output, no delay	All		1.0	ns, max
T_{IOPID}	Pad to I output, with delay	XC2S15		1.8	ns, max
		XC2S30		1.8	ns, max
		XC2S50		1.8	ns, max
		XC2S100		1.8	ns, max
		XC2S150		1.8	ns, max
		XC2S200		1.8	ns, max
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All		2.0	ns, max
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15		4.5	ns, max
		XC2S30		4.5	ns, max
		XC2S50		4.5	ns, max
		XC2S100		4.5	ns, max
		XC2S150		4.7	ns, max
		XC2S200		4.7	ns, max
Sequential Delays					
T_{IOCKIQ}	Clock CLK to output IQ	All		0.8	ns, max
Setup/Hold Times with Respect to Clock CLK(2)					
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All		1.9 / 0	ns, max
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay(1)	XC2S15		4.4 / 0	ns, max
		XC2S30		4.4 / 0	ns, max
		XC2S50		4.4 / 0	ns, max
		XC2S100		4.4 / 0	ns, max
		XC2S150		4.6 / 0	ns, max
		XC2S200		4.6 / 0	ns, max
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All		0.9 / 0.01	ns, max
Set/Reset Delays					
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All		1.2	ns, max
T_{IOSRIQ}	SR input to IQ (asynchronous)	All		1.7	ns, max
T_{GSRQ}	GSR to output IQ	All		11.7	ns, max

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 10.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

IOB Input Delay Adjustments for Different Standards(1)

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL		0	ns
$T_{ILVCMOS2}$		LVCMOS2		–0.05	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V		–0.13	ns
T_{IPCI33_5}		PCI, 33 MHz, 5.0V		0.30	ns
T_{IPCI66_3}		PCI, 66 MHz, 3.3V		–0.13	ns
T_{IGTL}		GTL		0.24	ns
T_{IGTLP}		GTL+		0.13	ns
T_{IHSTL}		HSTL		0.04	ns
T_{ISSTL2}		SSTL2		–0.09	ns
T_{ISSTL3}		SSTL3		–0.05	ns
T_{ICTT}		CTT		0.02	ns
T_{IAGP}		AGP		–0.07	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 10.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Delay Adjustments for Different Standards**, page 9.

Symbol	Description	Speed Grade		Units
		-6	-5	
Propagation Delays				
T_{IOOP}	O input to Pad		3.4	ns, max
T_{IOOLP}	O input to Pad via transparent latch		4.0	ns, max
3-state Delays				
T_{IOTHZ}	T input to Pad high-impedance (1)		2.3	ns, max
T_{IOTON}	T input to valid data on Pad		3.6	ns, max
$T_{IOTLPHZ}$	T input to Pad high-impedance via transparent latch (1)		2.9	ns, max
$T_{IOTLPON}$	T input to valid data on Pad via transparent latch		4.2	ns, max
T_{GTS}	GTS to Pad high impedance (1)		5.9	ns, max
Sequential Delays				
T_{IOCKP}	Clock CLK to Pad		3.4	ns, max
T_{IOCKHZ}	Clock CLK to Pad high-impedance (synchronous)		2.7	ns, max
T_{IOCKON}	Clock CLK to valid data on Pad (synchronous)		4.0	ns, max
Setup/Hold Times with Respect to Clock CLK (2)				
T_{IOOCK} / T_{IOCKO}	O input		1.3 / 0	ns, max
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input		0.9 / 0.01	ns, max
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)		1.3 / 0	ns, max
T_{IOTCK} / T_{IOCKT}	3-state Setup Times, T input		0.9 / 0	ns, max
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state Setup Times, TCE input		1.0 / 0	ns, max
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state Setup Times, SR input (TFF)		1.2 / 0	ns, max
Set/Reset Delays				
T_{IOSRP}	SR input to Pad (asynchronous)		4.4	ns, max
T_{IOSRHZ}	SR input to Pad high impedance (asynchronous)		3.7	ns, max
$T_{IOTSRON}$	SR input to valid data on Pad (asynchronous)		4.9	ns, max
T_{IOGSRQ}	GSR to Pad		11.7	ns, max

Notes:
1. Three-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA		16.9	ns
T_{OLVTTL_S4}		4 mA		8.6	ns
T_{OLVTTL_S6}		6 mA		5.5	ns
T_{OLVTTL_S8}		8 mA		3.5	ns
T_{OLVTTL_S12}		12 mA		2.2	ns
T_{OLVTTL_S16}		16 mA		2.0	ns
T_{OLVTTL_S24}		24 mA		1.5	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA		15.0	ns
T_{OLVTTL_F4}		4 mA		6.1	ns
T_{OLVTTL_F6}		6 mA		3.6	ns
T_{OLVTTL_F8}		8 mA		1.2	ns
T_{OLVTTL_F12}		12 mA		0	ns
T_{OLVTTL_F16}		16 mA		–0.15	ns
T_{OLVTTL_F24}		24 mA		–0.23	ns
$T_{OLVCMOS2}$		LVCMOS2		0.18	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V		2.9	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V		3.5	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V		–0.42	ns
T_{OGTL}		GTL		0.7	ns
T_{OGTLP}		GTL+		1.1	ns
T_{OHSTL_I}		HSTL I		–0.54	ns
T_{OHSTL_III}		HSTL III		–1.0	ns
T_{OHSTL_IV}		HSTL IV		–1.1	ns
T_{OSSTL2_I}		SSTL2 I		–0.54	ns
T_{OSSLT2_II}		SSTL2 II		–1.0	ns
T_{OSSTL3_I}		SSTL3 I		–0.54	ns
T_{OSSTL3_II}		SSTL3 II		–1.1	ns
T_{OCTT}		CTT		–0.6	ns
T_{OAGP}		AGP		–1.0	ns

Notes:
1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables **Constants for Calculating T_{IOOP}** and **Delay Measurement Methodology**, page 10.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table **Constants for Calculating T_{IOOP}**, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from **IOB Output Delay Adjustments for Different Standards**, page 9, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Constants for Calculating T_{IOOP}

Standard	C_{SL} (1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHZ 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016

Constants for Calculating T_{IOOP} *(Continued)*

Standard	C_{SL} (1) (pF)	F_L (ns/pF)
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Delay Measurement Methodology

Standard	V_L (1)	V_H (1)	Meas. Point	V_{REF} Typ (2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I and II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I and II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2xV_{CCO})$	$V_{REF} + (0.2xV_{CCO})$	V_{REF}	Per AGP Spec

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the previous table, **Constants for Calculating T_{IOOP}**.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Guidelines(1)

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
GCLK Clock Skew					
$T_{GSKEWIOB}$	Global Clock Skew between IOB flip-flops	XC2S15		0.14	ns, max
		XC2S30		0.14	ns, max
		XC2S50		0.14	ns, max
		XC2S100		0.15	ns, max
		XC2S150		0.15	ns, max
		XC2S200		0.16	ns, max

Notes:
1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
GCLK IOB and Buffer				
T_{GPIO}	Global Clock PAD to output		0.8	ns, max
T_{GIO}	Global Clock Buffer I input to O output		0.8	ns, max

I/O Standard Global Clock Input Adjustments

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL		0	ns, max
$T_{GPLVCMOS2}$		LVCMOS2		–0.05	ns, max
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V		–0.13	ns, max
$T_{GPPCI33\_5}$		PCI, 33 MHz, 5.0V		0.30	ns, max
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V		–0.13	ns, max
T_{GPGTL}		GTL		0.9	ns, max
T_{GPGTLP}		GTL+		0.8	ns, max
T_{GPHSTL}		HSTL		0.7	ns, max
$T_{GPSSTL2}$		SSTL2		0.51	ns, max
$T_{GPSSTL3}$		SSTL3		0.55	ns, max
T_{GPCTT}		CTT		0.7	ns, max
T_{GPAGP}		AGP		0.53	ns, max

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 10.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6(2)		-5		
		Min	Max	Min	Max	
$F_{CLKINHF}$	Input Clock Frequency (CLKDLLHF)	60	200	60	180	MHz
$F_{CLKINLF}$	Input Clock Frequency (CLKDLL)	25	100	25	90	MHz
$T_{DLLPWHF}$	Input Clock Pulse Width (CLKDLLHF)	2.0	-	2.4	-	ns
$T_{DLLPWLF}$	Input Clock Pulse Width (CLKDLL)	2.5	-	3.0	-	ns

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to + 85°C).
2. Advance Information

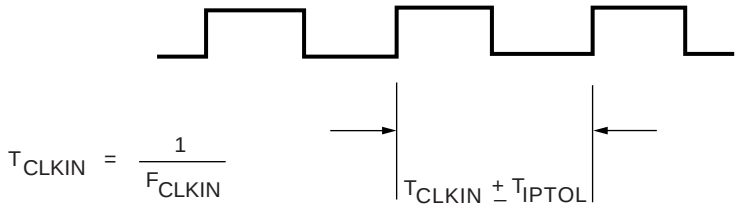
DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 1, page 13, provides definitions for various parameters in the table below.

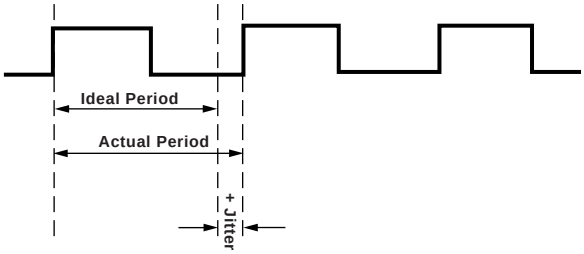
Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input Clock Period Tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input Clock Jitter Tolerance (Cycle to Cycle)		-	±150	-	±300	ps
T_{LOCK}	Time Required for DLL to Acquire Lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)		-	±60	-	±60	ps
T_{PHIO}	Phase Offset between CLKIN and CLKO(2)		-	±100	-	±100	ps
T_{PHOO}	Phase Offset between Clock Outputs on the DLL(3)		-	±140	-	±140	ps
T_{PHIOM}	Maximum Phase Difference between CLKIN and CLKO(4)		-	±160	-	±160	ps
T_{PHOOM}	Maximum Phase Difference between Clock Outputs on the DLL(5)		-	±200	-	±200	ps

Notes:
1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference

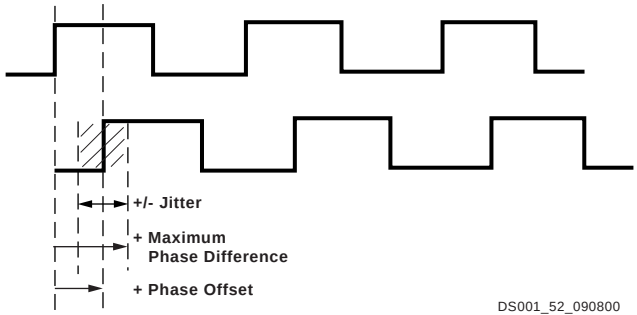


Figure 1: **Period Tolerance and Clock Jitter**

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{ILO}	4-input function: F/G inputs to X/Y outputs		0.7	ns, max
T_{IF5}	5-input function: F/G inputs to F5 output		0.9	ns, max
T_{IF5X}	5-input function: F/G inputs to X output		1.1	ns, max
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX		1.1	ns, max
T_{F5INY}	6-input function: F5IN input to Y output		0.4	ns, max
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs		0.9	ns, max
T_{BYYB}	BY input to YB output		0.7	ns, max
Sequential Delays				
T_{CKO}	FF Clock CLK to XQ/YQ outputs		1.3	ns, max
T_{CKLO}	Latch Clock CLK to XQ/YQ outputs		1.5	ns, max
Setup/Hold Times with Respect to Clock CLK (1)				
T_{ICK} / T_{CKI}	4-input function: F/G inputs		1.4 / 0	ns, max
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs		1.8 / 0	ns, max
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input		1.1 / 0	ns, max
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX		1.8 / 0	ns, max
T_{DICK} / T_{CKDI}	BX/BY inputs		0.8 / 0	ns, max
T_{CECK} / T_{CKCE}	CE input		0.9 / 0	ns, max
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)		0.8 / 0	ns, max
Clock CLK				
T_{CH}	Minimum Pulse Width, High		1.9	ns, max
T_{CL}	Minimum Pulse Width, Low		1.9	ns, max
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR/BY inputs		3.1	ns, max
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)		1.3	ns, max
T_{IOGSRQ}	Delay from GSR to XQ/YQ outputs		11.7	ns, max
F_{TOG}	Toggle Frequency (for export control)		263	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{OPX}	F operand inputs to X via XOR		0.9	ns, max
T_{OPXB}	F operand input to XB output		1.5	ns, max
T_{OPY}	F operand input to Y via XOR		2.0	ns, max
T_{OPYB}	F operand input to YB output		2.0	ns, max
T_{OPCYF}	F operand input to COUT output		1.5	ns, max
T_{OPGY}	G operand inputs to Y via XOR		1.1	ns, max
T_{OPGYB}	G operand input to YB output		2.0	ns, max
T_{OPCYG}	G operand input to COUT output		1.4	ns, max
T_{BXCY}	BX initialization input to COUT		1.0	ns, max
T_{CINX}	CIN input to X output via XOR		0.5	ns, max
T_{CINXB}	CIN input to XB		0.1	ns, max
T_{CINY}	CIN input to Y via XOR		0.6	ns, max
T_{CINYB}	CIN input to YB		0.7	ns, max
T_{BYP}	CIN input to COUT output		0.1	ns, max
Multiplier Operation				
T_{FANDXB}	F1/2 operand inputs to XB output via AND		0.5	ns, max
T_{FANDYB}	F1/2 operand inputs to YB output via AND		1.1	ns, max
T_{FANDCY}	F1/2 operand inputs to COUT output via AND		0.6	ns, max
T_{GANDYB}	G1/2 operand inputs to YB output via AND		0.7	ns, max
T_{GANDCY}	G1/2 operand inputs to COUT output via AND		0.2	ns, max
Setup/Hold Times with Respect to Clock CLK (1)				
T_{CCKX} / T_{CKCX}	CIN input to FFX		1.2 / 0	ns, max
T_{CCKY} / T_{CKCY}	CIN input to FFY		1.3 / 0	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

CLB Distributed RAM and Shift Register Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Sequential Delays (includes Shift-Register Mode)				
T_{SHCKO}	Clock CLK to X/Y outputs (WE active)		2.6	ns, max
Setup/Hold Times with Respect to Clock CLK (1)				
T_{AS} / T_{AH}	F/G address inputs		0.7 / 0	ns, max
T_{DS} / T_{DH}	BX/BY data inputs (DIN)		0.9 / 0	ns, max
T_{WS} / T_{WH}	CE input (WS)		1.0 / 0	ns, max
Shift-Register Mode				
T_{SHDICK}	BX/BY data inputs (DIN)		0.9	ns, max
T_{SHCECK}	BX/BY data inputs (DIN)		1.0	ns, max
Clock CLK				
T_{WPH}	Minimum Pulse Width, High		2.9	ns, max
T_{WPL}	Minimum Pulse Width, Low		2.9	ns, max
T_{WC}	Minimum clock period to meet address write cycle time		5.8	ns, max
Shift-Register Mode				
T_{SRPH}	Minimum Pulse Width, High		2.9	ns, max
T_{SRPL}	Minimum Pulse Width, Low		2.9	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Block RAM Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Sequential Delays				
T_{BCKO}	Clock CLK to DOUT output		4.0	ns, max
Setup/Hold Times with Respect to Clock CLK (1)				
T_{BACK} / T_{BCKA}	ADDR inputs		1.4 / 0	ns, max
T_{BDCK}/ T_{BCKD}	DIN inputs		1.4 / 0	ns, max
T_{BECK}/ T_{BCKE}	EN inputs		3.2 / 0	ns, max
T_{BRCK}/ T_{BCKR}	RST input		2.9 / 0	ns, max
T_{BWCK}/ T_{BCKW}	WEN input		2.8 / 0	ns, max
Clock CLK				
T_{BPWH}	Minimum Pulse Width, High		1.9	ns, max
T_{BPWL}	Minimum Pulse Width, Low		1.9	ns, max
T_{BCCS}	CLKA -> CLKB setup time for different ports		4.0	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{IO}	IN input to OUT output		0	ns, max
T_{OFF}	TRI input to OUT output high-impedance		0.12	ns, max
T_{ON}	TRI input to valid data on OUT output		0.12	ns, max

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
T_{TAPTCK}	TMS and TDI Setup times before TCK		4.0	ns, max
T_{TCKTAP}	TMS and TDI Hold times after TCK		2.0	ns, max
T_{TCKTDO}	Output delay from clock TCK to output TDO		11.0	ns, max
F_{TCK}	Maximum TCK clock frequency		33	MHz, max

Revision History

Version No.	Date	Description
2.0	09/18/00	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
2.1	11/02/00	Removed Power Down feature.
2.2	01/19/01	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.

The Spartan-II Family Data Sheet

DS001-1, ***Spartan-II 2.5V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS001-2, ***Spartan-II 2.5V FPGA Family: Functional Description*** (Module 2)

DS001-3, ***Spartan-II 2.5V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS001-4, ***Spartan-II 2.5V FPGA Family: Pinout Tables*** (Module 4)