XCR3384XL: 384 Macrocell CPLD

DS024 (v1.0) February 8, 2001 **Advance Product Specification**

Features

- 7.5 ns pin-to-pin logic delays
- System frequencies up to 127 MHz
- 384 macrocells with 9,600 usable gates
- Available in small footprint packages
  - 208-pin PQFP (172 user I/O)
  - 256-ball FBGA (212 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V supply voltage at industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

Description

The XCR3384XL is a 3.3V, 384 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 24 function blocks provide 9,600 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 127 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3384XL TotalCMOS CPLD (data taken with 24 up/down, loadable 16-bit counters at 3.3V, 25°C).

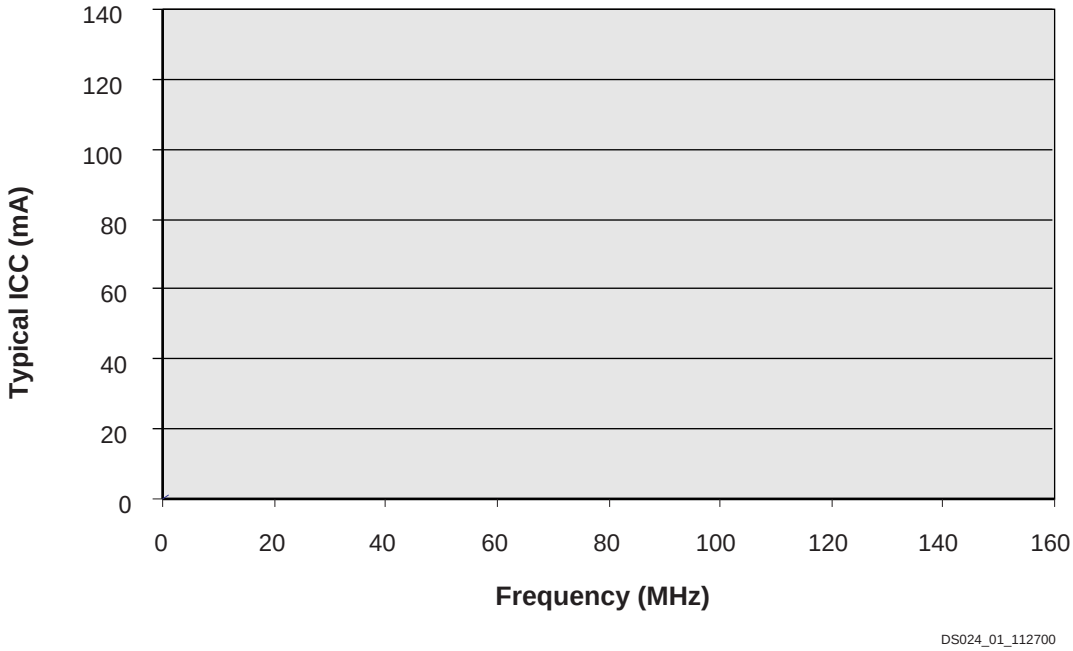


Figure 1: **XCR3384XL Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Frequency (MHz)	0	1	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}(2)	Output High voltage	Commercial: I_{OH} = –8 mA	2.4	-	V
		Industrial:I_{OH} = –6 mA	2.4	-	V
		I_{OH} = –500 µA	90% V_{CC}	-	V
V_{OL}	Output Low voltage	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(3,4)	f = 1 MHz	-		mA
		f = 50 MHz	-		mA
C_{IN}	Input pin capacitance(5)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(5)	f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance(5)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See Figure 2 for typical V_{OH}/I_{OH} curve.
3. See Table 1, Figure 1 for typical values.
4. This parameter measured with a 16-bit, loadable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
5. Typical values, not tested.

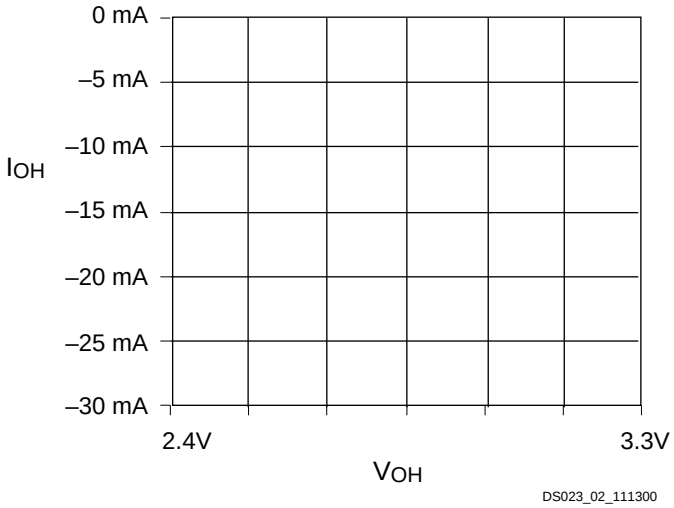


Figure 2: **Typical V_{OH} vs. I_{OH} at 3.3V, T_A = 25°C**

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	7.0	-	9.0	-	10.8	ns
T_{PD2}	Propagation delay time (OR array)(3)	-	7.5	-	10.0	-	12.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.5	-	5.8	-	6.9	ns
T_{SUF}(4)	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T_{SU}(4)	Setup time	4.8	-	6.5	-	7.9	-	ns
T_H(4)	Hold time	0	-	0	-	0	-	ns
T_{WLH}(4)	Global Clock pulse width (High or Low)	3.0	-	4.0	-	5.0	-	ns
Tt_{PLH}(4)	P-term clock pulse width	4.5	-	6.0	-	7.5	-	ns
T_R(4)	Input rise time	-	20	-	20	-	20	ns
T_L(4)	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}(4)	Maximum system frequency	-	127	-	102	-	83	MHz
T_{CONFIG}(4)	Configuration time(5)	-	40	-	40	-	40	µs
T_{POE}(4)	P-term OE to output enabled	-	9.0	-	11.0	-	13.0	ns
T_{POD}(4)	P-term OE to output disabled(6)	-	9.0	-	11.0	-	13.0	ns
T_{PCO}(4)	P-term clock to output	-	8.0	-	10.3	-	12.4	ns
T_{PAO}(4)	P-term set/reset to output valid	-	9.0	-	11.0	-	13.0	ns

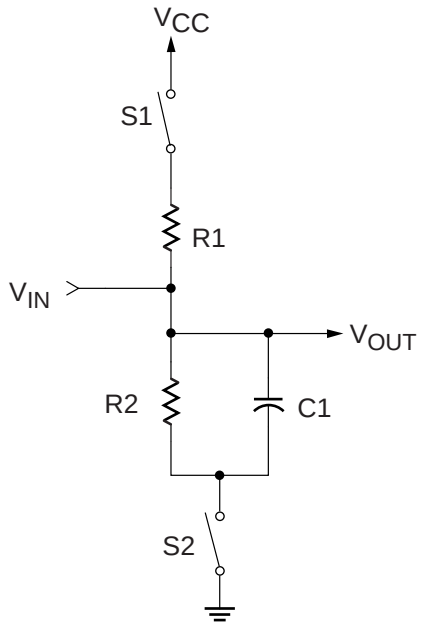
Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 4 for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 10 mA at 3.6V.
6. Output C_L = 5 pF.

Internal Timing Parameters(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.3	-	4.0	ns
T_{FIN}	Fast input buffer delay	-	2.2	-	2.8	-	3.3	ns
T_{GCK}	Global clock buffer delay	-	1.0	-	1.3	-	1.5	ns
T_{OUT}	Output buffer delay	-	2.5	-	2.8	-	3.3	ns
T_{EN}	Output buffer enable/disable delay	-	4.5	-	5.2	-	6.0	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	ns
T_{SUI}	Register setup time	0.8	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.0	-	2.0	-	2.2	ns
T_{RAI}	Register async. recovery	-	5.0	-	7.0	-	8.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.5	-	3.0	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.5	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	3.6	-	4.0	-	5.0	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	2.0	-	2.5	-	3.0	ns
T_{UDA}	Universal delay	-	2.2	-	2.8	-	3.5	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:
1. These parameters guaranteed by design and/or characterization, not testing.
2. See XPLA3 family data sheet (DS012) for timing model.

Switching Characteristics



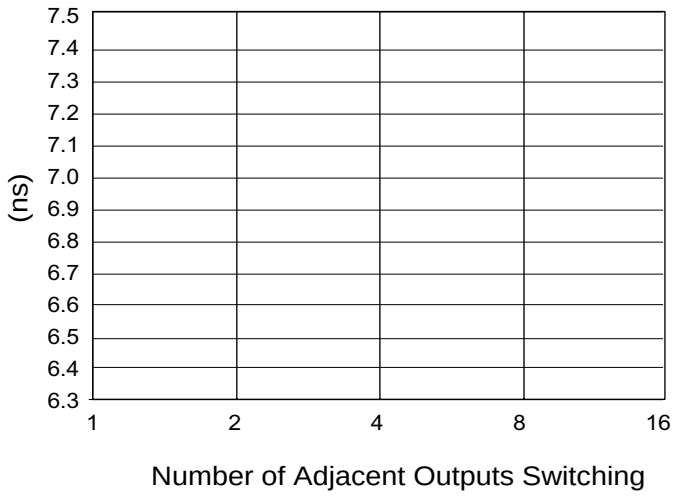
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

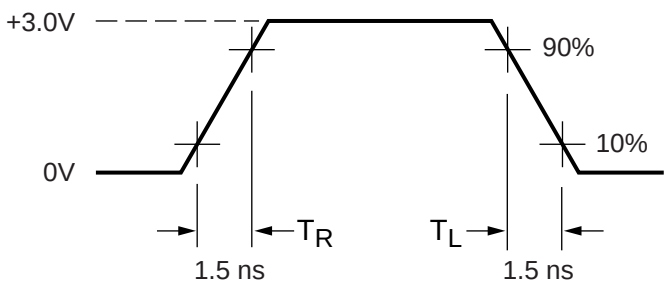
DS013_03_050200

Figure 3: **AC Load Circuit**



DS024_04_11800

Figure 4: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3384XL I/O Pins**

Function Block	Macrocell	PQ208	FT256
1	1	-	E15
1	2	-	F13
1	3	13	E16
1	4	15	F14
1	5	16	F15
1	6	-	-
1	7	-	-
1	8	-	-
1	9	-	-
1	10	-	-
1	11	-	-
1	12	-	-
1	13	17	G12
1	14	18	G15
1	15	19	G13
1	16	20	F16
2	1	12	E14
2	2	11	D16
2	3	10	F12
2	4	9	C16
2	5	8	E13
2	6	-	-
2	7	-	-
2	8	-	-
2	9	-	-
2	10	-	-
2	11	-	-
2	12	-	-
2	13	-	D15
2	14	7	D14
2	15	6	B16
2	16	-	C15
3	1	21	G14
3	2	22	G16
3	3	-	H13
3	4	-	-

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
3	5	24	H12
3	6	-	-
3	7	-	-
3	8	-	-
3	9	-	-
3	10	-	-
3	11	-	-
3	12	-	-
3	13	25	H15
3	14	26	H14
3	15	27	H16
3	16	28	J14
4	1	4	A16
4	2	3	E12
4	3	-	-
4	4	-	C14
4	5	207	D13
4	6	-	-
4	7	-	-
4	8	-	-
4	9	-	-
4	10	-	-
4	11	-	-
4	12	-	-
4	13	206	A15
4	14	205	B15
4	15	204	B14
4	16	203	C13
5	1	29	J15
5	2	30(1)	J13(1)
5	3	31	J16
5	4	-	L14
5	5	-	K15
5	6	-	-
5	7	-	-
5	8	-	-
5	9	-	-

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
5	10	-	-
5	11	-	-
5	12	-	-
5	13	33	K14
5	14	34	K16
5	15	35	K13
5	16	36	L15
6	1	62	R13
6	2	61	M11
6	3	60	T14
6	4	59	N12
6	5	58	R14
6	6	-	-
6	7	-	-
6	8	-	-
6	9	-	-
6	10	-	-
6	11	-	-
6	12	-	-
6	13	57	P13
6	14	56	T15
6	15	-	P14
6	16	-	T16
7	1	37	K12
7	2	38	L16
7	3	39	M15
7	4	40	N15
7	5	-	L13
7	6	-	-
7	7	-	-
7	8	-	-
7	9	-	-
7	10	-	-
7	11	-	-
7	12	-	-
7	13	-	M16
7	14	42	M14

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
7	15	43	N16
7	16	44	L12
8	1	55	M12
8	2	51	R15
8	3	-	N13
8	4	-	-
8	5	49	P16
8	6	-	-
8	7	-	-
8	8	-	-
8	9	-	-
8	10	-	-
8	11	-	-
8	12	-	-
8	13	48	N14
8	14	47	R16
8	15	46	M13
8	16	45	P15
9	1	187	D9
9	2	188	A9
9	3	189(1)	C10(1)
9	4	190	A10
9	5	-	D10
9	6	-	-
9	7	-	-
9	8	-	-
9	9	-	-
9	10	-	-
9	11	-	-
9	12	-	-
9	13	-	B11
9	14	192	C11
9	15	193	B12
9	16	194	E10
10	1	178	B8
10	2	177	D8
10	3	176(1)	A7(1)

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
10	4	175	C8
10	5	-	-
10	6	-	-
10	7	-	-
10	8	-	-
10	9	-	-
10	10	-	-
10	11	-	-
10	12	-	-
10	13	-	C7
10	14	173	B7
10	15	172	D7
10	16	171	A6
11	1	-	A14
11	2	202	E11
11	3	201	A13
11	4	-	D12
11	5	199	B13
11	6	-	-
11	7	-	-
11	8	-	-
11	9	-	-
11	10	-	-
11	11	-	-
11	12	-	-
11	13	198	C12
11	14	197	A12
11	15	196	D11
11	16	195	A11
12	1	163	E6
12	2	164	A4
12	3	-	C5
12	4	-	B5
12	5	166	D6
12	6	-	-
12	7	-	-
12	8	-	-

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
12	9	-	-
12	10	-	-
12	11	-	-
12	12	-	-
12	13	167	A5
12	14	168	C6
12	15	169	B6
12	16	170	E7
13	1	70	N10
13	2	69	P11
13	3	68	M10
13	4	67	R11
13	5	66	T12
13	6	-	-
13	7	-	-
13	8	-	-
13	9	-	-
13	10	-	-
13	11	-	-
13	12	-	-
13	13	65	R12
13	14	64	N11
13	15	-	T13
13	16	-	P12
14	1	91	R6
14	2	92	M7
14	3	93	T5
14	4	-	T6
14	5	-	R5
14	6	-	-
14	7	-	-
14	8	-	-
14	9	-	-
14	10	-	-
14	11	-	-
14	12	-	-
14	13	95	N6

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
14	14	96	T4
14	15	97	P5
14	16	98	R4
15	1	-	T11
15	2	-	-
15	3	71	R10
15	4	73	P10
15	5	76	T10
15	6	-	-
15	7	-	-
15	8	-	-
15	9	-	-
15	10	-	-
15	11	-	-
15	12	-	-
15	13	77	N9
15	14	78	R9
15	15	79	P9
15	16	80	T9
16	1	90	N7
16	2	89	T7
16	3	88	P6
16	4	87	R7
16	5	86	P7
16	6	-	-
16	7	-	-
16	8	-	-
16	9	-	-
16	10	-	-
16	11	-	-
16	12	-	-
16	13	-	T8
16	14	-	N8
16	15	84	R8
16	16	81	P8
17	1	147	E4
17	2	148	D1

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
17	3	149	F5
17	4	150	C2
17	5	151	D3
17	6	-	-
17	7	-	-
17	8	-	-
17	9	-	-
17	10	-	-
17	11	-	-
17	12	-	-
17	13	-	C1
17	14	-	-
17	15	153	B1
17	16	154	B2
18	1	146	D2
18	2	145	E3
18	3	144	E1
18	4	-	F4
18	5	-	F1
18	6	-	-
18	7	-	-
18	8	-	-
18	9	-	-
18	10	-	-
18	11	-	-
18	12	-	-
18	13	142	G5
18	14	141	E2
18	15	140	F3
18	16	139	F2
19	1	155	C3
19	2	156	D4
19	3	-	A2
19	4	-	A1
19	5	158	B3
19	6	-	-
19	7	-	-

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
19	8	-	-
19	9	-	-
19	10	-	-
19	11	-	-
19	12	-	-
19	13	159	C4
19	14	160	A3
19	15	161	D5
19	16	162	B4
20	1	138	G4
20	2	137	G1
20	3	136	G3
20	4	135	H1
20	5	-	H4
20	6	-	-
20	7	-	-
20	8	-	-
20	9	-	-
20	10	-	-
20	11	-	-
20	12	-	-
20	13	-	G2
20	14	133	H3
20	15	132	J1
20	16	131	J3
21	1	99	M6
21	2	100	T3
21	3	101	N5
21	4	102	R3
21	5	103	P4
21	6	-	-
21	7	-	-
21	8	-	-
21	9	-	-
21	10	-	-
21	11	-	-
21	12	-	-

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
21	13	104	T2
21	14	-	-
21	15	-	R2
21	16	106	N4
22	1	-	H2
22	2	130	J5
22	3	129	J2
22	4	128	J4
22	5	127(1)	K1(1)
22	6	-	-
22	7	-	-
22	8	-	-
22	9	-	-
22	10	-	-
22	11	-	-
22	12	-	-
22	13	126	K3
22	14	-	-
22	15	124	K2
22	16	123	L1
23	1	108	M5
23	2	109	P2
23	3	110	P3
23	4	111	T1
23	5	-	N3
23	6	-	-
23	7	-	-
23	8	-	-
23	9	-	-
23	10	-	-
23	11	-	-
23	12	-	-
23	13	-	R1
23	14	112	M4
23	15	113	P1
23	16	114	L5
24	1	122	K4

Table 2: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macrocell	PQ208	FT256
24	2	121	L3
24	3	120	K5
24	4	119	M1
24	5	-	L2
24	6	-	-
24	7	-	-
24	8	-	-
24	9	-	-
24	10	-	-
24	11	-	-
24	12	-	-
24	13	118	M2
24	14	117	L4
24	15	-	M3
24	16	115	N2

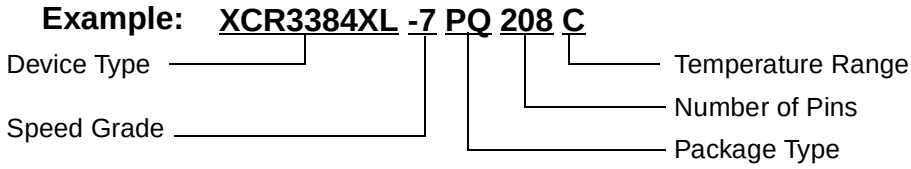
Notes:
1. JTAG pins.

Table 3: **XCR3384XL Global, JTAG, Port Enable, Power, and No Connect Pins**

Pin Type	PQ208	FT256
IN0 / CLK0	181	B9
IN1 / CLK1	182	A8
IN2 / CLK2	183	C9
IN3 / CLK3	184	B10
TCK	30	J13
TDI	176	A7
TDO	189	C10
TMS	127	K1
PORT_EN	116(1)	N1(1)
V_{CC}	5, 23, 41, 63, 74, 83, 85, 107, 125,143, 165, 179, 186, 191	E8, E9, F7, F8, F9, F10, G6, G11, H5, H6, H11, J6, J11, J12, K6, K11, L7, L8, L9, L10, M8, M9
GND	14, 32, 50, 72, 75, 82, 94, 134, 152, 174, 180, 185, 200	E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, L11
No Connects	1, 2, 52, 53, 54, 105, 157, 208	-

Notes:
1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet for full explanation.

Ordering Information



Device Ordering Options

Speed	
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay

Package	
PQ208	208-pin Plastic Quad Flat Package
FT256	256-ball Fineline BGA Package

Temperature	
C = Commercial	T_A = 0°C to +70°C V_{CC} = 3.0V to 3.6V
I = Industrial	T_A = –40°C to +85°C V_{CC} = 2.7V to 3.6V

Component Compatibility

Pins		208	256
Type		Plastic PQFP	Plastic FBGA
Code		PQ208	FT256
XCR3384XL	-7	C	C
	-10	C, I	C, I
	-12	C, I	C, I

Revision History

The following table shows the revision history for this document

Date	Version	Revision
02/08/01	1.0	Initial Xilinx release.