LogiCORE PCI-X Interface v4.0 For Virtex Series FPGAs

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Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408 559-7778
Fax: +1 408 626-6440
URL: http://www.xilinx.com/pci
Techsupport: http://support.xilinx.com
Feedback e-mail: logicore@xilinx.com

Introduction

With the Xilinx LogiCORE PCI-X Interface for Virtex series FPGAs, a designer can build a customized, 64-bit, 66 MHz, fully PCI-X 1.0 compliant system with the highest possible sustained performance, 528 Mbytes/sec, and up to 10 million system gates in a Virtex device.

Features

- Fully PCI 2.2 compliant, 64/32-bit, 33 MHz PCI initiator and target interface.
- Fully PCI-X 1.0 compliant, 64/32-bit, 66 MHz PCI-X initiator and target interface.
- Programmable single-chip solution with customizable user functionality.
- Pre-defined implementation for predictable timing in Virtex series FPGAs.
- Incorporates Xilinx Smart-IP Technology.
- 3.3 V PCI-X operation at 33-66 MHz.
- 3.3 V PCI operation at 0-33 MHz.
- Fully verified design tested with Xilinx proprietary testbench and hardware.
- Optional dual-port FIFOs may be added for maximum burst performance.
- Integrated extended capabilities:
  - PCI-X Capability Item
  - Power Management Capability Item
  - Message Signalled Interrupt Capability Item

LogiCORE™ Facts

Core Specifics		
Device Family		Virtex
System Clock f_{max}		66 MHz
Resources Used		
	I/O	**System Gates**
PCI-X 64/66[1]	89	30,000 - 40,000
PCI 64/33[1]	89	20,000 - 30,000
Supported Devices		
PCI-X 64/66		Virtex-E V300EBG432-8
PCI 64/33		Virtex-E V300EBG432-8
Provided with Core		
Documentation		*PCI-X Design Guide* *PCI-X Implementation Guide*
Design File Formats		Verilog/VHDL Simulation Model Verilog/VHDL Instantiation Code NGO Netlist
Constraint Files		User Constraint File (UCF)
Verification Tools		Verilog/VHDL Testbench
Example Design		Ping-X Example Design
Design Tool Requirements		
Xilinx Core Tools		M3.3i
Tested Entry and Verification Tools[2]		Synplicity Synplify Synopsys FPGA Express Synopsys FPGA Compiler II Exemplar Leonardo Spectrum Cadence Verilog XL Model Technology ModelSim

Xilinx provides technical support for this LogiCORE product when used as described in the Design Guide and the Implementation Guide. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed above, or if customized beyond that allowed in the product documentation, or if any changes are made in sections of design marked as “DO NOT MODIFY”.

1. The exact number of system gates depends on user configuration of the interface and level of resource sharing with adjacent logic. For example, a factor that may affect the size of the design is the number and size of the base address registers.
2. See the Xilinx web site for current supported versions.

Features (cont.)

- Supported PCI and PCI-X functions:
  - Full 64-bit Addressing Support
  - Memory Write
  - I/O Read, I/O Write
  - Configuration Read, Configuration Write
  - Bus Parking
  - Special Cycles
  - Interrupt Acknowledge
  - Type 0 Configuration Space Header
  - Up to 6 Base Address Registers (MEM or I/O with adjustable block size from 16 bytes to 8 Exabytes)
  - Expansion ROM Base Address Register
  - Cardbus CIS Pointer Register
  - Instant-On Base Address Registers
  - Parity Generation, Parity Error Detection
  - Target Abort, Target Retry, Target Disconnect
  - Full Command/Status Registers
- Supported PCI-X only functions:
  - Split Completion, Split Response
  - Memory Read DWORD
  - Memory Read Block
  - Memory Write Block
- Supported PCI only functions:
  - Memory Read
  - Memory Read Multiple (MRM)
  - Memory Read Line (MRL)
  - Memory Write and Invalidate (MWI)
- Available for configuration and download on the web.

Ease of Design

The Xilinx LogiCORE PCI-X Interface has several new features to make the design of a customized PCI-X application easier than ever:

- Simplified user application interface:
  - Reduces logic needed for target and initiator designs
  - Retains inherent flexibility of Xilinx PCI interfaces
  - Only one user design required for PCI-X or PCI bus modes and 32-bit or 64-bit bus widths
- Automatically handles datapath width conversion during 64-bit and 32-bit transactions.
- Unidirectional datapaths for easier, register-to-register timing.
- Automatically detects bus mode and bus width, and configures interface to match.

Applications

- Embedded applications in networking, industrial, and telecommunication systems.
- Server and other high performance I/O applications.
- PCI or PCI-X add-in boards such as frame buffers, network adapters, and data acquisition boards.
- Storage and other applications that require full support of 64-bit addressing.
- Other applications that need a PCI or PCI-X interface.

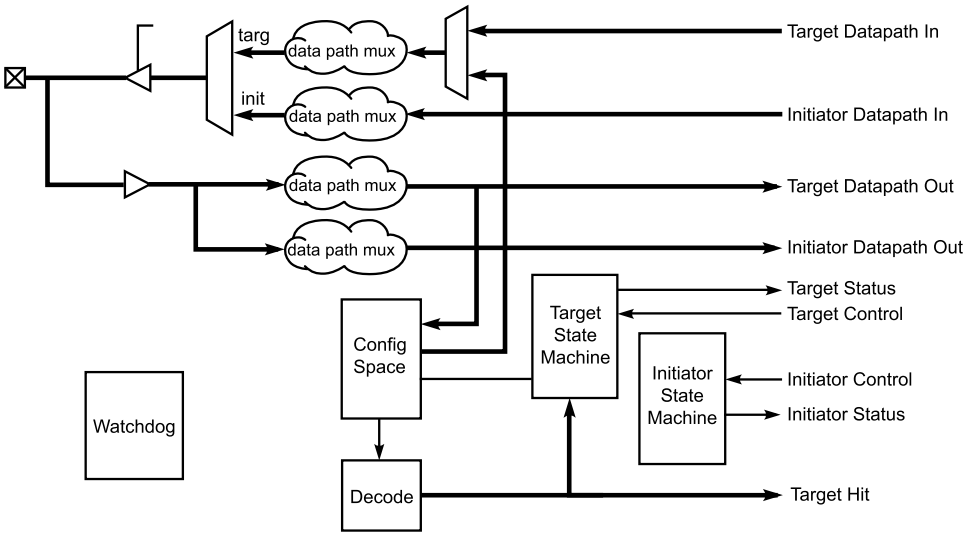

Figure 1: LogiCORE PCI-X Interface Block Diagram

General Description

The LogiCORE PCI-X Interface is a pre-implemented and fully tested module for Xilinx Virtex series FPGAs. The pinout for each device and the relative placement of the internal logic are pre-defined. Critical paths are controlled by constraint files to ensure predictable timing. This significantly reduces the engineering time required to implement the PCI-X portion of your design. Resources can instead be focused on your unique user application logic in the FPGA and on the system level design. As a result, LogiCORE PCI-X products can minimize your product development time.

Xilinx Virtex series FPGAs enable designs of fully PCI-X compliant systems. The devices meet all required electrical and timing parameters including AC output drive characteristics, input capacitance specifications, setup, hold, and clock to output. These devices meet all specifications for both 3.3 V (0-33 MHz) PCI and 3.3V PCI-X (33-66 MHz),.

The PCI-X Compliance Checklist has detailed information about electrical compliance. Other features that enable efficient implementation of a complete PCI-X system in the Virtex series include:

- Block SelectRAM+™ memory. Blocks of on-chip ultra-fast RAM with synchronous write and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.
- Select-RAM™ memory. Distributed on-chip ultra-fast RAM with synchronous write option and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.

The initiator and target Interface module is carefully optimized for best possible performance and utilization in Virtex series FPGA devices.

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, Xilinx Smart-IP technology ensures highest performance, predictability, repeatability, and flexibility in PCI-X designs. The Smart-IP technology is incorporated in every LogiCORE PCI-X Interface.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables, distributed RAM, and segmented routing, as well as floorplanning information, such as logic mapping and relative location constraints. This technology provides the best physical layout, predictability, and performance. Additionally, these features allow for significantly reduced compile times over competing architectures.

To guarantee the critical setup, hold, minimum clock to out, and maximum clock to out timing, the PCI-X interface is delivered with Smart-IP constraint files that are unique for a device and package combination. These constraint files guide the implementation tools so that the critical paths always are within specification. Retargeting the PCI-X interface to an unsupported device will void the guarantee of timing. Contact one of the Xilinx XPERTs partners for support of unlisted devices and packages.

Functional Description

The LogiCORE PCI-X Interface is partitioned into six major blocks and a user application as shown in Figure 1. Each block is described below.

Datapath

There are four datapaths, in and out for both target and initiator. To improve timing and ease of design, the four unidirectional datapaths are multiplexed inside the interface. All data transfers are register-to-register. Since fewer registers are on each datapath, loading is reduced and false timing paths are eliminated.

Decode

When an address is broadcast on the bus, the decode module compares it to the base address registers for a match. If one occurs, the target state machine is activated.

PCI Configuration Space

This block provides the first 64 bytes of Type 0, version 2.2 Configuration Space Header, and an additional 64 bytes reserved for extended capabilities. The remaining 128 bytes of configuration space are available to the user for application specific registers. Together, these support software-driven “Plug-and Play” initialization and configuration. This includes information for Command, Status, Base Address Registers, and the extended capabilities required for PCI-X.

Three extended capabilities are provided in the interface:

- PCI-X Capability Item
- Power Management Capability Item
- Message Signalled Interrupt Capability Item

These capability items may be linked or delinked from the capabilities list as required, and user functions can be integrated into the capabilities list.

Watchdog

The watchdog monitors various system conditions, including bus mode and bus width. This module also indicates when run-time reconfiguration is required for loading different bitstreams.

Table 1: PCI Configuration Space Header

31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Rev ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR0)				10h
Base Address Register 1 (BAR1)				14h
Base Address Register 2 (BAR2)				18h
Base Address Register 3 (BAR3)				1Ch
Base Address Register 4 (BAR5)				20h
Base Address Register 5 (BAR5)				24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			CapPtr	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Power Management Capability		NxtCap	PM Cap	40h
Data	PMCSR_ BRE	PMSCR		44h
Message Control		NxtCap	MSI Cap	48h
Message Address				4Ch
Message Upper Address				50h
Reserved		Message Data		54h
PCI-X Command		NxtCap	PCI-X Cap	58h
PCI-X Status				5Ch
Reserved				60h-7Fh
Available User Configuration Space				80h-FFh

Note:
Shaded areas are not implemented in the LogiCORE PCI-X interface default configuration. These locations return zero during configuration read accesses.

Target State Machine

This block controls the PCI-X and PCI interface for target functions. The controller is a high-performance state machine using one-hot encoding for maximum performance. One-hot encoding of the state facilitates a high performance implementation in register rich Xilinx FPGA devices.

Initiator State Machine

This block controls the PCI-X and PCI interface for initiator functions. The initiator control logic also uses one-hot encoding for maximum performance.

User Interface

The PCI-X interface provides a simplified user application interface which allows a user to create one design that handles both PCI-X and PCI transactions without design changes, and both 32-bit and 64-bit data transfers without external data width conversion. This eliminates the need for multiple designs to support PCI-X and PCI and varying bus widths.

This streamlined interface also simplifies the amount of work needed to create a user application. The user interface can be designed as either a 32-bit or 64-bit interface and the PCI-X interface will automatically handle data conversions regardless of the width of the PCI-X or PCI bus.

Interface Configuration

The LogiCORE PCI-X Interface can easily be configured to fit unique system requirements by using the Xilinx Web-based Configuration and Download Tool or by changing the HDL configuration file. The following customization options, among many others, are supported by the interface and are described in the product documentation.

- Base Address Registers (number, size, and mode)
- Expansion ROM BAR
- Cardbus CIS pointer
- Configuration Space Header ROM
- Interrupt Connectivity
- Extended Command Use
- Capability Configuration

Burst Transfer

The PCI bus derives its performance from its ability to support burst transfers. The performance of any PCI application depends largely on the size of the burst transfer. A FIFO to support PCI burst transfer can efficiently be implemented using the Virtex on-chip RAM features, both Distributed and Block SelectRAM+™.

Each Virtex slice supports two 16x1 RAM blocks. This corresponds to 32 bits of single-ported RAM or 16 bits of dual-ported RAM, with simultaneous read/write capability. The Block SelectRAM+ can be used to create deep FIFOs.

Supported Commands

Table 2 lists the PCI bus commands supported by the LogiCORE PCI-X Interface, and Table 3 lists the supported PCI-X bus commands.

Table 2: PCI Bus Commands

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	Yes
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read[1]	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple[2]	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line[2]	Yes	Yes
1111	Memory Write Invalidate[2]	Yes	Yes

Note:
1. This command can only be used for a single DWORD transfer.
2. These commands have fixed byte enables of 0h.

Table 3: PCI-X Bus Commands

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	Yes
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read DWORD	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Alias to Memory Read Block	Yes	Yes
1001	Alias to Memory Write Block	Yes	Yes
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Split Completion	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Block	Yes	Yes
1111	Memory Write Block	Yes	Yes

Bandwidth

The LogiCORE PCI-X Interface supports fully compliant burst operations for both sourcing and receiving data. This interface supports a sustained bandwidth of up to 528 MBytes/sec in PCI-X mode and 256 MBytes/sec in PCI mode. In both PCI and PCI-X modes, the burst can be up to the 4096 bytes in length.

The flexible user application interface, combined with support for many different PCI-X features, gives users a solution that lends itself to use in many high-performance applications. The user is not locked into one DMA engine, hence, an optimized DMA that fits a specific application can be designed.

Attaining maximum bandwidth depends on several factors, including the system bus mode, the system chipset, and the ability of other devices to keep up with your data stream. In addition, performance can depend on the volume of other traffic on the bus from other devices.

Timing Specifications

The Virtex series FPGA devices, together with the LogiCORE PCI-X Interface, enable design of fully compliant PCI-X systems. The maximum speed at which your user design is capable of running can be affected by the size of the design. Table 4 shows the key timing parameters for the LogiCORE PCI-X Interface.

Verification Methods

Xilinx has developed a system-level testbench that allows simulation of an open PCI-X environment in which a LogiCORE PCI-X Interface may be tested by itself or with other simulatable PCI-X agents. Included in these agents are a behavioral host and target, and several other modules, including a bus signal recorder and a protocol monitor. The Xilinx PCI-X testbench is a powerful verification tool that is also used as the basis for verification of the LogiCORE PCI-X Interface. The interface is also tested in hardware for electrical, functional, and timing compliance.

Ping Example Design

The Ping-X example design, delivered in Verilog and VHDL, has been developed to provide an easy-to-understand tutorial which demonstrates many of the principles and techniques required to successfully use a LogiCORE PCI-X Interface in a design. The Ping-X design is also used as a test vehicle when verifying the PCI-X interface.

Table 4: PCI-X 66 MHz Timing Parameters [ns]

PCI Spec Parameter	Xilinx Parameter	Parameter	PCI-X Spec.		PCI-X V300-8		Units
			Min	Max	Min	Max	
T_{cyc}	T_{cyc}[1]	CLK Cycle Time	15	20	15	30	ns
T_{val}	$T_{ICKOFDLL}$	CLK to Bus Signals Valid	0.7	3.8	1	3.1	ns
$T_{val\ (ptp)}$	$T_{ICKOFDLL}$	CLK to REQ# and GNT# Valid	0.7	3.8	1	3.1	ns
T_{su}	T_{PSDLL}	Bus Signal Setup to CLK (IOB, DLL)	1.7		1.5		ns
$T_{su(ptp)}$	T_{PSDLL}	GNT# Setup to CLK (IOB, DLL)	1.7		1.5		ns
T_h	T_{PHDLL}	Input Hold Time After CLK (IOB, DLL)		0.5		0	ns
$T_{rst-off}$	$T_{rst-off}$[1]	RST# to Tri-state		40		40	ns

Notes:
1. Controlled by TIMESPECS, included in product

Device Utilization

Utilization of the device can vary significantly, depending on the configuration choices made by the designer. Factors that can affect the size of the interface are:

- Number of Base Address Registers Used. Turning off any unused BARs will save resources.
- Size of the BARs. Setting the BAR to a smaller size requires more flip-flops. A smaller address space requires more logic to decode.

Recommended Design Experience

The LogiCORE PCI-X Interface is pre-implemented allowing engineering focus on the unique user application functions of a PCI-X design. Regardless, PCI-X is a high-performance design that is challenging to implement in any technology, ASIC or FPGA. Therefore, previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, constraint files, and guide files is recommended. The challenge to implement a complete PCI-X design including user application functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.