WP119 (v1.0) August 28, 2000

Fast Zero Power (FZP™) Technology

Summary

This white paper provides an overview of the patented Fast Zero Power (FZP™) technology used in Xilinx CoolRunner® CPLDs.

Introduction

Fast Zero Power (FZP) is the patented design technology used in Xilinx CoolRunner CPLDs that enables high-speed, low-power programmable logic devices. FZP is a key technology for CoolRunner CPLDs that minimizes system current demand and allows small chip-scale packaging options. Low-power designs are enabled through FZP by using true CMOS both in process technology and design technique.

Note: All times mentioned are process technology dependent.

Sense Amplifier Technology

In existing CPLD architectures, the circuits that propagate logic-level transitions in the product-term array are derived from the original bipolar PLD design technology. Product term word lines have connections for each input into the logic block (and its complement) and thus have a large capacitive load. Switching on this line would be slow, therefore sense amplifiers are used at the end of each product term word line in the product-term array to achieve fast propagation delays. Because CPLD product terms cannot be decoded (as with memory locations in an EPROM, for example) there must be a sense amplifier for each individual product-term. These sense amplifiers operate continuously, drawing supply current even when not switching.

In CPLDs, logic block inputs (and their complements) are connected to the product term line as shown in Figure 1. The sense amplifiers operate in the linear region, and ensure fast propagation times by amplifying small changes on the product term line, such that it represents a full voltage swing. The sense amplifier can recognize a product term voltage change as little as 100 mV.

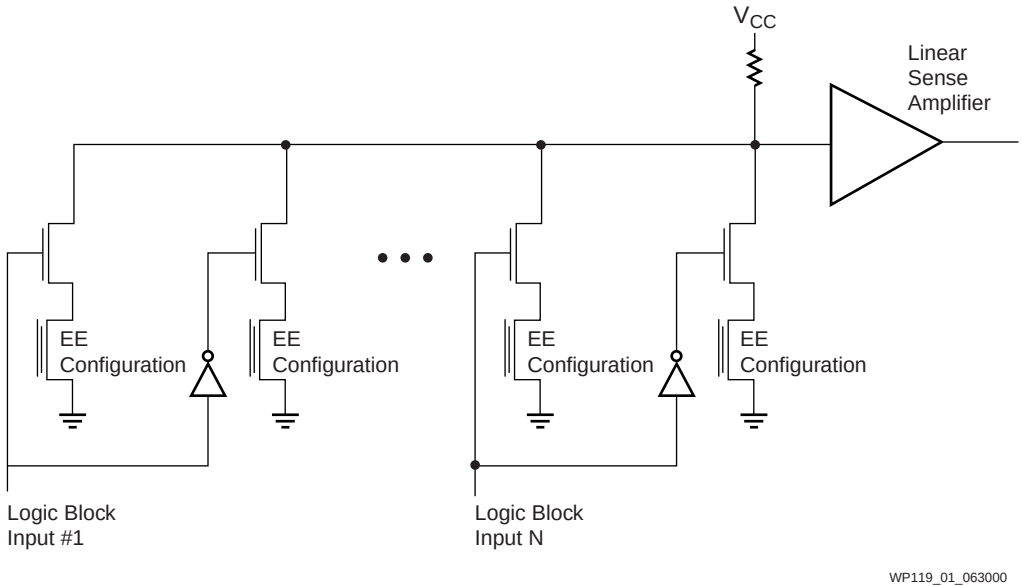

Figure 1: **Product Term in Existing CPLDs**

With the sense amplifier, a full voltage swing can be realized in a very short time by supplying the maximum current that the sense amplifier requires. The drawbacks of designing with sense amplifiers include noise rejection problems on the product term line and a large demand for system supply current.

FZP Technology

The FZP design technique used in Xilinx CoolRunner CPLDs takes a new and innovative approach to implementing the product term array. Instead of employing the bipolar design technique used in the sense amplifier approach, CoolRunner CPLDs use true CMOS design technology. CoolRunner CPLDs are the first TotalCMOS CPLD, that is CMOS both in process technology and design technique. With the FZP CoolRunner approach represented in Figure 2, the AND gates in the product-term array are implemented using configurable multiplexers (MUXs) attached to the inputs of a normal CMOS NAND gate. Each MUX selects either the input, it's complement, or Vcc (don't care state.) These MUXs are programmed with configurations bits. The full CMOS AND gate shown in Figure 2 has a delay of under 0.5 ns, including the delay path of the MUXs.

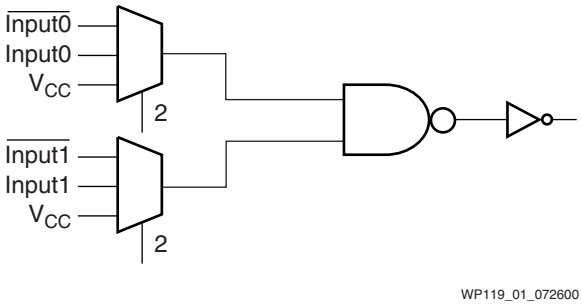

Figure 2: **CoolRunner FZP AND Gate**

Wider AND gates are built using a DeMorgan tree as shown in Figure 3. Doubling the input width simply requires the replacement of the inverter in Figure 2 with a 2-input NOR gate. This increases the total delay by less than 0.1 ns.

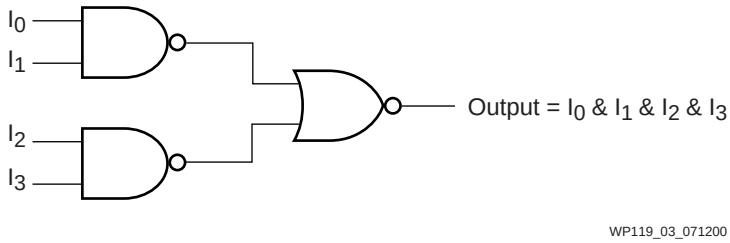

Figure 3: **4-Input Product Term Using FZP**

The FZP design technique can be extended for wider widths as shown in Figure 4, which shows an additional doubling to eight inputs. This adds an additional delay penalty of less than 0.3 ns for the NAND gate and inverter.

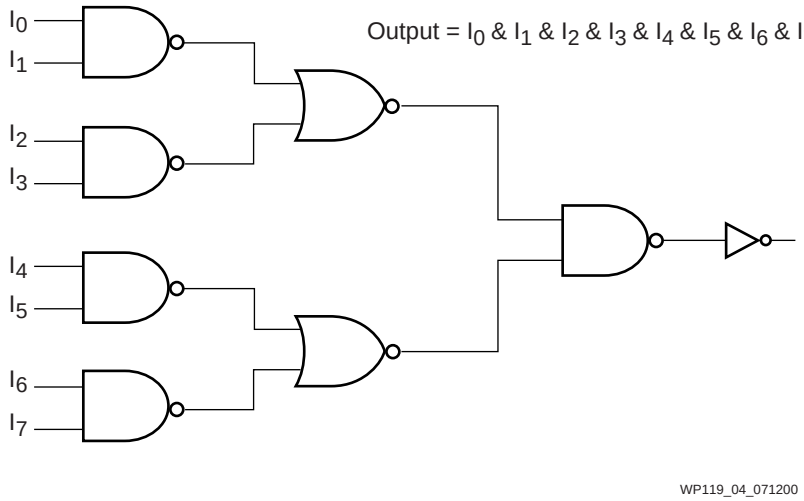

Figure 4: **Expanding to 8-input AND Function**

Expanding on this 8-input product term, the inverter shown in Figure 4 can be replaced with a 2-input NOR gate to enable a product term width of 16 inputs. With a product term width of 16 inputs, the delay penalty is only increased by 0.1 ns.

In the FZP design technique, the product term array is implemented by cascading the logic in a tree of full-CMOS gates. The delay penalty per additional input actually decreases as the number of inputs to each product term increases. Each CMOS gate switches in 200 picoseconds (ps), and the gates are cascaded in a way that achieves speed performance comparable to the sense amplifier approach in other CPLDs. Cascading the gates distributes the capacitance associated with the true and complement logic block inputs. The gate tree structure distributes the capacitance at each product term, so the capacitance is no longer lumped at a single node. By distributing the input capacitance for each product term the instantaneous I_{CC} is less compared with sense amplifiers.

Power Consumption

In the FZP design methodology, the switching current behaves in a manner similar to that of combinational logic in a gate array. The static current for each gate is small—about 1 femtoamp (fA). The total instantaneous dynamic current is also low, with only the gates in one path of the tree switching at a time. The gates in each path of the tree also switch in succession, rather than all at once, thus reducing peak dynamic current.

Total standby current for Xilinx CoolRunner CPLDs is under 100 microamps (µA)—1000 times less than that exhibited by CPLDs that use the sense amplifier approach. During dynamic operation, total power is also decreased relative to other CPLDs by as much as 70% for a device whose logic is fully-populated with 16-bit counters operating at f_{MAX}.

For more information on reducing power in CoolRunner CPLDs, see **http://www.xilinx.com/xapp/xapp346.pdf**.

Conclusion

The advantages of FZP are numerous. The power savings achieved with FZP can be realized with no impact on performance and no externally-controlled provisions, such as power-down circuitry. FZP is immune to noise that can affect sense amplifiers. Because power consumption is so low, chip-scale packaging options, once considered impossible due to thermal limits, are now available. As a result, FZP is an innovative technology for CPLDs, because it enables very low-power and high-performance applications.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/28/00	1.0	Initial Xilinx release.