CAST

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Features

- Independent and simultaneous access to two registers save machine cycles
- Eight function ALU
- Expandable – Any number of devices can be connected for wider bus structures
- Four status flags for Carry, Overflow, Zero and Negative
- Microprogrammable
- Functionality based on the Advanced Micro Devices AM2901

Applications

The C2901 core is used where simple microprogrammable controllers are required.

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF Netlist; .ngc VHDL/Verilog Source RTL available extra
Constraints File	C2901.ucf
Verification Tool	VHDL/Verilog test bench, test vectors
Instantiation Templates	None
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
1076 compliant VHDL simulator, Verilog simulator	
Support	
Support provided by CAST, Inc.	

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[2]	Clock IOBs	IOBs[1]	Performance (MHz)	Xilinx Tools	Special Features
Virtex	V50-6	143	1	44	36	M2.1i	None
Virtex-E	V50E-8	143	1	44	46	M2.1i	None
Spartan-II	2S50-6	143	1	44	36	M2.1i	None

Notes:
1. Assuming all core I/Os are routed off-chip.
2. Optimized for speed.

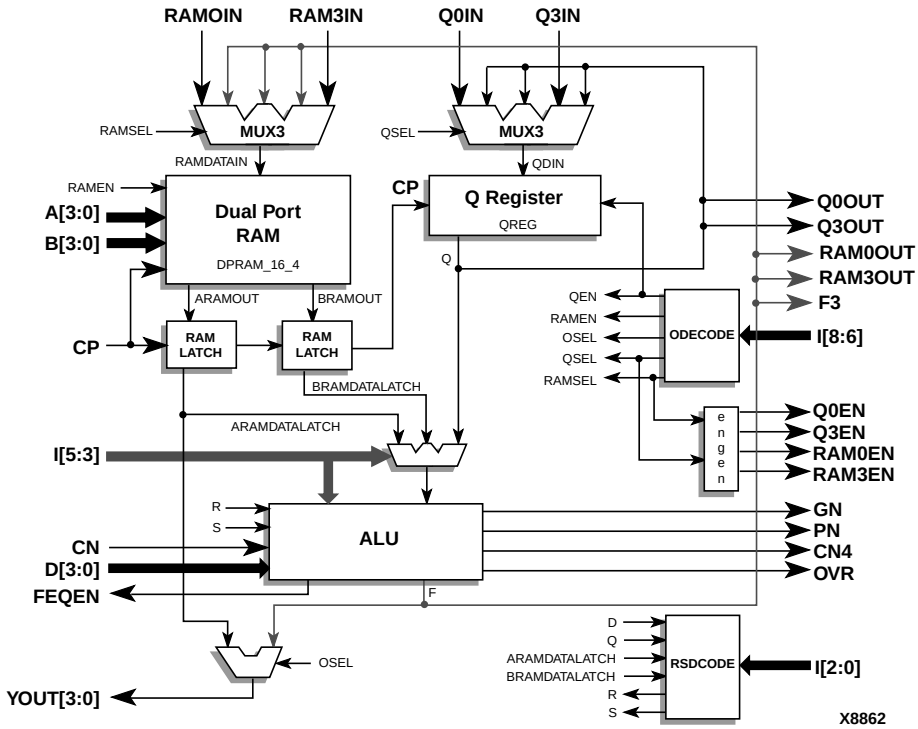

Figure 1: 2901 Microprocessor Slice Block Diagram

General Description

The C2901 4-bit microprocessor slice core is a cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The core includes a dual port RAM, ALU, shifter, register and multiplexer. The microinstructions of the C2901 allow for easy modeling of various microcontrollers.

Functional Description

The C2901 core is partitioned into sections as shown in Figure 1 and described below.

Dual Port RAM

The internal memory is a 4-bit by 16 deep Dual Port RAM. It is addressed for writing by the B Port and for reading by both the A and B Ports. The input data is defined by a microinstruction decoded from 3 bits of the 9-bit I Port.

RAM Latch

These latches store the outputs of the Dual Port RAM. They are clocked using the CP input.

Q Register

The Q register is enabled by the internal signal qen which is generated by the Instruction input (I) and clocked on the rising edge of CP.

ALU

The ALU accepts input from either RAM Port, the Q Register and cascaded inputs from previous stages. It has basic functions including most logic and arithmetic operations including such functions as shifting, adding and subtracting.

ODecode

The ODecode block takes bits 6 – 8 of the MicroInstruction Bus and uses them to control the internal output enables and selects of the other blocks.

RSDecode

The RSDecode block takes bits 0 – 2 of the MicroInstruction Bus and uses them to control the 4-bit R and S buses. These buses get loaded with the outputs of the other blocks, routing various results back through the ALU block.

ENGEN

This block takes the select bits for the ram and q register and decodes the enable pins for the bidirectional RAM and Q bits.

MicroInstructions

The I Port is internally decoded to define the flow of data to the above sections.

Core Modifications

The C2901 core can be customized to include:

- 4-bit Data width or greater
- Bi-directional pins as in the original AM2901 device

Please contact CAST, Inc. directly for any required modifications.

Pinout

The pinout of the C2901 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and in Table 2.

All bi-directional pins have been split to have input, output and enable pins associated with them. This is done to be in compliance with VSIA.

Verification Methods

The C2901 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original AMD 2901 chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Table 2: Core Signal Pinout

Name	Type	Description
A[3:0]	Input	A-port Address
B[3:0]	Input	B-port Address
CP	Input	Clock (Clock IOB)
CN	Input	Carry In
D[3:0]	Input	Data Input
FEQEN	Output	ALU outputs are zero (control for Open Collector Output)
OEN	Input	Output
YOUT[3:0]	Output	Data Output
RAM0IN	Input	Shift Line – RAM Stack
RAM3IN	Input	Shift Line – RAM Stack
Q0IN	Input	Shift Line-Q Register
Q3IN	Input	Shift Line-Q Register
Q0OUT	Output	Shift Line – Q Register
Q3OUT	Output	Shift Line-Q Register
RAM0OUT	Output	Shift Line – RAM Stack
RAM3OUT	Output	Shift Line – RAM Stack
F3	Output	ALU MSB
I[8:0]	Input	Instruction/Microcode
Q0EN	Output	Enable for Q0 Tristate Output
Q3EN	Output	Enable for Q3 Tristate Output
RAM0EN	Output	Enable for RAM0 Tristate Output
RAM3EN	Output	Enable for RAM3 Tristate Output
GN	Output	Carry Generate
PN	Output	Carry Propagate
CN4	Output	Carry out
OVR	Output	Overflow

Ordering Information

The C2901 core is available from CAST, Inc. Please contact CAST, Inc. directly for pricing and information.

Related Information

Bipolar Microprocessor Logic and Interface Data Book

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