DVB Satellite Modulator Core

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Features

- Supports Spartan™-II, Virtex™, and Virtex™-E devices
- Compatible with DVB standard
- Conforms to European Telecommunications Standard (ETSI) EN 300 421 v1.1.2
- Byte wide data path
- Test points at the output of each block and at the input to the Baseband Shaping block
- 204/188 Reed-Solomon Outer Coder
- Selectable convolutional code rates of: 1/2, 2/3, 3/4, 5/6, and 7/8
- Supports uncoded (1/1) operation
- DC to 45+ MHz symbol rate (R_S)
- DC to 70+ MHz bit rate (at 7/8 code rate). Supports SONET STS-1 bit rate at code rates of 7/8 down to 2/3
- Fully synchronous operation

Applications

- DVB Satellite Modulator
- Microwave Transmitter

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex
Device Tested	V50-4
CLBs	
Core	300
Core+Ext logic	300
Clock IOBs	1
IOBs Core[1]	146
Core+Ext logic	146
Performance (MHz)	45+[2]
Xilinx Core Tools	Alliance 1.5i
Special Features	Block RAM, Distributed RAM
Provided with Core	
Documentation	User's Guide
Design File Formats	Verilog Source RTL[3]
Constraints File	xfmoddvb.ucf
Verification	Verilog Testbench
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Application Note
Additional Items	None
Simulation Tool Used	
Silos III	
Support	
Support provided by Memec Design Services	

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.
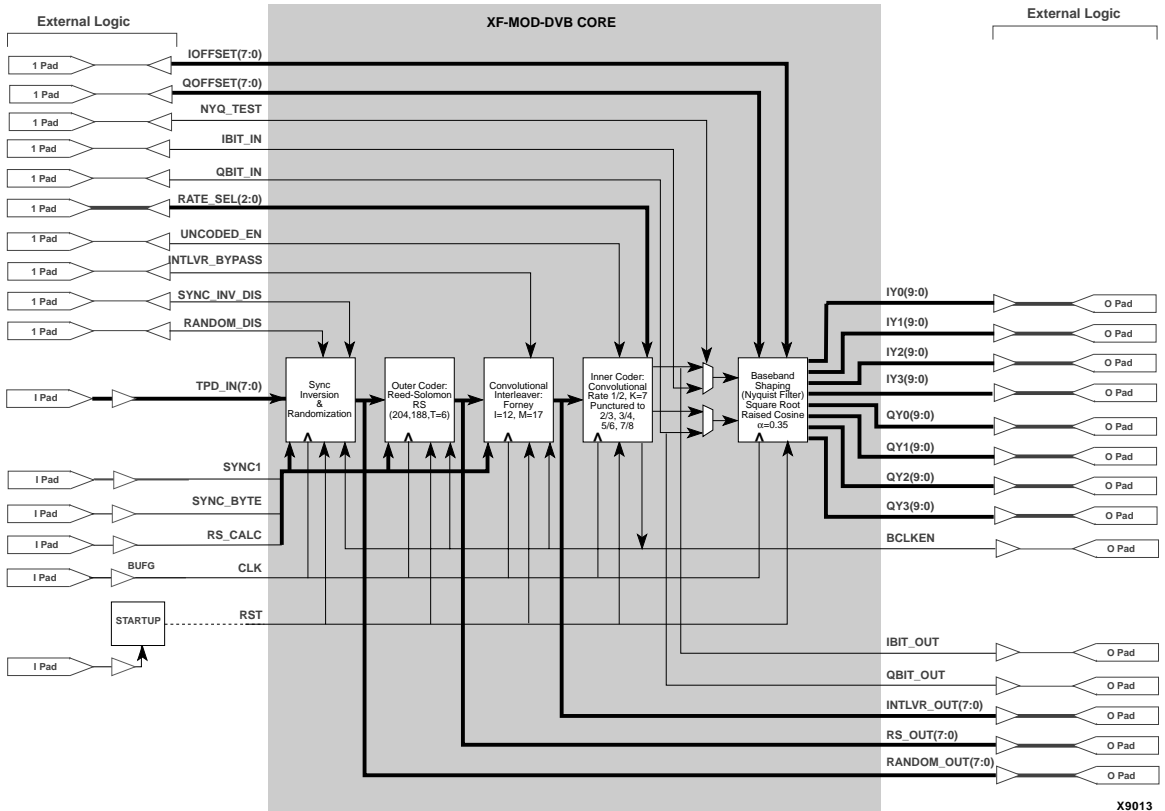3. Synplify 5.08A used for synthesis.

Figure 1:   Modulator Core Block Diagram

General Description

The XF-MOD-DVB is a "core" logic module specifically designed for Xilinx FPGAs that performs the digital baseband functions required for the transmit side of a DVB satellite link. It accepts MPEG-2 formatted transport packets as input and outputs filtered I/Q symbols suitable for digital to analog conversion and subsequent QPSK modulation. This core implements five of the functions required for a satellite channel adapter as described by the DVB standard ETSI EN 300 421 V1.1.2 and shown in Figure 1 of that standard. These functions are: Mux Adaptation & Energy Dispersal, Outer Coder, Convolutional Interleaver, Inner Coder, and Baseband Shaping. Figure 1 and Table 1 show the core's basic block diagram and signal list, respectively.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Compo-

nents, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inorder to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

Functional Description

Sync Inversion and Randomization

The Sync Inversion and Randomization block is the first processing block in the chain. It takes an MPEG-2 transport packet stream as input and produces a randomized data stream with every eighth sync byte inverted.

The DVB standard, ETSI document EN 300 421 v1.1.2, describes a data randomizer to "ensure adequate binary transitions". The randomizer is a pseudo random binary sequence (PRBS) generator whose output is XORed with the clear data stream on the transmitter side and with the randomized data on the receiver side. The PRBS polynomial is specified as: $1 + x^{14} + x^{15}$.

The DVB standard describes a procedure called "Transport Multiplex Adaptation". This is a fancy title for inverting the sync byte of the first transport packet in a group of eight packets. The sync byte of the first packet is bit-wise inverted from 0x47 to 0xb8, whereas the sync bytes of the next seven packets remain 0x47. During the inverted sync byte interval (SYNC 1), the PRBS generator is loaded with a seed value of "100101010000000". After the seed is loaded, the PRBS generator runs continuously through eight transport packets (8 packets * 188 bytes/packet – 1 byte period/load = 1,503 bytes). During all sync byte intervals, the PRBS output is disabled, leaving the sync bytes unrandomized.

Outer Coder

The Outer Coder block sits between the output of the Randomizer and the input to the Convolutional Inter-leaver in the processing chain. It is a Reed-Solomon encoder, RS(204, 188), that takes the 188-byte randomized transport packets as input and calculates 16 parity symbols (check bytes) which it appends to the end of each packet to produce 204-byte error protected packets as output.

The Reed-Solomon encoder implements the primitive polynomial, $P(x) = x^8 + x^4 + x^3 + x^2 + 1$, and generator polynomial, $G(x) = (x-a^0)(x-a^1)…(x-a^{15})$, over a Galois field of GF(256). This block is also available as a separate core from Memec Design Services, part number XF-RSENC-DVB.

Convolutional Interleaver

The Convolutional Interleaver block sits between the output of the Outer Coder and the input to the Inner Coder in the processing chain. It takes 204-byte Reed-Solomon error protected packets as input and produces 204-byte interleaved frames as output.

The interleaver is implemented with a block RAM and a special addressing mechanism to access the RAM as 12 delay pipes, each one 17 bytes deeper than the previous one. That is, the first delay pipe (branch 0) is 0 bytes deep (no delay), the second (branch 1) is 17 bytes deep, the third (branch 2) is 34 bytes, and the twelfth (branch 11) is 187 bytes. The total number of byte storage locations required is 1,122. The sync byte of each 204 byte packet is passed through branch 0 (the zero delay path) and is therefore passed straight through the interleaver without being written into the RAM. The next byte is written into branch 1, followed by branch 2, etc; each consecutive byte is written to the next branch. The branch ordering is, 0, 1, 2, … 10, 11, 0, 1, 2, …

Thus, the sequence repeats every 12 bytes. Note that the 204 byte packets are divisible by 12 (204/12 = 17) and therefore, sync byte will always pass through the zero delay path (branch 0).

See Figure 4 in the DVB standard, EN 300 421 V1.1.2, for a conceptual diagram of the operation.

Inner Coder

The Inner Coder block sits between the output of the Convolutional Interleaver and the input to the Baseband Shaping block in the processing chain. It takes bytes from the 204-byte interleaved frames as input and produces I/Q symbol pairs as output.

The Inner Coder performs three functions: convolutionally encodes input data; optionally punctures certain bits to obtain higher code rates; and serializes I/Q symbols to be transmitted. The convolutional encoder and puncturing logic can be disabled with the UNCODED_EN control input, in which case the block only serializes the I/Q symbols to be transmitted.

See Table 2 in the DVB standard, EN 300 421 V1.1.2, for the definition of punctured codes.

Baseband Shaping

The Baseband Shaping block is the last block in the processing chain. Its input comes from the Inner Coder and its output goes out of the core, typically through a parallel to serial stage and then to the digital to analog converters (DACs). It is basically two identical 4x interpolating polyphase FIR filters, one for I and one for Q. Each filter takes a 1-bit input stream and generates four 10-bit filtered output streams. The filtering operation spans 8 symbols.

Core Modifications

Customizing is available through Memec Design Services.

Pinout

The pinout of the DVB Satellite Modular Core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are provided in Table 2.

Verification Methods

Complete functional and timing simulation has been performed on the core using Silos III. Simulation vectors used for verification are provided with the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
IOFFSET[7:0]	Input	I-Channel DC Offset Control: This two's complement value is sign extended to ten bits and added to the output of each Nyquist (baseband shaping) filter LUT. The outputs of the LUTs have a maximum excursion of +/- 482. IOFFSET can safely take a value of +/- 29. Values greater than +/- 29 will cause the output of the adders to wrap, resulting in improper operation.
QOFFSET[7:0]	Input	Q-Channel DC Offset Control: Same as IOFFSET above, except this is added to the Q-channel Nyquist filter outputs.
NYQ_TEST	Input	Nyquist Filter Test: When asserted high, input to Baseband Shaping block (Nyquist filter) is sourced from external pins, IBIT_IN and QBIT_IN. This is a test mode used for system level testing, and alignment. When deasserted (normal operating mode), output of Inner Coder is source to Baseband Shaping block in normal operating mode.
IBIT_IN	Input	I-Channel Nyquist Filter test input: This test input is used when NYQ_TEST is asserted (see above). This input is ignored when NYQ_TEST is deasserted,
QBIT_IN	Input	Q-Channel Nyquist Filter test input: Similar to IBIT_IN but drives Q-Channel input to Nyquist filter.
RATE_SEL[2:0]	Input	Code Rate Select: These inputs select which of the five puncture patterns to apply to the output of the convolutional encoder. These inputs are encoded as shown in Table 2.
UNCODED_EN	Input	Uncoded (1/1) Enable: When asserted high, the convolutional encoder and puncturing logic are bypassed and the data bits are sent out in pairs on I_BIT and Q_BIT. This input is for test purposes and should be deasserted during normal operation.
INTLVR_BYPASS	Input	Interleaver Bypass Control: When asserted high, the Reed Solomon output (see RS_OUT below) passes directly to the input of the Convolutional Encoder. This input is for test purposes and should be deasserted during normal operation.
SYNC_INV_DIS	Input	Sync Inversion Disable Control: When asserted high, inversion of every eighth sync byte is disabled. This input is for test purposes and should be deasserted during normal operation.
RANDOM_DIS	Input	Randomizer Disable Control: When asserted high, the output of the PRBS generator is not XORed with the data stream. This input is for test purposes and should be deasserted during normal operation.
TPD_IN[7:0]	Input	Transport Packet Data In: This is byte wide MPEG-2 transport packet data. The first byte in every transport packet must be a sync byte (0x47).
SYNC1	Input	Sync Byte 1 Indicator: This signal is asserted high to indicate that the first sync byte in a group of eight packets is present on TPD_IN bus. This repeats every 1,504 bytes.
SYNC_BYTE	Input	Sync Byte Indicator: This signal is asserted high to indicate that a sync byte is present on TPD_IN bus. This repeats every 188 bytes.

Table 1: Core Signal Pinout (Contd)

Signal	Signal Direction	Description
RS_CALC	Input	Parity Calculate: This signal controls whether the Outer Coder block is calculating the parity (check bytes) or shifting them out. High = calculate, Low = shift. In DVB, this signal is high for the first 188 bytes of the packet, and low for 16 bytes. The Outer Coder block uses it to qualify on which clock cycles input data is processed; it is enabled for input data when RS_CALC and BCLKEN are both asserted.
CLK	Input	Clock input: The clock input to every register in the core. This clock is continuous and operates at the punctured symbol rate, R_s. One I/Q symbol pair is output on each rising edge.
RST	Input	Reset: Asynchronous reset to every register in the core.
IY0[9:0], IY1[9:0], IY2[9:0], IY3[9:0]	Output	I-Channel Nyquist Filter Out, phases 0-3: These are the outputs of an M=4 polyphase FIR filter. All four buses are updated once per symbol clock, CLK. External logic commutates values on these buses to I-channel DAC input at 4x the symbol rate. These values are in 10-bit offset-binary format. With IOFFSET=0 (see above), the buses can have a maximum excursion of 30 (0x01e) to 994 (0x3e2).
QY0[9:0], QY1[9:0], QY2[9:0], QY3[9:0]	Output	Q-Channel Nyquist Filter Out, phases 0-3: Same as the IYn_[9:0] outputs above, except these feed the Q-channel DAC.
BCLKEN	Output	Byte Clock Enable: This output is asserted high when puncturing logic needs the next byte. This enable qualifies clock input to all of the byte-wide blocks. .
IBIT_OUT	Output	I Channel Output Bit (Test Point): The punctured result of X output (171_{OCT}) of the convolutional encoder.
QBIT_OUT	Output	Q Channel Output Bit (Test Point): The punctured result of Y output (133_{OCT}) of the convolutional encoder.
INTLVR_OUT[7:0]	Output	Interleaved Frame Data Out (Test Point): This data is formatted as shown in figure 3d of DVB standard, EN 300 421.
RS_OUT[7:0]	Output	Reed Solomon Output (Test Point): The 204-byte error protected packets output here. First 188 bytes of the packets are randomized packet data (see RANDOM_OUT above) and the last 16 bytes are the Reed-Solomon check bytes. See Figure 3c in DVB standard, EN 300 421.
RANDOM_OUT[7:0]	Output	Randomized Packet Data (Test Point): Randomized transport packets output here. The first sync byte in a group of eight packets is inverted (0xb8), the remaining seven sync bytes are unchanged (0x47), and all of the 187-byte payloads are randomized. See Figure 3b in the DVB standard, EN 300 421.

Table 2: Selection of Puncturing with RATE_SEL[2:0]

UNCODED_EN	RATE_SEL[2:0]	Puncturing
0	000	None (1/2)
0	001	2/3
0	010	3/4
0	011	5/6
0	100	7/8
0	101	reserved
0	110	reserved
0	111	reserved
1	xxx	1/1 Uncoded

Recommended Design Experience

For the source code version, users should be familiar with Verilog HDL entry, synthesis, simulation, and Xilinx design flows.

Ordering Information

The DVB Satellite Modulator Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Ser-

Related Information

European Standard EN 300 421 v1.1.2, *Digital Video Broadcasting (DVB); Framing Structure, Channel Coding, and Modulation for 11/12 GHz Services*, France: European Telecommunications Standards Institute (ETSI), 1997.

AllianceCORE™ data sheet, *XF-RSENC Reed-Solomon Encoder*, November 9, 1998, Xilinx Inc.

Xilinx Programmable Logic

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