



Microprocessor Based Core Evaluation Card

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Product Specification



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Features

- Microprocessor based IP Core evaluation card
- i486DX™ based system, supporting both +5V and +3.3V CPU's with selectable clock speeds up to 50MHz
- Single XC95216 system control CPLD with integrated NMI DRAM Controller Core
- XC4000XL site available as a dedicated memory controller (in place of the XC95216)
- Single, industry standard 72 pin SIMM DRAM memory connector
 - Configurable for SDRAM operation with custom NMI module
- Parallel connected XC95216 and XC4000E available for general purpose I/O core integration:
 - Connected to full 32 bit i486DX™ bus
 - RS232 port connection
 - PC-compatible parallel port connection
 - I²C master/slave controller connection
 - General purpose pin strip header connection
- XC9500 parts programmable in-circuit via JTAG chain



Figure 1: Microprocessor Based Core Evaluation Card

- XC4000 parts programmable in-circuit via either programming cable or directly from the system CPU
- System support devices include boot EPROM and/or Flash EPROM, SRAM and serial port
- Full featured debug monitor facilitates thorough evaluation and test of cores
- Operates from single +8V to +20V DC input

General Description

NMI's AllianceCORE™ Evaluation Card is intended to allow developers to quickly evaluate the functionality of CPU peripheral and memory controller cores. Developers can also test, using real target hardware, modifications to the cores and/or their own peripheral logic. This increases confidence that user designs will be fully functional when integrated into the final target hardware platform.

Functional Description

The Evaluation Card's host CPU is i486DX™ and both +5V (e.g. i486DX™ and i486DX2™) and +3.3V (e.g. i486DX4™) versions of the CPU are supported. CPU operating voltage is auto-sensed using the standard Intel 486DX4™ mechanism.

The i486DX™ has a general purpose, high speed synchronous bus and this allows developers to easily migrate designs to other microprocessor or system interfaces. The bus clock speed can be set to a number of frequencies ranging from 16MHz to 66MHz (although the Intel 486DX4™ is limited to 50MHz maximum). The bus clock is distributed using individual, low skew (PLL controlled) clock drivers to the CPU and each of the Xilinx PLD's.

The XC95216 system controller CPLD is the only required PLD device as it provides all of the basic CPU state and address decoding. NMI's AllianceCORE DRAM Controller can also be integrated into this device, providing the board with increased memory resources. The CPU has a central resource of boot EPROM, Flash EPROM, SRAM and RS232 serial port with which it can run its built in debug and test monitor.

An optional XC4KXL device can be used to provide the memory controller function instead of the XC95216 (the XC95216 is still required in the system though). A single, industry standard 72 pin DRAM SIMM connector is provided on the board, allowing the use of any standard SIMM module with either one or two banks of DRAM. The SIMM power supply can be set to either +3.3V or +5V. A single configuration jumper also allows the bus clock to be routed to a no connect pin on the SIMM connector, allowing custom Synchronous DRAM SIMM modules to be used also.

Two (optional) peripheral controller PLD's are also provided on the board: an XC95216-HQ208 and an XC4KE-HQ240. The devices are effectively connected in parallel, with one

side each connected to the full i486DX™ system bus, the other side connected to some general purpose I/O. Both devices employ +5V I/O buffers.

The general purpose I/O consists of:

- A full 9 pin RS232 serial port (level translators provided)
- A PC parallel port (ESD protection provided)
- A separate, Philips Semiconductors I²C master/slave controller
- Pin headers (16 off)
- Two LED's

The board is provided with a full featured debug monitor which has been optimized for debugging and testing hardware. The monitor includes:

- Standard memory and I/O display and modification commands.
- Assembly language coded fill and test commands which ensure maximum CPU bandwidth utilization of memory. These commands are very useful for stress testing designs.
- Software assembler and disassembler (80186 instruction set).
- File transfer via the serial port. Includes binary format plus Intel HEX and Microsoft EXE program loaders.
- Basic DOS INT 21 emulator to ease user test software development.
- Built in macro language.

The two XC95216 devices are configured in a single JTAG chain and can easily be programmed using the XACTstep M1 JTAG CPLD Programmer software. The two XC4K devices can be programmed using asynchronous peripheral mode via the debug monitor; alternatively each device is provided with a separate serial download cable connection.

The Evaluation Card is powered from a single, +8V to +20V DC input. Switched-mode power converters are used, resulting in low heat dissipation by the board (other than by the CPU). The power supplies are protected against input voltage reversal.

The Evaluation Card will be CE approved by NMI.

Available Support Products

NMI will develop a Synchronous DRAM SIMM module which will be compatible with the Evaluation Card and this will be available, at additional cost, in the near future.

Ordering Information

To make further enquiries or purchase the Core Evaluation Card, please contact NMI directly at the location detailed on the front page. NMI also offers core products and design services, the latter covering not only CPLD and FPGA design but also complete systems design.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm
