200 MHz SDRAM Controller Core

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Features

- Supports 4000X, Spartan™-II, Virtex™, and Virtex™-E devices
- World's fastest FPGA SDRAM interface. 200MHz.
- Works with SDRAM or SGRAM. Currently 19 bit. address (512K), 32 bit data, but modifiable.
- Uses Auto-precharge mode with a CAS latency of 3 cycles and linear bursts of length 4.
- Bursts may be aborted for fewer than 4 words.
- Supports 2 or 4 SDRAM banks.
- Provides 4 commands
  - Mode Register Write
  - Burst Write
  - Burst Read
  - Refresh (manual)
- Automatic refresh occurs 15.6µs after the last manual or automatic refresh.
- Manual refresh can be used to ensure continuous SDRAM availability for 15.6µs.
- Throughput of up to 6.4 Gbits/sec per memory chip.

AllianceCORE™ Facts

Core Specifics		
Supported Family	4000XL/XLA	Virtex
Device Tested	4013XL/A	V100-6
CLB Slices	62	129
Clock IOBs	4	1
IOBs[1]	53+92	53+92
Performance (MHz)	200	200
Xilinx Tools	1.5i	1.5i
Special Features	1 BUFG 3 BUFGE 2 BUFGLS 1 OSC	1 DLL
Provided with Core		
Documentation	User guide, Design guide, ViewSim .vwf files	
Design File Formats	EDIF netlist	
Constraints File	sdram_controller.ucf	
Verification	Functional and timing simulation (with .cmd files), Hardware testing on FastRAM board	
Instantiation Templates	VHDL, Verilog, Viewlogic symbol	
Reference designs & application notes	None	
Additional Items	Demo board available extra	
Simulation Tool Used		
Viewlogic ViewSim 7.4		
Support		
Support provided by Rapid Prototypes Inc. 90 days email and telephone support (not including user modifications) included in core price.		

Applications

- Real-time image processing applications
- High performance reconfigurable computing
- High performance digital signal processing
- Realtime video processing
- Digital neural networks
- Algorithmic research
- PC peripherals
- Digital video

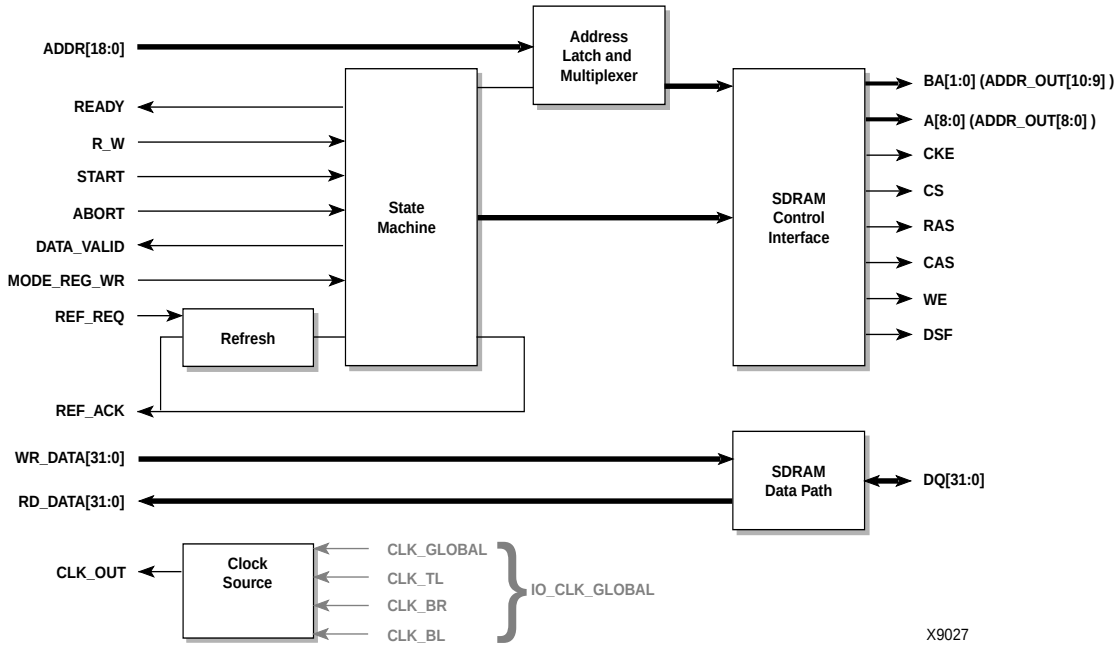

Figure 1: SDRAM Controller Block Diagram

General Description

The SDRAM controller provides a static-RAM-like interface to synchronous dynamic RAMs, for use by application circuits within the remainder of the FPGA or external to it.

200MHz operation was achieved by floor-planning and using multiple fast BUFGE and BUFGLS clocks. So the design is pin-locked to 0FP 240 package relative to the SDRAM and clocks but modifications are possible.

The SDRAM controller is supplied as an EDIF netlist and constraint files, with VHDL and Verilog templates and a Viewlogic symbol file.

The core is currently available for 4000XL/XLA, and Virtex FPGAs.

Functional Description

The SDRAM Controller is partitioned into modules as shown in Figure 1 and described below.

State Machine

In response to requests on its START, ABORT, MODE_REG_WR and internal ref_req inputs, the State Machine sends the required sequence of commands and addresses to the SDRAM Control Interface. The direction of data transfer is determined by the state of R_W when START is asserted. Commands are only accepted when the READY output is asserted. When reading from the SDRAM, the DATA_VALID output is asserted when valid data is on the RD_DATA bus.

Address Latch and Multiplexer

The Address Latch and Multiplexer takes the full 19 bit address and under the control of the State Machine passes the bank address and either the row address or the column address and auto-precharge bit to the SDRAM Control Interface at the appropriate time.

SDRAM Control Interface

The SDRAM Control Interface provides the appropriate timing and drive to the address and control pins of the SDRAM.

Refresh

The Refresh unit issues a refresh request to the State Machine 15.6 us after the last refresh, whether it was manual or automatic. It accepts manual refresh requests on the REF_REQ input. The State Machine acknowledges receipt of a refresh request by pulsing the REF_ACK output.

SDRAM Data Path

The Data Path unit handles the direction of data flow and provides the appropriate drive and timing to and from the SDRAM data (DQ) pins. It also maintains zeros on the SDRAM data mask (DQM) pins.

Clock Source

The Clock Source takes four copies of the (200MHz) clock from four FPGA pins, buffers them and supplies them (not shown) to various parts of the SDRAM controller. It is the physical layout of these clocks and the circuits they drive, that allows the controller to operate at 200MHz. The Clock Source also provides a clock to other circuitry within the FPGA, via CLK_OUT.

External to the FPGA, a fifth copy of the clock must be fed to the CLK input of the SDRAM.

Core Modifications

The SDRAM core can be modified to unlock the pin locations, but will result in slower performance than the basic core. The design is matched to the QFP 240 packages. Cores for other packages can be provided for an additional fee.

Rapid Prototypes will contract to modify the core to your specifications. We regret that Rapid Prototypes cannot provide support for user modifications.

Pinout

The pinout of the SDRAM Controller is described in Table 1. The SDRAM signals are padded and part of the core.

The SDRAM signals connect to the FPGA via suitable terminations. You will find more detail on these in the datasheet for any SDRAM or SGRAM. e.g. MoSys® MG802C512.

Verification Methods

Functional simulation has been carried out using ViewSim from Viewlogic's Workview Office™ version 7.4. Static timing analysis has been carried out for all paths using the Xilinx 1.5i tools. Hardware testing has been carried out at 200 MHz using the FastRAM board which Rapid Prototypes developed for Xilinx.

Recommended Design Experience

Users should be familiar with Xilinx design flows and their chosen design entry format (schematic or HDL). They should also be familiar with PCB layout considerations for operation at 200MHz, including microstrip transmission lines, termination techniques, high-frequency power supply decoupling and parasitic capacitance minimization.

Available Support Products

The FastRAM demo board is available from Rapid Prototypes, Inc. This board demonstrates the SDRAM core operating at 200 MHz and 800 MBytes/sec peak.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Application Signals		
ADDR[18:0]	Input	SDRAM address (demultiplexed)
READY	Output	Controller is ready for data transfer (reading or writing data)
R_W	Input	Direction of data transfer to be initiated by START
START	Input	Initiate data transfer if READY
ABORT	Input	Aborts a write command to allow writing of less than 4 words
DATA_VALID	Output	Read data is on the bus
MODE_REG_WR	Input	Write ADDR[17:9] to the SDRAM mode register
REF_REQ	Input	Perform an early refresh now so as to leave 15.6µs clear for data transfers
REF_ACK	Output	Acknowledge for REF_REQ
WR_DATA[31:0]	Input	Data bus from application to SDRAM
RD_DATA[31:0]	Output	Data bus from SDRAM to application
CLK_OUT	Output	The system clock out. The clock source is internal to the controller
SDRAM Signals		
BA[1:0]	Output	SDRAM bank address (ADDR_OUT[10:9]). LOC'ed to specific pad
A[8:0]	Output	SDRAM address (multiplexed, ADDR_OUT[8:0]). LOC'ed to specific pad
CKE	Output	SDRAM clock enable (always high). LOC'ed to specific pad

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
CS	Output	SDRAM chip select. Loc'ed to specific pad
RAS	Output	SDRAM row address strobe
CAS	Output	SDRAM column address strobe. LOC'ed to specific pad
WE	Output	SDRAM write enable. LOC'ed to specific pad
DSF	Output	Special function selector for SGRAM (always low). LOC'ed to specific pad
DQM[3:0]	Output	SDRAM data mask bits (always low). LOC'ed to specific pad
DQ[31:0]	In/Out	Perform an early refresh now so as to leave 15µs clear for data transfers. LOC'ed to specific pad
Clock Signals		
CLK_GLOBAL	Input	Clock for reading SDRAM and general use. Only in 4000XL/XLA
CLK_TL	Input	Clock to top left of FPGA. Only in 4000XL/XLA
CLK_BR	Input	Clock to bottom right of FPGA. Only in 4000XL/XLA
CLK_BL	Input	Clock to bottom left of FPGA. Only in 4000XL/XLA
IO_CLK_GLOBAL	Input	Clock signal in Virtex core

Ordering Information

To make further inquiries or purchase the SDRAM Controller Core contact Rapid Prototypes Inc. directly. Rapid Prototypes Inc. retains the right to make changes to these specifications at any time, without notice. All trademarks, registered trademarks, or servicemarks are the property of their respective owners. Contact Rapid Prototypes for more information on this or other company products.

Related Information

Xilinx Programmable Logic

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