M16550A - Universal Asynchronous Receiver/Transmitter With FIFOs

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Features

- Complete asynchronous communication protocol includes:
  - 5, 6, 7 or 8 bit data transmission
  - Even/odd or no parity bit generation and detection.
  - Start and stop bit generation and detection.
  - Line break detection and generation.
  - Receiver overrun and framing errors detection
- Communications rates of up to 56K baud
- Internal programmable baud rate generator
- Buffered transmit and receive registers
- Exception handling using interrupt/polled modes
- Two Modes of operation - NS16450 and FIFO mode
- Transmitter is buffered with 16 Byte FIFO
- Receiver is buffered with 16 Byte FIFO plus 3 error bits per data byte
- Internal diagnostic capabilities with loopback
- Modem handshake capability using CTS, RTS, DSR, DTR, RI and DCD signals
- Complete status reporting Capabilities
- Line break generation and detection

Applications

- Serial Communication Port
- Modem Interface Port

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000E
CLBs Used	359	359
IOBs Used	38[1]	38[1]
System Clock fmax	16 MHz	16 MHz
Device Features Used	Global Buffers	

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS40 PQ240-3	155	425
XC4020E HQ240-2	155	425

Provided with Core	
Documentation	Core Design Document FPGA Design Document
Design File Formats	NGD or XNF netlist Verilog Source RTL (available extra)
Constraint Files	.cst file, xactinit.dat.
Verification Tool	Test Vectors
Schematic Symbols	None
Evaluation Model	None
Reference designs & application notes	FPGA Design Document
Additional Items	Evaluation Board available extra

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Verilog RTL/Verilog XL simulator

Support
Support provided by Virtual IP Group, Inc.

Note:
1. Assuming all core signals are routed off-chip.

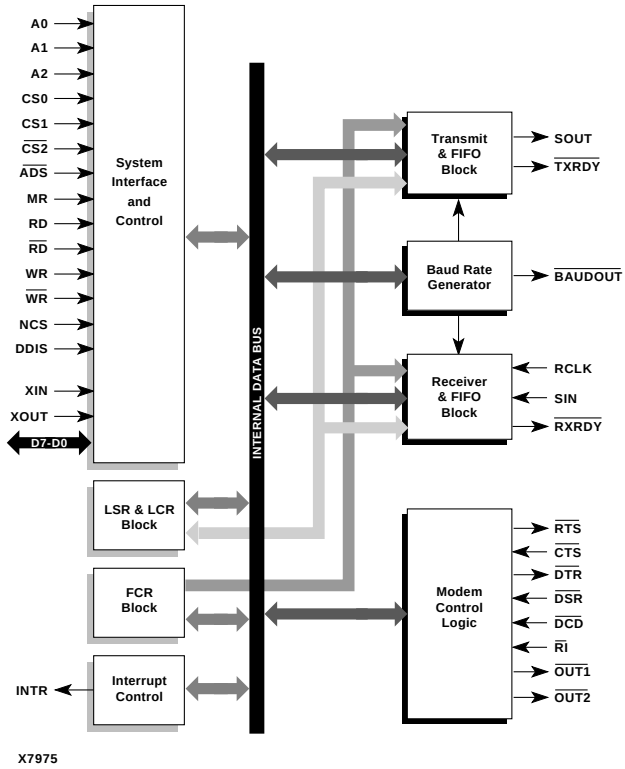

Figure 1: M16550A Block Diagram

General Description

The M16550A interfaces with a microcontroller or microprocessor on one side and serial communications equipment on the other. It provides full modem control through easy handshaking with modems during communication. Internal registers provide full programmability of serial asynchronous communication parameters. It also implements exception detection and reporting to the processor using interrupt or polled modes. The communication line and modem status can be monitored at any time by the processor by reading appropriate registers in the core.

Functional Description

This core emulates the functionality of National Semiconductor's NS16550A. The block diagram with internal structure is shown in Figure 1.

System Interface and Control Block

This block supports the processor interface and generates the internal system level signals for proper functioning.

LSR and LCR Block

This block holds the Line Status and Line Control Registers. These two registers control serial communication capabilities of the core.

FCR Block

This block has the FIFO control register which controls the parameters for the transmit and receive FIFOs.

Interrupt Control Block

This block handles all interrupt capabilities for the core.

Transmit and FIFO Block

This block holds the transmitter section and a 16-byte transmit FIFO.

Baud Rate Generator Block

This block generates the Baud Rate Clock for the transmitter section of the core. This clock can also be used by the receiver block by connecting $\overline{\text{BAUDOUT}}$ to RCLK

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
System Interface Signals		
A0, A1, A2	Input	Address signals to select an internal register for read/ write operations.
CS0-2	Input	Chip Select. CS0 and CS1 are active high, CS2 is active low.
ADS	Input	Address Strobe. Chip Select, and address signals are latched internally on rising edge of $\overline{ADS}$. Pulled low if unused.
MR	Input	Master Reset Signal, active high.
RD	Input	Control, active high. Pulled low if unused.
$\overline{RD}$	Input	Control, active low. Pulled high if unused.
WR	Input	Control, active high. Pulled low if unused.
$\overline{WR}$	Input	Write Control, active low. Pulled high if unused.
DDIS	Output	**D**river **DIS**able signal, driven low, when core outputs data. Used to control data flow direction intransceiver, or tristate buffers enable control.
CSOUT	Output	Indicates read/write selection of UART, active high and remains high when UART is selected through chip select inputs.
XIN	Input	Master clock input.
XOUT	Input	Master clock output, inverted from XIN.
D7 - D0	In/Out	Bidirectional databus carries data to be written to internal registers; also reports status of registers during read cycle.
Modem Interface Signals		
$\overline{RTS}$	Output	Active low **R**EQUEST **T**O **S**END indicates UART is ready to exchange data. System controls this pin through bit in modem control register.
$\overline{CTS}$	Input	Active low **C**LEAR **T**O **S**END indicates modem is ready to exchange data. Present state monitored by reading MSR.
$\overline{DTR}$	Output	Active low **D**ATA **T**ERMINAL **R**EADY tells modem that UART is ready to establish communication link. System controls this pin by programming a bit in MSR.
$\overline{DSR}$	Input	Active low **D**ATA **S**ET **R**EADY indicates modem is ready to handshake with core. Present state monitored by reading MSR.
$\overline{DCD}$	Input	Active low **D**ATA **C**ARRIER **D**ETECT indicates modem has detected carrier on communications line. Present state monitored by reading MSR.
$\overline{RI}$	Input	Active low **R**ING **I**NDICATOR indicates modem has detected ring signal. Present state monitored by reading MSR.
OUT1-2	Output	General purpose outputs. System controls these pins by through bit in MSR.
Transmit/Receive Signals		
SOUT	Output	Serial data output from transmitter block.
RCLK	Input	Input receive clock, should be 16 times communications baud rate.
SIN	Input	Serial data input for receiver block.
Other Signals		
INTR	Output	Active high interrupt signal.
BAUDOUT	Output	Baud rate generator output clock.16 times the programmed communication baud rate.

Receiver and FIFO Block

This block handles reception for the core. The clock for this block is provided by RCLK. This clock should be 16X the Baud Rate. The receive data FIFO is included in this block which stores 16 bytes at a time. The 16 bit FIFO's for status parameters (parity, framing and break) for the corresponding bytes in the receiver data FIFO is also included in this block.

Modem Control Logic Block

This block handles the modem control capabilities for the megacell core. These signals can be used for the communication purpose also some of the signals can be used as general purpose signals ($\overline{OUT1}$ and $\overline{OUT2}$). The modem control register resides in this block which provides the internal diagnostic capability for the core.

Core Modifications

Modifications can be done to remove the internal baud rate generator, or strip off either transmitter or receiver or size the FIFO of Transmitter and Receiver separately. These modifications can be performed by Virtual IP Group, Inc. for additional cost.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the users application. The evaluation board pinout, however has been fixed. This information is included in the design documentation. Signal names are provided in the block diagram shown in Figure 1 and Table 1.

Verification Methods

The core has been tested with in-house developed simulation test vectors that are provided with the core. Assembly level 80x86 programs were used to test the functionality of the FPGA in hardware.

Recommended Design Experience

Knowledge of interface with Microprocessor based systems is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment. Usage of Alliance or Foundation tools is required.

Available Support Products

The FPGA Design Document included with the core gives directions of constructing a general purpose FPGA evaluation daughter board that can be plugged in to a standard port socket on the target system through a flat cable.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Refer to Specification Document for programming of this core for a typical application in a system. The user is required to refer to Designer's application note for integrating this core with other cores.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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