X_DCT_IDCT Forward and Inverse Discrete Cosine Transform

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Features

- Supports Virtex, Virtex™-E, and Spartan™-II devices
- X_DCT_IDCT supports both DCT and IDCT on an 8x8 block of samples
- DCT and IDCT operations performed at one clock/sample
- DCT input precision 8 bits; output precision 12 bits
- IDCT input precision 12 bits; output precision 8 bits
- Suitable for JPEG, MPEG, H261 designs
- Fully synchronous design
- Test benches provided

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Product Datasheet Programmer's Guide
Design File Formats	EDIF netlist
Constraints File	dctchip.ucf
Verification	Testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference Designs and Application Notes	None
Additional Items	None
Simulation Tool Used	
ModelSim 5.3b	
Support	
Provided by Xentec, Inc.	

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices		Clock IOBs[1]		IOBs[1]		Performance (MHz)		Xilinx Tools	Special Features
		DCT_IDCT	DCT only	DCT_IDCT	DCT only	DCT_IDCT	DCT only	DCT_IDCT	DCT only		
Spartan-II	2CS100-6	1027	912	1	1	28	25	29	38	M2.1i	Block RAM
Virtex-E	V100E-8	1027	912	1	1	28	25	36	47	M2.1i	Block RAM
Virtex	V100-6	1140	943	1	1	28	25	32	38	M2.1i	Block RAM

Notes:
1. Assuming all core I/Os are routed off-chip

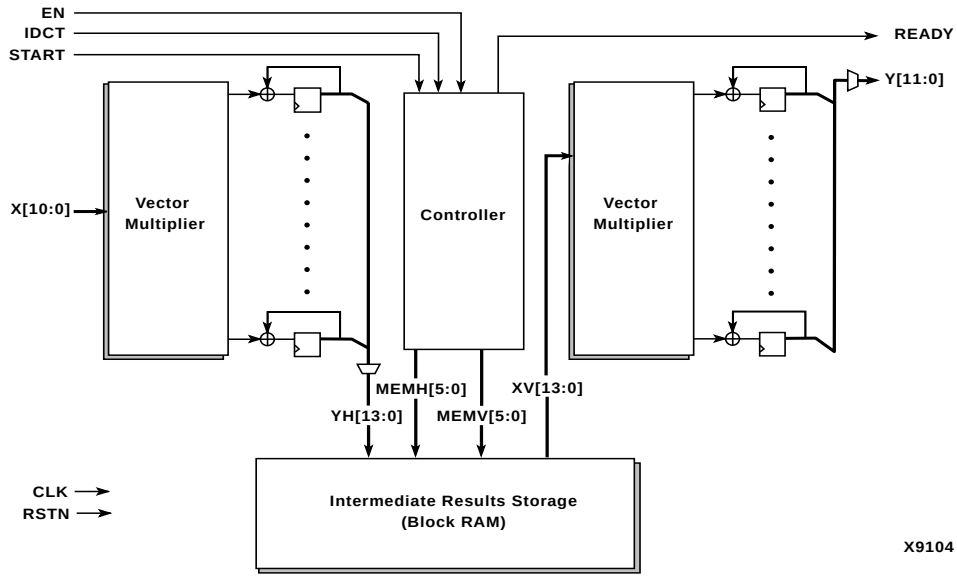


Figure 1: X_DCT_IDCT Transform Block Diagram

Applications

X_DCT_IDCT is a typical building block for image processing, printers, desktop video editing, digital still cameras, surveillance systems, and video conferencing cores.

General Description

X_DCT_IDCT can perform the two dimensional Discrete Cosine Transform (DCT) and its inverse (IDCT) on an 8x8 block of samples. The simple, fully synchronous design allows for fast operation while maintaining a low gate count. It offers high performance and many features to meet your multimedia, digital video and digital printing applications.

Functional Description

This core can perform both Discrete Cosine Transform (DCT) and its inverse (IDCT) on an 8X8 block of samples. The mathematical definition for the DCT and IDCT are shown below.

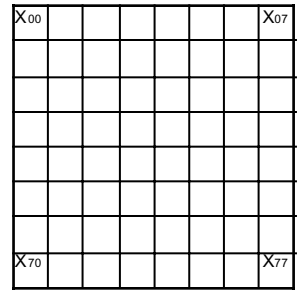
$$Y_{uv} = \frac{1}{4} CuCv \sum_{i=0}^{7} \sum_{j=0}^{7} X_{ij} \cos\frac{(2i+1)u\pi}{16} \cos\frac{(2j+1)}{16} v\pi$$

$$Y_{uv} + \frac{1}{4} \sum_{u=0}^{7} \sum_{v=0}^{7} C_u C_v Y_{uv} \cos\frac{(2i+1)u\pi}{16} \cos\frac{(2j+1)}{16} v\pi$$

Where $C_u = C_v = 1/\sqrt{2}$ for u, v=0,

and $C_u = C_v = 1$ otherwise.

Input samples are provided to the *X* port, while transformation results are available from port *Y*. If we consider a block of samples as shown below, the input port *X* accepts rows of samples. This means that input samples are to be provided in the order X_{00}, X_{01}, ... , X_{07},



X_{10}, ... , X_{70}, ... , X_{77}. Port Y outputs transformed samples as columns (i.e. Y_{00}, Y_{10}, ... , Y_{70}, Y_{01}, ... , Y_{07}, ... , Y_{77}) after a latency period of 64 clock cycles.

Port Y outputs transformed samples as columns (i.e. Y_{00}, Y_{10}, ... , Y_{70}, Y_{01}, ... , Y_{07}, ... , Y_{77}) after a latency period of 64 clock cycles.

A clock cycle wide pulse on the START input indicates the very first sample X00 of a series of blocks that need to be transformed.

The idct pin selects the type of transform to be performed on the input samples, DCT or IDCT. This input must be stable from the input sample X_{00} to at least the output sample Y_{77}.

Pinout

The pinout of the X_DCT_IDCT core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation has been performed, using the Model Technology ModelSim simulator. Test vectors and the test bench used for design verification are provided with the core.

Recommended Design Experience

A basic understanding of digital signal processing algorithms and DCT/IDCT is suggested. Users should be familiar with Verilog or VHDL synthesis and simulation and Xilinx design flows as well.

Ordering Information

The X_DCT_IDCT core is provided under license by Xentec for use in Xilinx programmable logic devices. RTL synthesizable source code is also available. Please contact Xentec for information about pricing, terms, and conditions of sale.

Xentec reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
EN	Input	Enable
IDCT	Input	IDCT selector: idct=0, DCT operation idct=1, IDCT operation
START	Input	Indicator of the 1st sample in the input block
X[10:0]	Input	Input data
CLK	Input	System clock
RSTN	Input	Asynchronous system reset
READY	Output	Indicator of the 1st sample in the output block
Y[11:0]	Output	Output data

Related Information

Xilinx Programmable Logic

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