Constant Coefficient Multiplier (Pipelined)

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Features

- Pipelined construction for increased throughput
- Multiplies a variable **A** times a constant **B**
- The **A** value can range from 4 to 32 bits
- The **B** value can range from 2 to 26 bits
- Independent **A** and **B** word size
- Independent selection of signed and unsigned data format for each operand
- Full precision output
- Supports 2's complement signed and unsigned magnitude numbers
- The inputs are not registered, but the outputs are registered
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This parameterized module multiplies an N-bit wide variable times an M-bit fixed coefficient and produces an N+M bit result. The coefficient multiplication tables are stored in distributed ROM-based look-up tables (LUTs), taking advantage of the FPGA look-up table architecture. It is an efficient, high speed, parallel implementation.

The variable and constant bit widths can be set independently, allowing the user to multiply different word widths together. The module automatically adjusts the signed and unsigned data to properly handle different sizes.

The variable and constant can be independently selected to be 2's complement signed or unsigned magnitude-only values. Note that the module will automatically handle a signed times an unsigned number, two signed numbers, or two unsigned numbers.

The Constant Coefficient Multiplier (KCM) is used where the value of an incoming variable needs to be multiplied by a number that does not change, a constant. This is often the case in scaling functions, FIR filters, IIR filters, etc.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

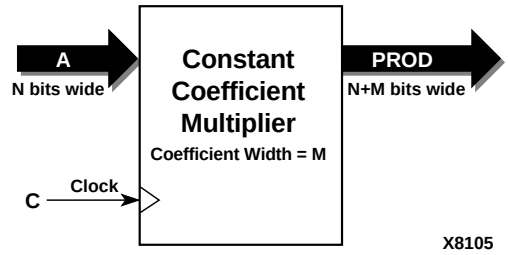

Figure 1: Block Diagram

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	PARALLEL DATA IN – A operand.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
PROD[m+n+1:0]	Output	PARALLEL DATA OUT - product result.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **A Width**: Select an input bit width from the pull-down

menu for the variable width. The valid range is 4 to 32.

- **Signed Input Data**: Set the sign of the variable to Signed or Unsigned.
- **Coefficient Width**: Select an input bit width from the pull-down menu for the constant width. The valid range is 2 to 26.
- **Coefficient**: Enter the value of the desired constant.
- **Signed Coefficient**: Set the sign of the constant to Signed or Unsigned.
- **Radix**: Hexadecimal or Decimal representation of the constant.

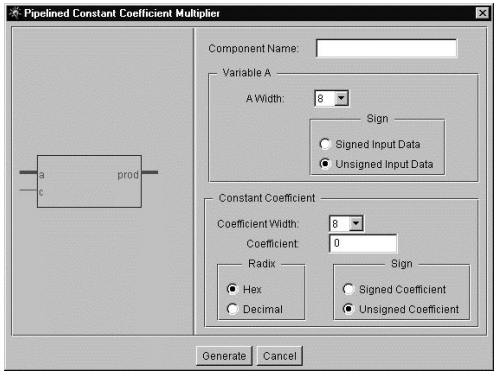

Figure 2: Parameterization Window

Multiplier Latency

The total latency (number of clocks required to get the first output) is a function of the width of variable **A**. Table 2 shows the latency for the possible bit widths of **A**.

Table 2: Multiplier Latency

A Data Width	Latency (# Clocks)
4 to 5 bits	1
6 to 10 bits	2
11 to 17 bits	3
18 to 32 bits	4

Core Resource Utilization

Table 3 shows the resource utilization for some available bit widths.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Table 3: Constant Coefficient Multiplier Characterization Table

A Width	B Width	CLB Count	Area Required for RPM (Rows, Columns)	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan -4 (Advanced) MHz
4	4	4	4,1		228	152	175
4	8	6	6,1		210	147	170
4	16	10	10,1		169	118	141
4	20	12	12,1		172	120	131
4	24	14	14,1		161	115	121
4	26	15	15,1		158	110	121
8	4	15	5,3		126	83	110
8	8	21	7,3		117	77	100
8	16	33	11,3		101	66	81
8	20	39	13,3		94	62	76
8	24	45	15,3		83	54	70
8	26	48	16,3		83	55	68
16	4	41	7,7		115	74	96
16	8	55	9,7		105	68	88
16	16	83	13,7		88	58	74
16	20	97	15,7		81	53	68
16	24	111	17,7	87	80	52	64
16	26	118	18,7	86	78	51	62
24	4	77	7,12		108	71	89
24	8	101	9,12		103	67	86
24	16	149	13,12		87	56	73
24	20	173	15,12		82	54	68
24	24	197	17,12	86	79	52	64
24	26	209	18,12	83	76	50	60
32	4	101	11,15		89	57	73
32	8	131	13,15		84	54	69
32	16	191	17,15	81	75	48	60
32	20	221	19,15	77	71	45	55
32	24	251	21,15		68	43	53
32	26	266	22,15		66	42	44

To achieve the performance documented in this table, it may be necessary to specify a TIMESPEC (timing specification) PERIOD constraint appropriate to meet the documented frequency.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
A_Width	Integer	4 - 32
Coef_Width	Integer	2 - 26
Signed_Input_Data	Boolean	True/False
Signed_Coefficient	Boolean	True/False
Coefficient	Integer	