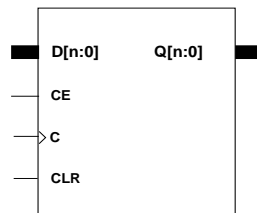




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X8482

## Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan Families
- Data widths from 2 to 32 bits
- Asynchronous clear
- Clock enable
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

## Functional Description

This module performs the function of a N-bit rising-edge sensitive D-type register with optional clock-enable and asynchronous clear. See truth table for details:

C	CE	CLR	Q
X	X	1	0
X	0	0	Q
	1	0	D

## Pinout

Port names for the schematic symbol are shown in Figure 1 and Table 1.

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D[n:0]	Input	DATA INPUT – values on this input are captured by the register when CE is active, CLR is in-active, and a rising edge occurs on C.
CE	Input	CLOCK ENABLE – the value on D is only captured by the register when CE is active and a rising edge occurs on C.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CLR	Input	ASYNCHRONOUS CLEAR – clears the register when asserted. Overrides Clock and Clock Enable. Level sensitive.
Q[n:0]	Output	REGISTERED OUTPUT DATA

## CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name:** Enter a name for the output files generated for this module.
- **Port Width:** Select an input bit width from the pull-down menu. The valid range is 2-32.

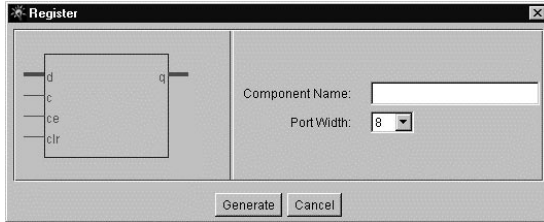


Figure 2: Parameterization Window

## Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

## Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to [coregen@xilinx.com](mailto:coregen@xilinx.com).

Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	1
3	2
4	2
5	3
6	3
7	4
8	4
9	5
10	5
11	6
12	6
13	7
14	7
15	8
16	8
17	9
18	9
19	10
20	10
21	11
22	11
23	12
24	12
25	13
26	13
27	14
28	14
29	15
30	15
31	16
32	16

## Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Port_Width	Integer	2 - 32