Square Root

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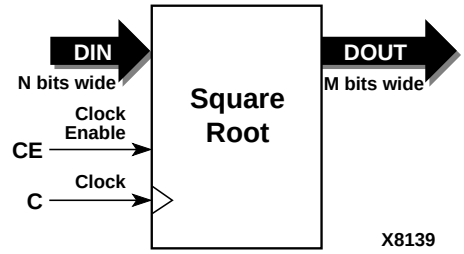

Figure 1: Block Diagram

Features

- Input data widths from 4 to 64 bits
- Pipelined construction for increased throughput
- Performs one square-root function per clock cycle
- Output data widths from 4 to 64 bits
- Clock enable for entire pipeline
- User can determine the accuracy of the result by selecting the desired output width
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The Square Root module derives the square root of the given input value.

The default output bit-width equals one-half the input bit-width. If higher accuracy is desired, choose a higher output width, up to the value of the input width.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

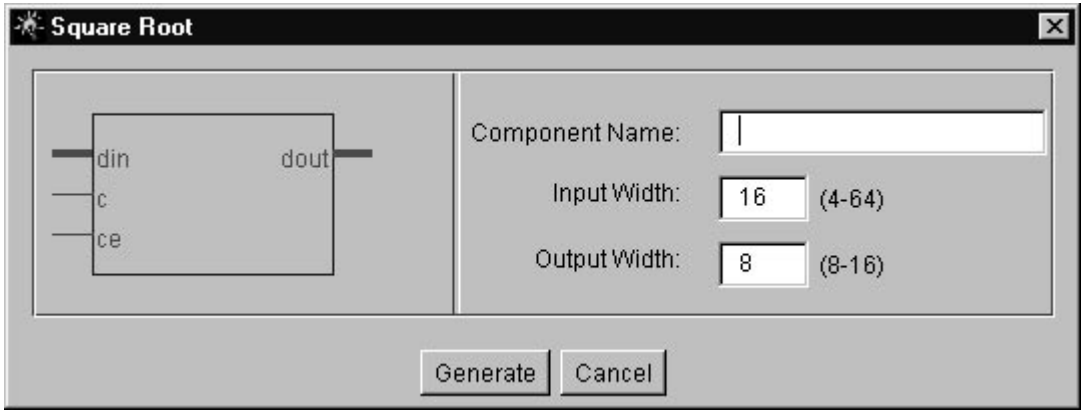

Figure 2: Parameterization Window

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
DIN [n:0]	Input	INPUT DATA
C	Input	CLOCK with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CE	Input	CLOCK ENABLE – active high
DOUT [m:0]	Output	OUTPUT DATA

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 4 to 64.
- **Output Width**: Select an output bit width from the pull-down menu. The valid range varies with the size of input data width.

Latency

The latency equals the output width +1.

Core Resource Utilization

The number of CLBs required depends on the size of the input and output data widths selected in the CORE Generator parameterization window.

If output_width = input_width/2:

$$CLBs = (input\_width/2 + 1)^2$$

If output_width > input_width/2:

$$CLBs = (input\_width/2 + 1)(output\_width + 1) + (output\_width - input\_width/2) * (output\_width - input\_width/2 + 1)/2$$

Table 2 shows the resource utilization for some available bit widths.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com

Table 2: Square Root Characterization Data.

Input Width	Output Width	CLB Count	Area Required for RPM (Rows, Columns)[2]	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan-4 (Advanced)
8	8	58	9,9				
12	12	117	13,13				
16	8	80	9,9		84	56	
16	16	196	17,17				
24	12	168	13,13		80	54	
24	24	414	25,25				
32	16	288	17,17	76	69	46	
32	32	712	33,33				
48	24	624	25,25		60	39	
64	32	1088	33,33		51	34	

Note 1: To achieve the performance documented in this table, it may be necessary to specify a TIMESPEC (timing specification) PERIOD constraint appropriate to meet the documented frequency.

Note 2: The RPM dimensions shown provide guidance for selecting a device with the appropriate CLB array size.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Input_Width	Integer	4 - 64
Output_Width	Integer	4 - 64