Using the Digital Clock Manager (DCM)

Introduction

The Virtex-II DCM provides a complete on-chip and off-chip clock(s) generator, offering a wide range of powerful clock management features:

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock.

- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.

- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

- **EMI Reduction**: The DCM provides the capability to reduce electromagnetic interference (EMI) by broadening the output clock frequency spectrum.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four DCM clock outputs can drive global clock multiplexer buffer inputs simultaneously. All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers. The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM

- LOCKED output pin: asserted High when all enabled DCM circuits have locked.

- STATUS output pins (active High): shown in Table 2-8.

Table 2-8: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The Virtex-II Digital Clock Manager (DCM) offers a fully digital, dedicated on-chip de-skew circuit providing zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. They can be used to implement several circuits that improve and simplify system level design.

Any four outputs of the DCM can be used to drive a global clock network. All DCM outputs can drive general interconnect at the same time; for example, DCM output can be used to generate board-level clocks. The well-buffered global clock distribution network minimizes clock skew caused by loading differences. By monitoring a sample of the output clock (CLK0 or CLK2X), the de-skew circuit compensates for the delay on the routing

network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DCM provides multiple phases of the source clock (CLK0, CLK90, CLK180, and CLK270). The de-skew circuit can also act as a clock doubler, or it can divide the user source clock by up to 16. Figure 2-19 shows all of the inputs and outputs relevant to the DCM de-skew feature.
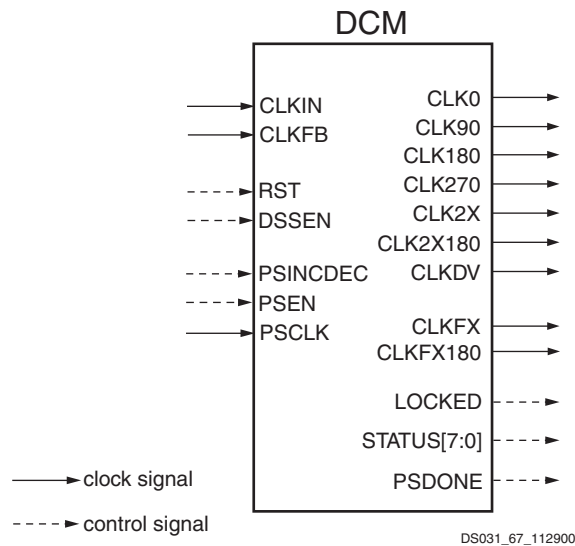

Figure 2-19: **Clock De-Skew Outputs**

Clock multiplication gives a number of design alternatives. For instance, a 100 MHz source clock doubled by the DCM can drive an FPGA design operating at 200 MHz. This technique simplifies board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The de-skew feature can also act as a clock mirror. By driving the CLK0 or CLK2X output off-chip and then back in again, the de-skew feature can be used to de-skew a board-level clock serving multiple devices.

By taking advantage of the de-skew circuit to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Operation

A de-skew circuit in its simplest form consists of variable delay line and control logic. The delay line produces a delayed version of the input clock CLKIN. The clock distribution network routes the clock to all internal registers and to the clock feedback CLKFB pin. The control logic must sample the input clock as well as the feedback clock in order to adjust the delay line.

For optimum performance, the Virtex-II DCM uses a discrete digital delay line, which is a series of buffer elements each with an intrinsic delay of less than DCM_TAP (see AC characteristics in the *Virtex-II Data Sheet).*

A de-skew circuit works by inserting delay between the input clock and the feedback clock until the two rising edges align, putting the two clocks 360 degrees out of phase, which means they are in phase. When the edges from the input clock line up with the edges from the feedback clock, the DCM achieves "lock." The two clocks have no discernible difference. Thus, the DCM output clock compensates for the delay in the clock distribution network, effectively removing the delay between the source clock and its loads.

Input Clock Requirements

The output clock signal of a DCM, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. A DCM cannot improve the input jitter. The DCM input clock requirements are specified in the *Virtex-II Data Sheet*.

Once locked, the DCM can tolerate input clock period variations of up to the value specified by CLKIN_PER_DRIFT_DLL_HF (at high frequencies) or CLKIN_PER_DRIFT_DLL_LF (at low frequencies). Larger frequency changes can cause the DCM to lose lock, which is indicated by the LOCKED output going low. The user must then reset the DCM. The cycle-to-cycle input jitter must be kept to less than CLKIN_PER_JITT_DLL_LF in the low frequencies and CLKIN_PER_JITT_DLL_HF for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the DCM. Failure to reset the DCM produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the de-skew circuit. The clock should be stopped no more than 100 ms to minimize the effect of device cooling, which would change the tap delays. The clock should be stopped during a Low phase, and when restored, must generate a full High half-period. During this time, LOCKED stays High and remains High when the clock is restored. So a High on LOCKED does not necessarily mean that a valid clock is available.

When the clock is stopped, one to four more clocks are still generated as the delay line is flushed. When the clock is restarted, the output clocks are not generated for one to four clocks as the delay line is filled. The most common case is two or three clocks. In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates to the output one to four clocks after the original shift, with no disruption to the DCM control.

The clock input of the DCM can be driven either by an IBUFG, an IBUF, or a BUFGMUX. An LVDS clock can also be used as input.

Output Clocks

Some restrictions apply regarding the connectivity of the output pins. The DCM clock outputs can drive an OBUF, a global clock buffer BUFGMUX, or they can route directly to destination clock pins. The DCM clock outputs can drive BUFGMUXs that are on the same edge of the device (top or bottom).

Do not use the DCM output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DCM output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Characteristics of the De-Skew Circuit

- Can eliminate clock distribution delay by effectively adding one clock period delay. Clocks are de-skewed to within CLKOUT_PHASE specified in the data sheet.
- Adapts to a wide range of frequencies. However, once locked to a frequency, cannot tolerate large variations of the input frequency.
- Does not eliminate jitter. The de-skew circuit output jitter is the sum of input jitter and some jitter value that the de-skew circuit might add.
- Requires a continuously running input clock.
- Can be used to eliminate on-chip as well as off-chip clock delay.
- Has no restrictions on the delay in the feedback clock path.
- The completion of configuration can be delayed until after DCM locks to guarantee the system clock is established prior to initiating the device.
- De-skew circuit is part of the DCM, which also includes phase adjustment, frequency synthesis, and spread spectrum techniques that are described in this document.

Port Signals

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the de-skew circuit operates) to the DCM. The CLKIN frequency must fall in the ranges specified in the Virtex-II *Data Sheet*. The clock input signal can be provided by one of the following:

IBUF — Input buffer

IBUFG — Global clock input buffer on the same edge of the device (top or bottom)

BUFGMUX — Internal global clock buffer

Feedback Clock Input — CLKFB

A reference or feedback signal is required to provide the delay-compensated output. Connect only the CLK0 or CLK2X DCM outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DCM. The feedback clock input signal can be driven by an internal global clock buffer (BUFGMUX), one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom), or IBUF (the input buffer.)

If an IBUFG sources the CLKFB pin, the following special rules apply:

1. An external input port must source the signal that drives the IBUFG input pin.

2. That signal must directly drive only OBUFs and nothing else.

Reset Input — RST

When the reset pin activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DCM delay taps reset to zero, glitches can occur on the DCM clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DCM output clocks no longer de-skew with respect to one another. For these reasons, use the reset pin only when reconfiguring the device or changing the input frequency. The reset input signal is asynchronous and should be held HIGH for 2 ns. It takes approximately 120 ns for the DCM to achieve lock after a reset for the slowest frequency range. The DCM locks faster at higher frequencies.

2x Clock Output — CLK2X

The CLK2X output provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the DCM has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DCM to lock on the correct edge with respect to source clock. This output is not available in the high frequency mode.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin has a 50/50 duty cycle but only for integer values of the division factor N.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. In the low frequency mode, the DCM provides three phase-shifted versions of the CLK0 signal (CLK90, CLK180, and CLK270) while in the high frequency mode only the 180 phase-shifted version is provided. All four (including CLK0) of the phase shifted outputs can be used simultaneously in the low frequency mode. The

relationship between phase shift and the corresponding period shift appears in Table 2-9. The timing diagrams in Figure 2-20 illustrate the DLL clock output characteristics.

Table 2-9:   **Relationship of Phase-Shifted Output Clock to Period Shift**

Phase (degrees)	% Period Shift
0	0%
90	25%
180	50%
270	75%

By default, the DCM provides a 50/50 duty cycle correction on all 1x clock outputs. The DUTY_CYCLE_CORRECTION attribute (TRUE by default), controls this feature. In order to deactivate the DCM duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DCM symbol. With duty cycle correction deactivated, the output clock has the same duty cycle as the source clock.

The DCM clock outputs can drive an OBUF, a BUFGMUX, or they can route directly to destination clock pins.

2

x132_07_092599
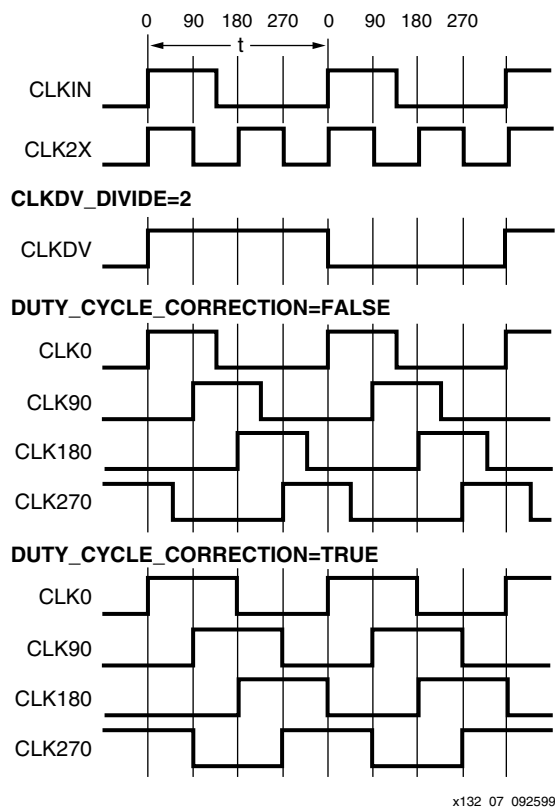
Figure 2-20:   **DLL Output Characteristics**

Locked Output — LOCKED

In order to achieve lock, the DCM may need to sample several thousand clock cycles. After the DCM achieves lock, the LOCKED signal activates. The DCM timing parameter section of the data sheet provides estimates for locking times.

To guarantee that the system clock is established prior to the device "waking up," the DCM can delay the completion of the device configuration process until after the DCM locks. The STARTUP_WAIT attribute activates this feature.

Until the LOCKED signal activates, the DCM output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular, the CLK2X output appears as a 1x clock with a 25/75 duty cycle.

Status - STATUS

The STATUS output is 8-bit output, of which the STATUS[1] reveals the loss of the input clock, CLKIN to the DCM.

Attributes

The following attributes provide access to some of the Virtex-II series de-skew features, (for example, clock division and duty cycle correction).

Frequency Mode

The de-skew feature of the DCM is achieved with a delay-locked loop (DLL). This attribute specifies either the high or low frequency mode of the DLL. The default is the low frequency mode. In the high frequency mode, the only outputs available from the DLL are the CLK0, CLK180, CLKDV, and LOCKED. The frequency ranges for both the frequency modes are specified in the data sheet. In order to set the DLL to the high frequency mode, attach the DLL_FREQUENCY_MODE=HIGH attribute in the source code or schematic.

Feedback Input

This attribute specifies the feedback input to the DCM (CLK0, or CLK2x). CLK0 is the default feedback. When both the CLK0 and the CLK2x outputs are used internally or externally to the device, the feedback input can be either the CLK0 or CLK2x. In order to set the feedback to CLK2X, attach the CLOCK_FEEDBACK=2X attribute in the source code or schematic.

Duty Cycle Correction

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty cycle corrected default such that they exhibit a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION attribute (by default TRUE) controls this feature.

In order to deactivate the DCM duty cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE attribute in the source code or schematic. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

Clock Divide

The CLKDV_DIVIDE attribute specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this attribute are 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, or 16; the default value is 2.

Startup Delay

This attribute, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DCM locks before going to High. For details, refer to Chapter 3: Configuration.
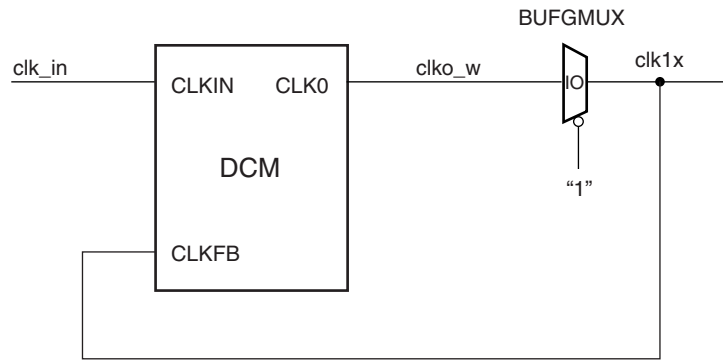
Legacy Support

The Virtex/Virtex-E library primitives/sub modules are supported in Virtex-II for legacy purposes. The following are supported primitives/submodules:

- CLKDLL
- CLKDLLE
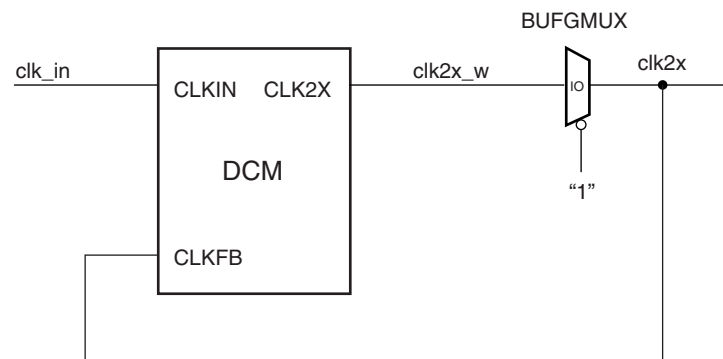- CLKDLLHF
- BUFGDLL

Library Primitive

Only a single library primitive is available for the DLL, a part of the DCM. It is labeled the 'DCM' primitive.
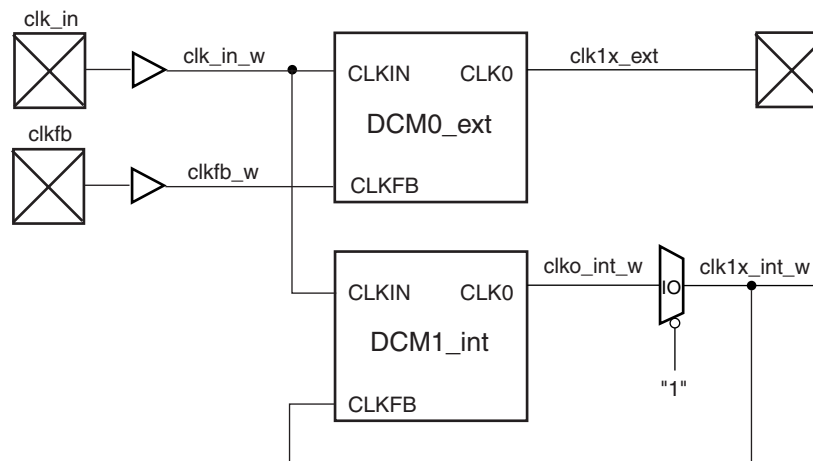
Submodules

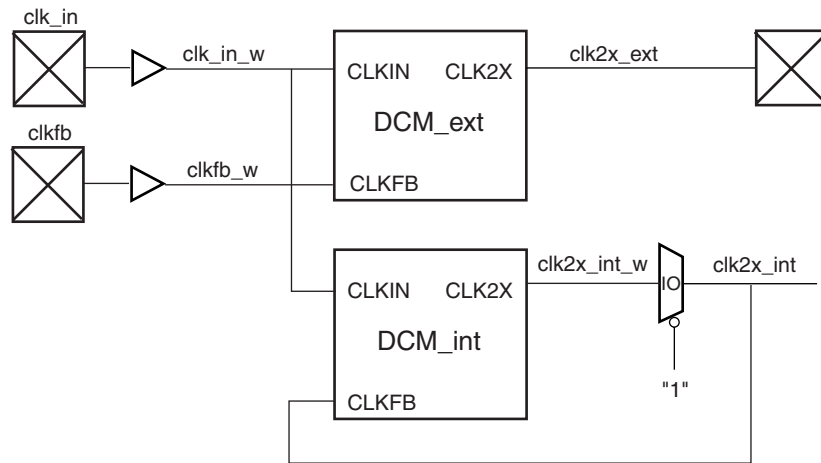UG002_C2_061_112800

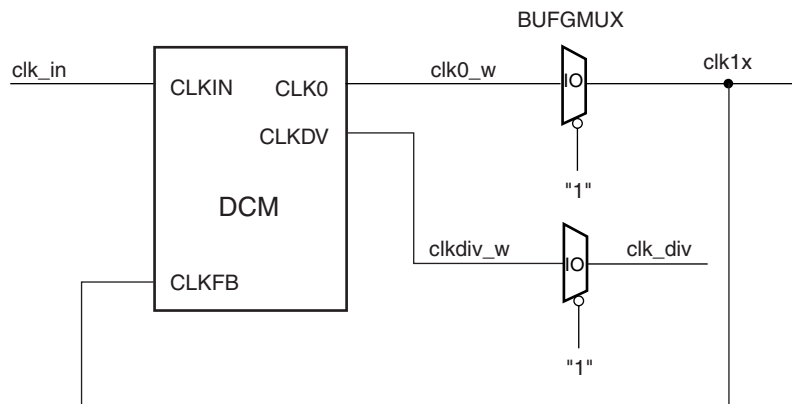*Figure 2-21:* **BUFG_CLK0_SUBM**

UG002_C2_062_112800

Figure 2-22: **BUFG_CLK2X_SUBM**

UG002_C2_063_110700

Figure 2-23: **BUFG_CLK0_FB_SUBM**

UG002_C2_064_112800

Figure 2-24: **BUFG_CLK2X_FB_SUBM**

UG002_C2_065_110700

Figure 2-25: **BUFG_CLKDV_SUBM**

Frequency Synthesizer

The Virtex-II FPGA offers a fully digital, dedicated on-chip digital Frequency Synthesizer circuit as part of each Digital Clock Manager (DCM). The output, of the DFS can be any function of the input clock frequency described by M/D. M, the numerator is the multiplication factor and D, the denominator is the division factor.

The two counter-phase frequency synthesized outputs can drive global clock routing networks within the device. The well-buffered global clock distribution network minimizes clock skew due to differences in distance or loading. See Figure 2-25.

Operation

The DCM clock output CLKFX is any M/D product of the clock input to the DCM. M and D values can each range from 1 to 4096. However, note that the frequency synthesizer has an input frequency range and an output frequency ranges specified in the data sheet. The frequency synthesizer output is not phase aligned to the clock output, CLK0, unless a feedback is provided to the CLKFB input of the DCM.
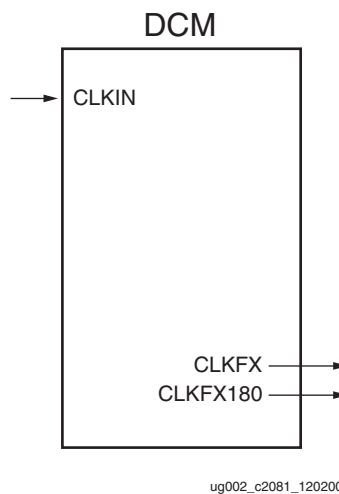
DCM

CLKIN

CLKFX
CLKFX180

ug002_c2081_120200

Figure 2-26:   **Frequency Synthesized Outputs**

The internal operation of the frequency synthesizer is complex and beyond the scope of this document. The frequency synthesizer multiplies the incoming frequencies by the pre-calculated quotient M/D and generates the correct output frequencies as long as it is within the range specified in the data sheet.

Consider, input frequency = 50 MHz, e. g., M = 333, D = 100 (note that M and D values have no common factors and hence cannot be reduced). The output frequency is correctly 166.50 MHz, although 333 x 50 MHz = 1.665 GHz and 50 MHz/100 = 500 kHz are both far outside the range of the frequency output.

Frequency Synthesizer Characteristics

- The frequency synthesizer provides an output frequency equal to the input frequency multiplied by M and divided by D.

- The outputs CLKFX and CLKFX180 always have a 50/50 duty-cycle.

- Phase-alignment with CLK0 is an option.

- Smaller M and D values achieve faster lock times. The user should divide M and D by the largest common factor.

Port Signals

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock to the DCM. The CLKIN frequency must fall in the ranges specified in the *Virtex-II Data Sheet*. The clock input signal can be provided by one of the following:

- IBUF   — Input buffer

- IBUFG — Global clock input buffer

- BUFGMUX — Internal global clock buffer

Reset Input — RST

When the reset pin activates, the LOCKED signal deactivates within four source clock cycles. The M and D values at configuration are maintained after the reset. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. For this reason, activate the reset pin only when reconfiguring the device or changing the input frequency. The reset input signal is asynchronous and should be held High for 2 ns.

Frequency Synthesized Clock Output - CLKFX

The CLKFX output provides a frequency-synthesized clock (M/D * CLKIN) with a 50/50 duty cycle. For the CLKFX output to be phase-aligned to the CLKIN, the clock feedback (CLK0) has to be provided at the CLKFB input of the DCM. With M and D adjusted such that they have no common factor, the alignment can only occur every D input clock cycle.

Frequency Synthesized Clock Output 180º Phase Shifted - CLKFX180

The CLKFX180 output is a 180º phase shifted version of the CLKFX clock output, also with a 50/50 duty cycle.

Locked Output — LOCKED

The LOCKED signal is activated after the DCM has achieved the values set by the user parameters. To guarantee that the system clock is established prior to the device "waking up," the DCM can delay the completion of the device configuration process until after the DCM locks. The STARTUP_WAIT attribute activates this feature. Until the LOCKED signal activates, the DCM output clocks are not valid and can exhibit glitches, spikes, or other spurious signals.

Status - STATUS

The STATUS output is an 8-bit output, of which the STATUS[1] indicates the loss of the input clock, CLKIN to the DCM, only when CLKFB is connected.

Attributes

The following attributes provide access to some of the Virtex-II series frequency synthesis features, (for example, clock multiplication, clock division).

Frequency Mode for Frequency Synthesis

This attribute specifies either the high or low frequency mode of the frequency synthesizer. The default is the low frequency mode. The frequency ranges for both the frequency modes are specified in the data sheet.

To set the frequency synthesizer to the high frequency mode, attach the DFS_FREQUENCY_MODE=HIGH attribute in the source code or schematic.

Multiply/Divide Attribute

The M and D values can be set using the CLKFX_MULTIPLY and the CLKFX_DIVIDE attributes. The default settings are M = 4 and D = 1.

Startup Delay

The STARTUP_WAIT attribute can be configured TRUE or FALSE (the default value). When TRUE, the device configuration DONE signal waits in the Low state until the DCM locks before going to High. For details, refer to Chapter 3: Configuration.
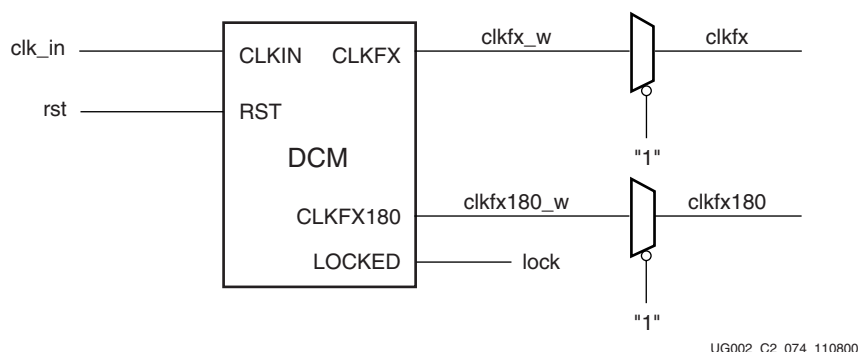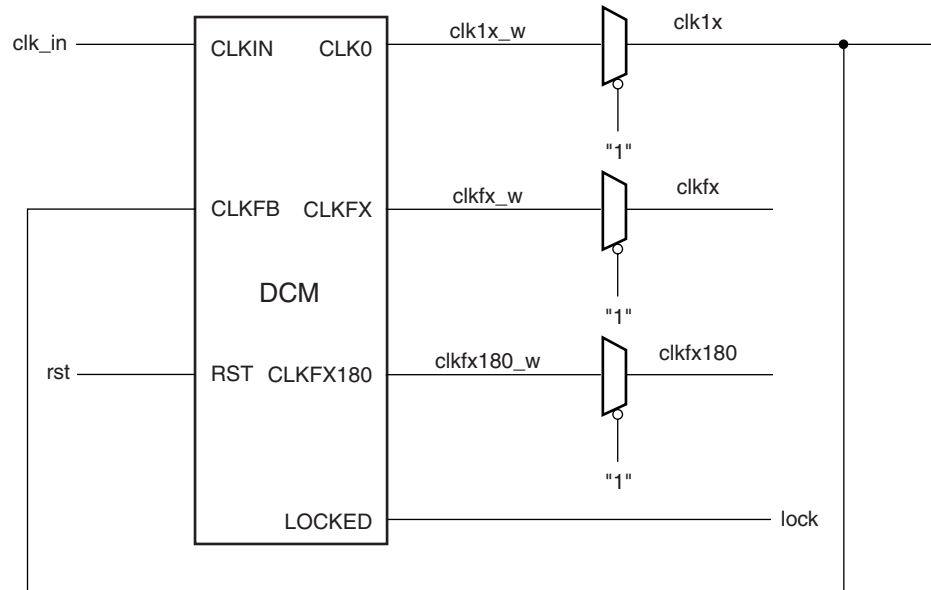
Submodules

UG002_C2_074_110800

Figure 2-27: **BUFG_DFS_SUBM**

UG002_C2_075_110800

Figure 2-28: **BUFG_DFS_FB_SUBM**

Phase Shifter

The Virtex-II FPGA offers a digital dedicated on-chip digital phase shifter circuit that is part of the Digital Clock Manager (DCM). A phase shifted output with a resolution of DCM_TAP or $1/256^{th}$ of the input clock period can be created. The phase shift can be fixed (established by configuration) or dynamic. The phase shifter settings affect all of the outputs of the DCM. See Figure 2-29.

Operation

Figure 2-30 shows a block diagram of the DCM and all of the outputs affected by the phase shifter circuitry. The phase shifter settings affect the frequency synthesizer outputs only if a clock feedback is provided to the CLKFB input of the DCM.
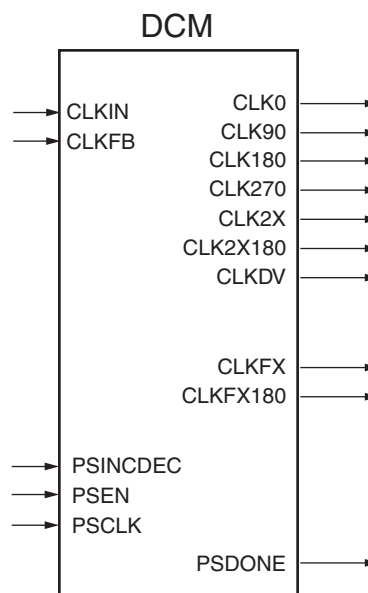
ug002_c2_082_120200

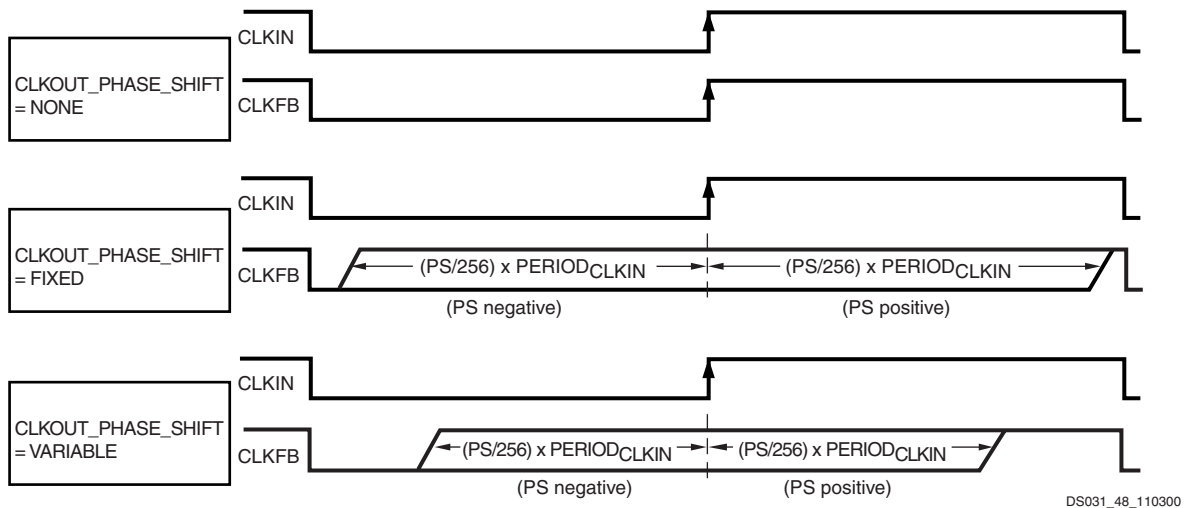*Figure 2-29:* **Phase Shift Outputs**

Figure 2-30: **Phase Shift Effects**

The phase shifter provides fine phase adjustment for the outputs of the DCM. The phase shifter operates in two modes: fixed mode and variable mode. In fixed mode, the phase shift between the clock input to the DCM and the DCM clock output is set by the phase shift configuration attribute. In fixed mode, the variation in the phase can cover a range from -255/256 to +255/256 of the clock period (FINE_SHIFT_RANGE). In variable mode, the phase shift between the clock input to the DCM and the DCM clock output set at configuration is used as the starting point, and the phase value can be changed during operation using the PSEN, PSINCDEC, and the PSCLK signals. In variable mode, the variation in the phase can be up to FINE_SHIFT_RANGE divided by 2, from -255/256 to +255/256 of the clock period.

The equation for the phase shift is as follows:

$$\text{CLKIN\_CLKFB\_skew} = (\text{Phase Shift}/256) \times \text{PERIOD}_{\text{CLKIN}}$$

In the variable mode, the phase factor can be changed by activating PSEN for one period of PSCLK. Increments or decrements to the phase factor can be made by setting the PSINCDEC pin to a High or Low, respectively. When the de-skew circuit has completed an increment or decrement operation, the signal PSDONE goes high for a single PSCLK cycle. This indicates to the user that the next change may be made.

The user interface and the physical implementation are different. The user interface describes the phase shift as a fraction of the clock period (N/256). The physical implementation adds the appropriate number of buffer stages (each DCM_TAP) to the clock delay. The DCM_TAP granularity limits the phase resolution at clock frequencies > 100 MHz. The available number of buffer stages limits the ability to achieve a granularity (1/256 x clock period) less than DCM_TAP.

Phase Shifter Characteristics

- Offers fine phase adjustment with a resolution of ±1/256 of the clock period (or ± DCM_TAP, whichever is greater) by configuration and also dynamically under user control.

- The phase shifter settings affect all DCM outputs.

- The phase shifter settings affect the frequency synthesized output, but only if clock feedback is provided.

- The frequency specification is a same as that of the DCM.

- V_{CC} and temperature do not affect the phase shift provided by the phase shift feature.

Port Signals

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock to the DCM. The CLKIN frequency must fall in the ranges specified in the data sheet. The clock input signal can be provided by one of the following:

IBUF — Input buffer

IBUFG — Global clock input buffer

BUFGMUX — Internal global clock buffer

Feedback Clock Input — CLKFB

The DCM requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DCM outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DCM. The feedback clock input signal can be driven by an internal global clock buffer (BUFGMUX), one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom), or IBUF (the input buffer.)

If an IBUFG sources the CLKFB pin, the following special rules apply:

1.   An external input port must source the signal that drives the IBUFG input pin.

2.   That signal must directly drive only OBUFs and nothing else.

Phase Shift Clock - PSCLK

The PSCLK input can be sourced by the CLKIN signal to the DCM, or it can be a lower or higher frequency signal provided from any clock source (external or internal). The frequency range of PSCLK is defined by PSCLK_FREQ_LF/HF (see the *Virtex-II Data Sheet*). This input has to be tied to ground when the CLK_OUT_PHASE_SHIFT attribute is set to NONE or FIXED.

Phase Shift Increment/Decrement - PSINCDEC

The PSINCDEC signal is synchronous to PSCLK and is used to increment or decrement the phase shift factor. In order to increment or decrement the phase shift by 1/256 of clock period, the PSINCDEC signal must be set to a logic High or Low, respectively. This input has to be tied to ground when the CLK_OUT_PHASE_SHIFT attribute is set to NONE or FIXED.

Phase Shift Enable - PSEN

The PSEN signal is synchronous to the PSCLK and is used in conjunction with the PSINCDEC signal. The phase shift factor is incremented when the PSINCDEC signal is a High or decremented when the PSINCDEC signal is a Low, only during the PSCLK period when PSEN is High. This input has to be tied to ground when the CLK_OUT_PHASE_SHIFT attribute is set to NONE or FIXED.

Reset Input — RST

When the reset pin activates, the LOCKED signal deactivates within four source clock cycles. After reset, the phase shift value set to its value at configuration in both the fixed and variable modes. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. For this reason, activate the reset pin only when reconfiguring the device or changing the input frequency. The reset input signal is asynchronous and should be held High for 2 ns.

Locked Output — LOCKED

The LOCKED signal activates after the DCM has achieved lock. To guarantee that the system clock is established prior to the device "waking up," the DCM can delay the completion of the device configuration process until after the DCM locks. The STARTUP_WAIT attribute activates this feature. Until the LOCKED signal activates, the DCM output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. For details, refer to Chapter 3: Configuration.

Phase Shift DONE - PSDONE

The PSDONE signal is synchronous to PSCLK and indicates that the requested phase shift was completed. This signal also indicates to the user that the next change to the phase shift numerator can be made. This output signal is not used if the phase shift feature is not being used or the phase shifter is in FIXED mode.

Status - STATUS

The STATUS output is an 8-bit output, of which the STATUS[0] indicates the overflow of the phase shift numerator, and indicates that the absolute delay range of the phase shift delay line is exceeded.

Attributes

The following attributes provide access to the fine phase adjustment feature of the Virtex-II series phase shifter.

Clock Out Phase Shift

The CLK_OUT_PHASE_SHIFT attribute controls the use of the PHASE_SHIFT value. It can be set to NONE, FIXED, or VARIABLE. By default, this attribute is set to NONE indicating that the phase shifter is not being used. The PHASE_SHIFT value has no effect on the DCM outputs when this attribute is set to NONE. If the CLOCK_OUT_PHASE_SHIFT attribute is set to FIXED or NONE, then the PSEN, PSINCDEC, and the PSCLK inputs have to be tied to ground. The effects of the CLK_OUT_PHASE_SHIFT attribute are shown in Figure 2-30.

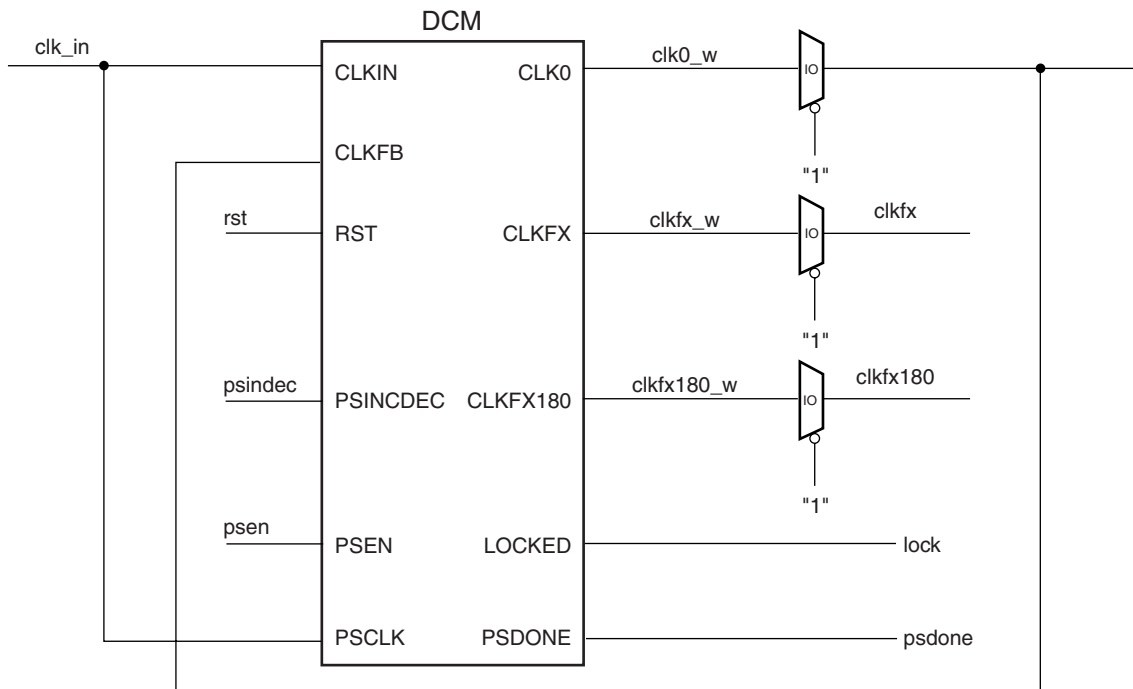### PHASE_SHIFT

This attribute allows the phase shift numerator to be set to any value from -255 to 255.

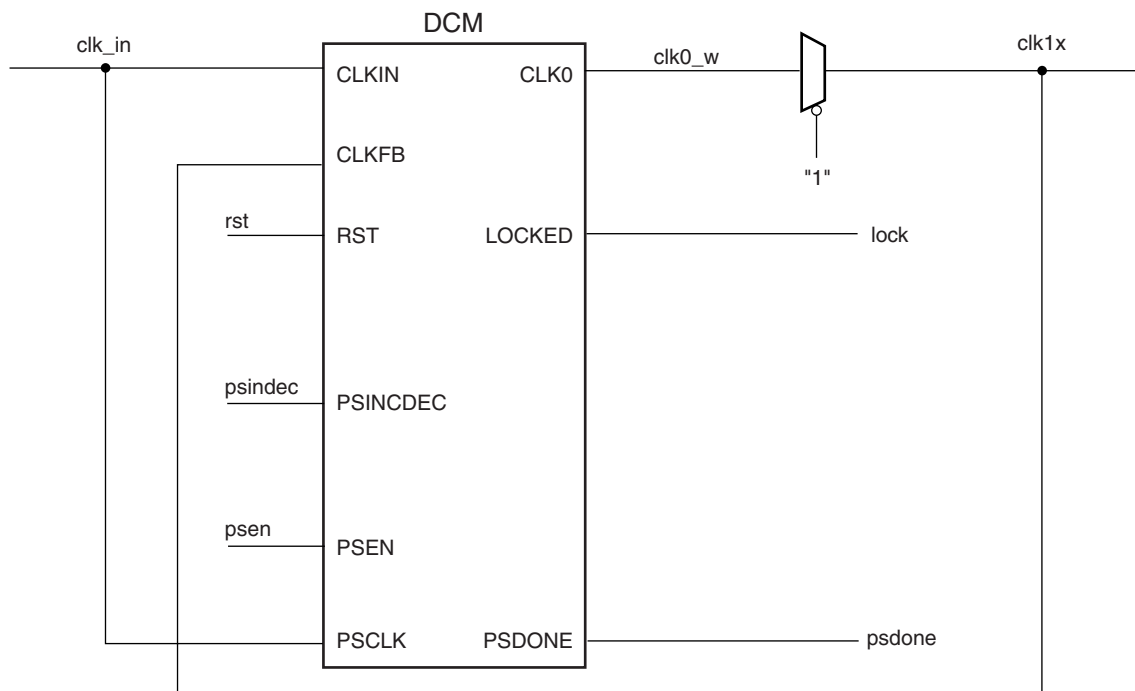### Maximum Period of Phase Shift Clock - PSCLK_FREQ_LF/HF

This parameter defines the maximum clock period for the phase shift clock.

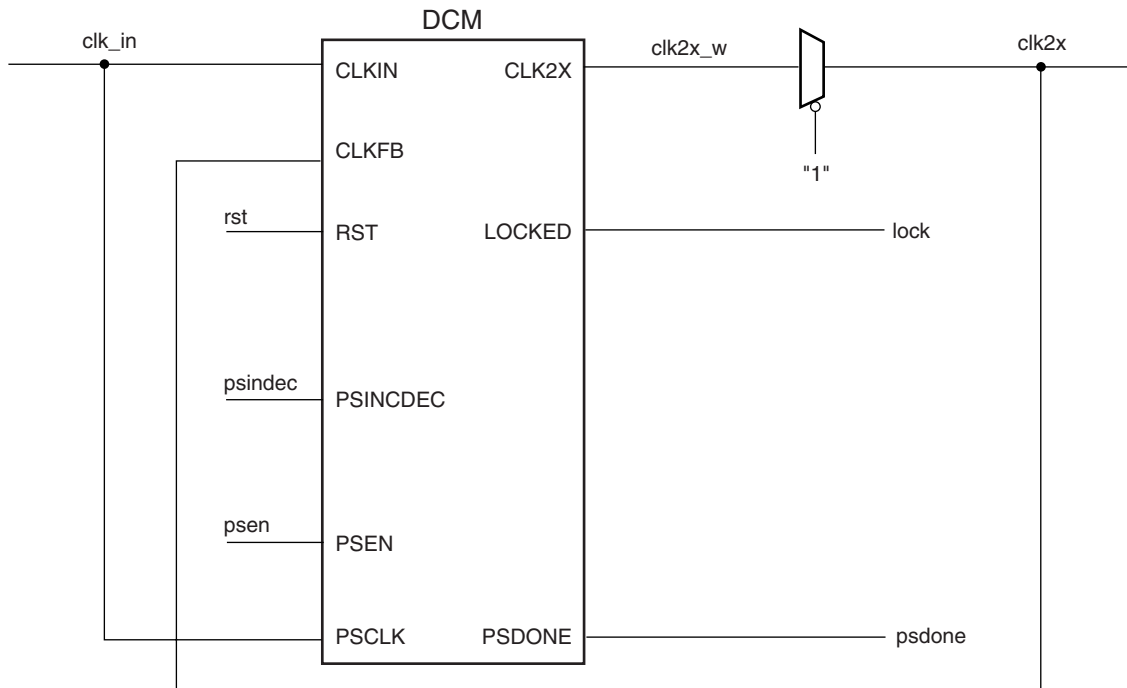Submodules

ioUG002_C2_076_112900

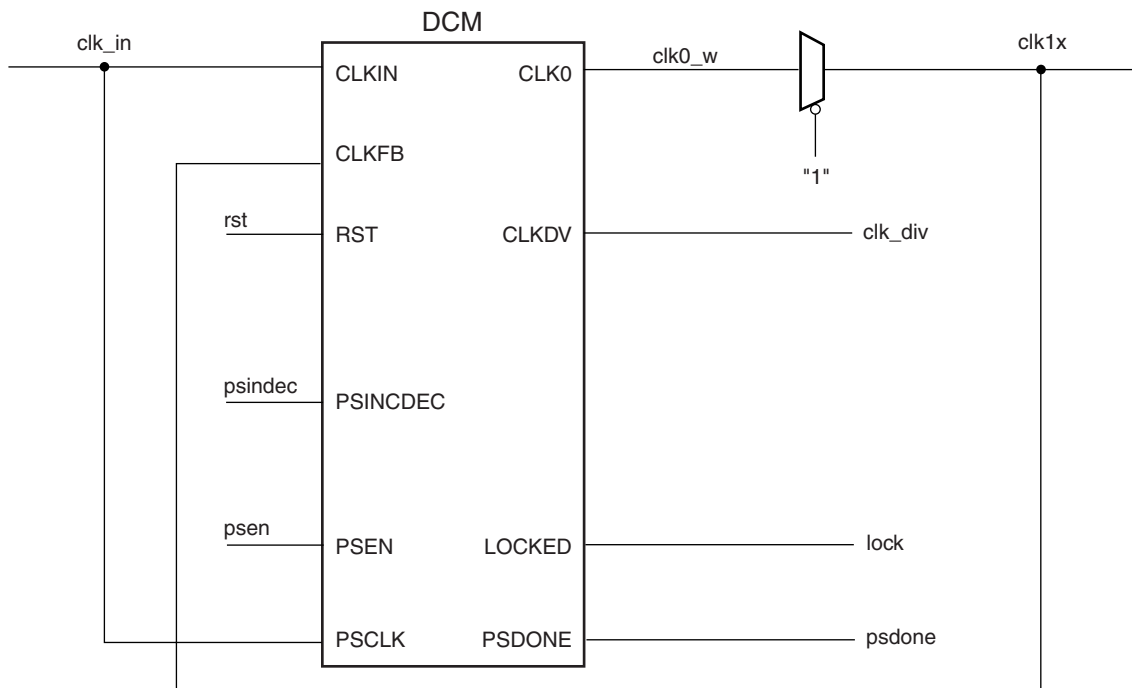*Figure 2-31:* **BUFG_PHASE_CLKFX_FB_SUBM**

UG002_C2_071_110800

Figure 2-32: **BUFG_PHASE_CLK0_SUBM**

UG002_C2_072_120200

Figure 2-33: **BUFG_PHASE_CLK2X_SUBM**

UG002_C2_073_110800

Figure 2-34: **BUFG_PHASE_CLKDV_SUBM**

Digital Spread Spectrum (DSS)

The Virtex-II FPGA offers up to 12 fully digital dedicated on-chip DCMs that are capable of broadening the frequency spectrum of output clocks through the Digital Spread Spectrum (DSS) circuitry.

Operation

The DSS spreads the frequency spectrum of DCM clock outputs. If the DSS circuitry is enabled, the user can set a spread value to any one of four values (2,4,6, or 8) using the DSS_MODE attribute. A spread value of 2 provides new clock periods at ± DCM_TAP of the original clock period; a spread value of 4 corresponds to cumulative new clock periods at ± DCM_TAP and ±2 x DCM_TAP; a spread value of 6 corresponds to cumulative new clock periods at ±DCM_TAP, ±2 x DCM_TAP, and ±3 x DCM_TAP; and a spread value of 8 corresponds to cumulative new clock periods at ±DCM_TAP, ±2 x DCM_TAP, ±3 x DCM_TAP, and ±4 x DCM_TAP.

Characteristics

- The DSS is useful in spreading the frequency spectrum of output clocks.

- The DSS can provide cumulative new clock periods at ±DCM_TAP, ±2 x DCM_TAP, ±3 x DCM_TAP, and ±4 x DCM_TAP.

- The DSS settings affect the 1x clock outputs fully. The effects on the other outputs are minimal.

Port Signals

DSS Enable (DSSEN)

The DSSEN input signal to the DCM indicates whether the DSS circuitry is enabled. When the DSS_MODE attribute is set to NONE, the DSSEN input has no effect. When the DSS_MODE is set to a value other than NONE and DSSEN is HIGH, the output clock frequency is modulated by the amount of spread specified by the DSS_MODE value.

Attributes

The following attribute provides access to the digital spread spectrum feature of the Virtex-II series DCM.

DSS_MODE

The DSS_MODE attribute takes a value of NONE, 2, 4, 6, or 8. NONE indicates that the DSS circuitry is disabled. A DSS_MODE value of 2 corresponds to new clock periods at ± DCM_TAP of the original clock period. A DSS_MODE value of 4 corresponds to cumulative new clock periods at ± DCM_TAP, and ±2 x DCM_TAP; a DSS_MODE value of 6 corresponds to cumulative new clock periods at ± DCM_TAP, ±2 x DCM_TAP, ±3 x DCM_TAP; and a DSS_MODE value of 8 corresponds to cumulative new clock periods at ± DCM_TAP, ±2 x DCM_TAP, ±3 x DCM_TAP, and ±4 x DCM_TAP.

VHDL and Verilog Instantiation

VHDL and Verilog instantiation templates are available as examples (see "VHDL and Verilog Templates" on page 178) for all submodules.

In VHDL, each template has a component declaration section and an architecture section. Each part of the template should be inserted within the VHDL design file. The port map of the architecture section should include the design signal names.

VHDL and Verilog Templates

The following submodules described in this section are available:

- BUFG_CLK0_SUBM
- BUFG_CLK2X_SUBM
- BUFG_CLK0_FB_SUBM
- BUFG_CLK2X_FB_SUBM
- BUFG_CLKDV_SUBM
- BUFG_DFS_SUBM
- BUFG_DFS_FB_SUBM
- BUFG_PHASE_CLKFX_FB_SUBM
- BUFG_PHASE_CLK0_SUBM
- BUFG_PHASE_CLK2X_SUBM
- BUFG_PHASE_CLKDV_SUBM

The corresponding submodules must be synthesized with the design. The BUFG_CLK0_SUBM submodule is provided in VHDL and Verilog as an example.

VHDL Template

```
-- Module: BUFG_CLK0_SUBM
-- Description: VHDL submodule
--  DCM with CLK0 deskew
--
-- Device: Virtex-II Family
----------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
--
-- pragma translate_off
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;
-- pragma translate_on
--
entity BUFG_CLK0_SUBM is
  port (
        CLK_IN : in std_logic;
        RST    : in std_logic;
        CLK1X  : out std_logic;
        LOCK   : out std_logic
       );
end BUFG_CLK0_SUBM;
--
architecture BUFG_CLK0_SUBM_arch of BUFG_CLK0_SUBM is
--
-- Components Declarations:
component BUFG
  port (
  I   : in std_logic;
        O     : out std_logic
  );
end component;
--
component DCM
-- pragma translate_off
    generic (
              DLL_FREQUENCY_MODE : string := "LOW";
              DUTY_CYCLE_CORRECTION : boolean := TRUE;
              STARTUP_WAIT : string : boolean := FALSE
            );
```

```vhdl
-- pragma translate_on
    port ( CLKIN     : in  std_logic;
           CLKFB     : in  std_logic;
           DSSEN     : in  std_logic;
           PSINCDEC  : in  std_logic;
           PSEN      : in  std_logic;
           PSCLK     : in  std_logic;
           RST       : in  std_logic;
           CLK0      : out std_logic;
           CLK90     : out std_logic;
           CLK180    : out std_logic;
           CLK270    : out std_logic;
           CLK2X     : out std_logic;
           CLK2X180  : out std_logic;
           CLKDV     : out std_logic;
           CLKFX     : out std_logic;
           CLKFX180  : out std_logic;
           LOCKED    : out std_logic;
           PSDONE    : out std_logic;
           STATUS    : out std_logic_vector(7 downto 0)
          );
end component;
--
-- Attributes
attribute DLL_FREQUENCY_MODE : string;
attribute DUTY_CYCLE_CORRECTION : string;
attribute STARTUP_WAIT : string;

attribute DLL_FREQUENCY_MODE of U_DCM: label is "LOW";
attribute DUTY_CYCLE_CORRECTION of U_DCM: label is "TRUE";
attribute STARTUP_WAIT of U_DCM: label is "FALSE";

-- Signal Declarations:
signal GND : std_logic;
signal CLK0_W: std_logic;
signal CLK1X_W: std_logic;

begin
GND <= '0';
--
CLK1X <= CLK1X_W;
--
-- DCM Instantiation
U_DCM: DCM
  port map (
           CLKIN =>    CLK_IN,
           CLKFB =>    CLK1X_W,
           DSSEN =>    GND,
           PSINCDEC => GND,
           PSEN =>     GND,
           PSCLK =>    GND,
           RST =>      RST,
           CLK0 =>     CLK0_W,
           LOCKED =>   LOCK
      );
-- BUFG Instantiation
U_BUFG: BUFG
  port map (
      I => CLK0_W,
           O => CLK1X_W
      );
end BUFG_CLK0_SUBM_arch;
```

Verilog Template

```
// Module:        BUFG_CLK0_SUBM
// Description: Verilog Submodule
//  DCM with CLK0 deskew
//
// Device: Virtex-II Family
//----------------------------------------------------------------------

module BUFG_CKL0_SUBM (
                        CLK_IN,
                        RST,
                        CLK1X,
                        LOCK
                      );

    input CLK_IN;
    input RST;

    output CLK1X;
    output LOCK;

    wire CLK0_W;
    wire GND;

    assign GND = 1'b0;

//BUFG Instantiation
//
BUFG  U_BUFG
            (.I(CLK0_W),
             .O(CLK1X)
            );

// Attributes for functional simulation//
// synopsys translate_off
      defparam U_DCM.DLL_FREQUENCY_MODE = "LOW";
      defparam U_DCM.DUTY_CYCLE_CORRECTION = "TRUE";
      defparam U_DCM.STARTUP_WAIT = "FALSE";
// synopsys translate_on

// Instantiate the DCM primitive//
  DCM U_DCM (
                    .CLKFB(CLK1X),
                    .CLKIN(CLK_IN),
                    .DSSEN(GND),
                    .PSCLK(GND),
       .PSEN(GND),
                    .PSINCDEC(GND),
                    .RST(RST),
                    .CLK0(CLK0_W),
       .LOCKED(LOCK)
                  );

// synthesis attribute declarations
  /* synopsys attribute

  DLL_FREQUENCY_MODE "LOW"
  DUTY_CYCLE_CORRECTION "TRUE"
  STARTUP_WAIT "FALSE"
  */
endmodule
```
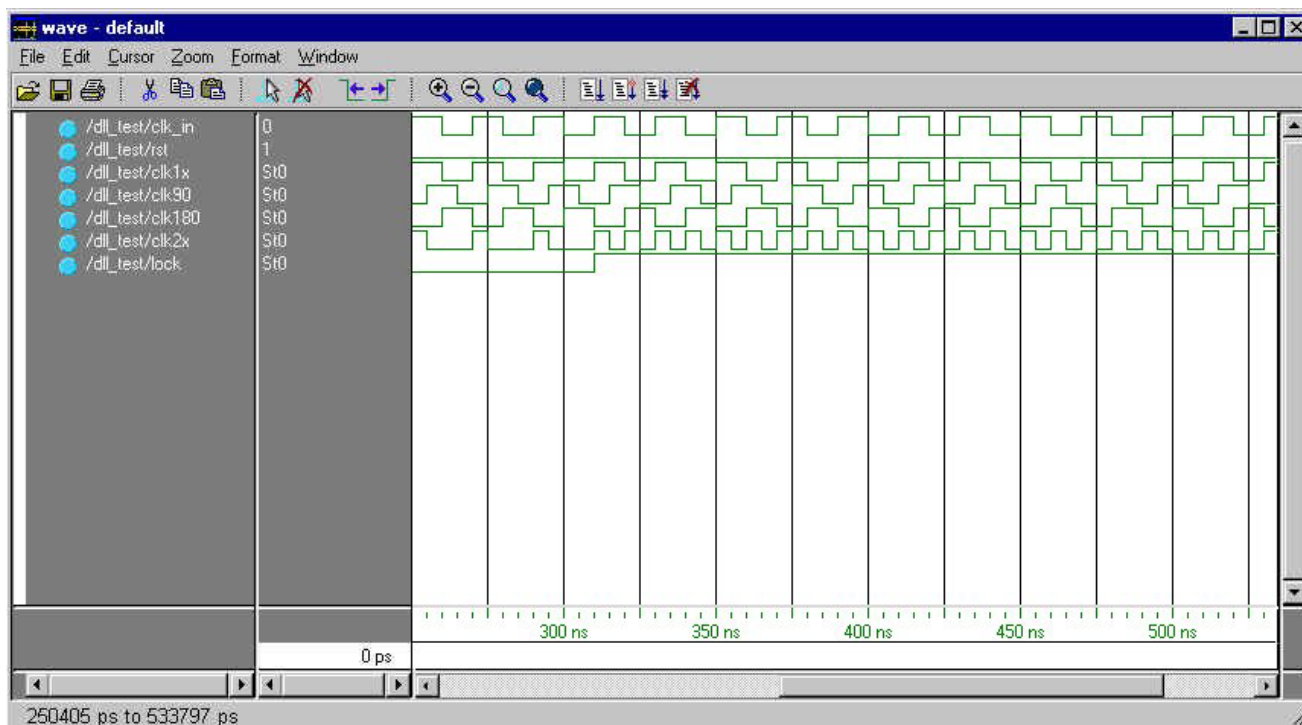
DCM Waveforms

The DCM waveforms shown below are the results of functional simulation using Model Technology's ModelSim EE/Plus 5.3a_p1 simulator. Note that the time scale for these simulations were set to 1ns/1ps. It is important to set the unused inputs of the DCM to logic 0 and to set the attribute values to the correct data types. For example, the PHASE_SHIFT, CLKFX_DIVIDE, and CLKFX_MULTIPLY attributes are integers and should be set to values as shown.

```
defparam U_DCM.DFS_FREQUENCY_MODE = "LOW";
defparam U_DCM.CLKFX_DIVIDE = 1;       (Any value from 1 to 4096)
defparam U_DCM.CLKFX_MULTIPLY = 4;     (Any value from 1 to 4096)
defparam U_DCM.CLKOUT_PHASE_SHIFT = "FIXED";
defparam U_DCM.PHASE_SHIFT = 150;      (Any value from 1 to 255)
defparam U_DCM.STARTUP_WAIT = "FALSE";
```

The input clock, 'clk_in' (CLKIN input of DCM) in all these waveforms is 50 MHz. The DCM_DLL waveforms in Figure 2-35 shows four DCM outputs, namely, clk1x (CLK0 output of DCM), clk2x (CLK2X output of DCM), clk90 (CLK90 output of DCM), and clk180 (CLK180 output of DCM).
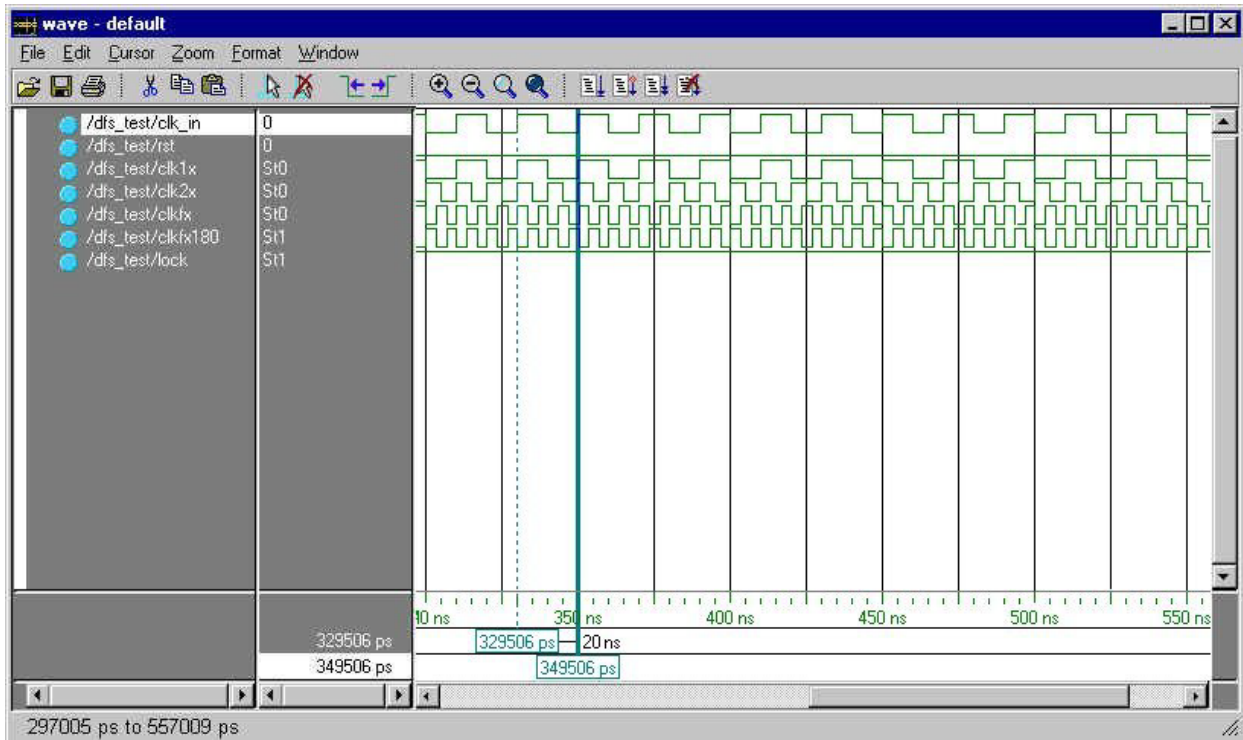

ug002_c2_095_113000

Figure 2-35: **DCM_DLL Waveforms**
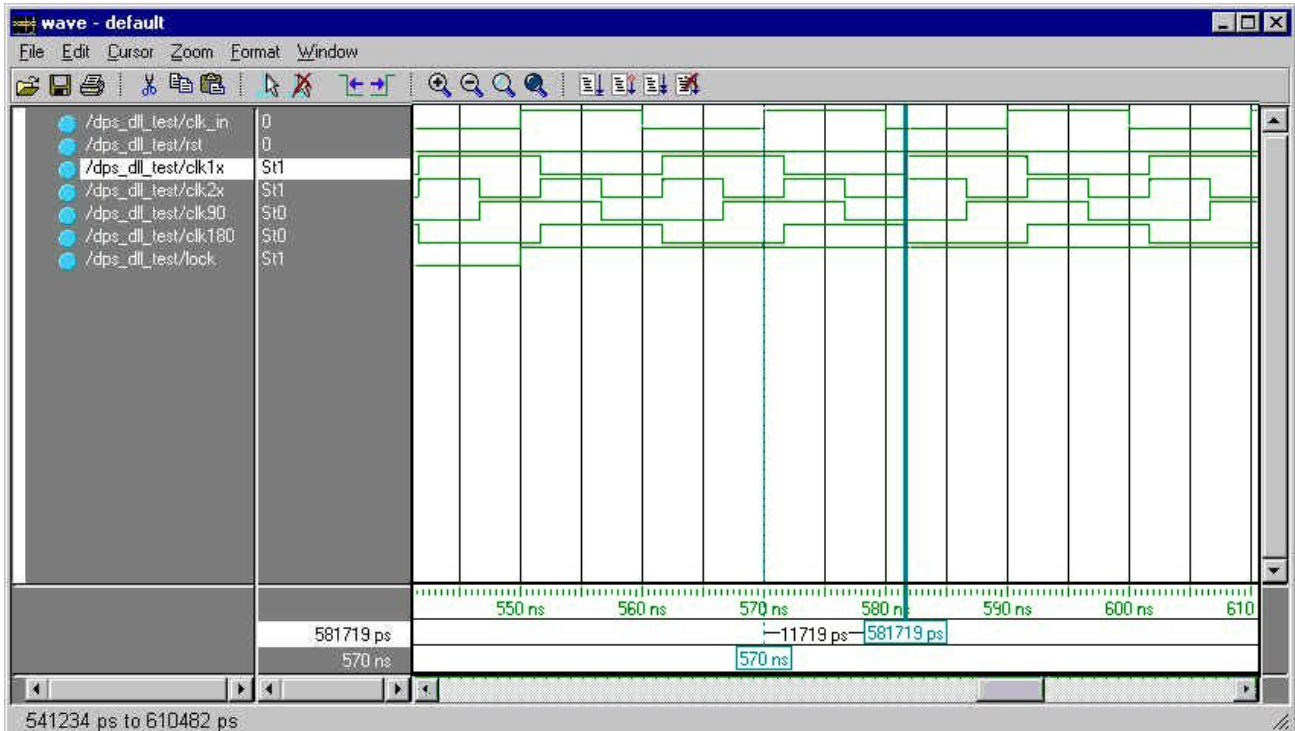
The DCM_DFS Waveforms in Figure 2-36 shows four DCM outputs namely, clk1x (CLK0 output of DCM), clk2x (CLK2X output of DCM), clkfx (CLKFX output of DCM), and clkfx180 (CLKFX180 output of DCM). In this case the attributes, CLKFX_DIVIDE = 1, and the CLKFX_MULTIPLY = 3.

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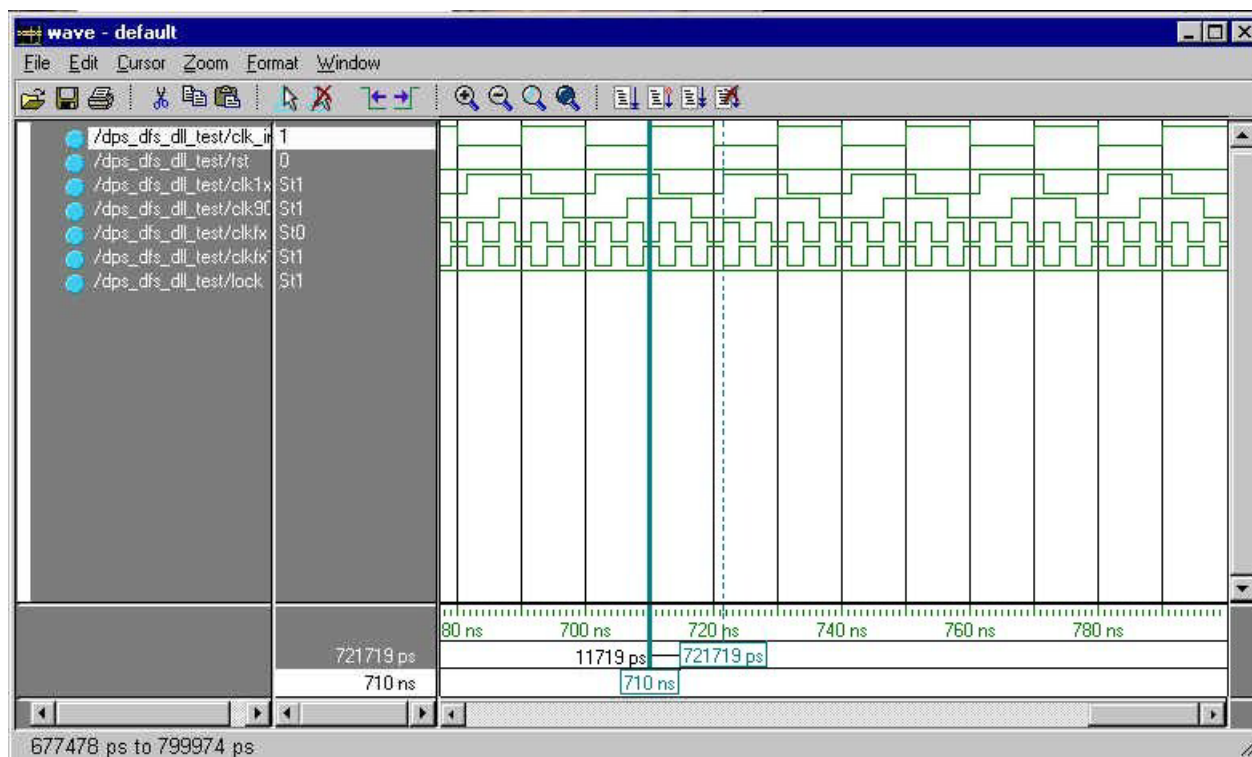*Figure 2-36:*   **DCM_DFS Waveforms**

The DCM_DPS waveforms in Figure 2-37 shows four DCM outputs, namely, clk1x (CLK0 output of DCM), clk2x (CLK2X output of DCM), clk90 (CLK90 output of DCM), and clk180 (CLK180 output of DCM). In this case, the attribute PHASE_SHIFT = 150 which translates to a phase shift of (150 x 20 ns)/256 = 11.719 ns, where 20 ns is the clock period.

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Figure 2-37:   **DCM_DPS Waveforms**

The DCM_DPS_DFS waveforms in Figure 2-38 shows four DCM outputs namely, clk1x (CLK0 output of DCM), clk90 (CLK90 output of DCM), clkfx (CLKFX output of DCM), and clkfx180 (CLKFX180 output of DCM). In this case, the attributes, CLKFX_DIVIDE = 1, and the CLKFX_MULTIPLY = 4. The attribute, PHASE_SHIFT = 150 which translates to a phase shift of (150 x 20 ns)/256 = 11.719 ns, where 20 ns is the clock period.

ug002_c2_098_113000

Figure 2-38:   **DCM_DPS_DFS Waveforms**