SelectLink™ Technology: Virtex Series High-Performance Communications Channel

Introduction

As the need for higher bandwidth continues to accelerate, external busses can easily be the bottleneck limiting system performance. To satisfy the need for high bandwidth, high-speed external bus ports using new signal standards and protocols are found in state-of-the-art memories, processors, and other integrated circuits. The Virtex series supports up to twenty high-performance single-ended and differential I/O standards on all of the I/Os through its SelectI/O+™ technology. The Xilinx exclusive SelectLink technology utilizes techniques similar to high-performance processor and memory devices to create a high-bandwidth Virtex-to-Virtex communication link. It accomplishes this task with resources that are standard on all Virtex FPGAs such as Delay Locked Loops (DLLs), True Dual-Port™ BlockRAM, and SelectI/O technology. The flexibility of the SelectLink technology allows system designers to customize the chip-to-chip communication channel ideal for their specific designs, leaving the remaining resources for other purposes.

SelectLink Features and Benefits

SelectLink technology enables Virtex designers to create a high-performance communication link between two Virtex devices. Capable of up to 80 Gigabits per second (Gb/s) total aggregate bandwidth using up to 256 I/O pins. Xilinx provides a web-based design tool allowing system designers to customize the internal and external busses, and the FIFO resources to their specific designs. The SelectLink design tool generates the Verilog codes and the test benches in seconds, for easy integration into the rest of the system. Xilinx exclusive SelectLink technology offers the following features and benefits.

- Source-synchronous Device Interface: The SelectLink technology uses a source-synchronous (clock forwarding) technique where the transmit clock is sent to the receiver along with the data. Since the transmit clock remains in phase with the data as both propagate to the receiver, very high speed data recovery at the receiver is achieved without errors due to set-up or hold violations.
- Unidirectional - Data is sent in one direction only on a single SelectLink channel, from one transmitter to one receiver. Two channels may be used for bi-directional operation. By using point-to-point interconnection, a very high data rate can be achieved with superior signal quality.
- Double Data Rate Technique: New data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements with this approach, making it attractive for very high-speed systems.
- Configurable Bus Widths: The width of the external inter-chip bus and the width of the internal FIFO is alterable to match the design requirements.
- Data Buffering: FIFO data buffers are included in both the transmitter and receiver modules. The depth of the FIFOs is configurable to match the design requirements.
- Data Flow Control: Flow control is built-in to the SelectLink channel. To the user, the transmitter and receiver ports appear to be the write and read ports of the same FIFO with the Full and Empty Flags. This feature provides a simple data flow control mechanism between the transmitter and receiver.
- Data Funneling and Expansion: The external bus can be configured to be equal to or less than half the width of the internal FIFO ports. By allowing the data to travel over a narrower external bus width SelectLink technology can save pins, power, noise, and interconnects.
- Fully Synchronous User Clocks - The user clocks in the transmitter and receiver FPGA are in phase with each other allowing the FPGAs to synchronously communicate with a third IC placed between them without the need for any external logic.

- Online Source Code Generation: The SelectLink design tool available at www.xilinx.com allows system designers everywhere to instantly create customized SelectLink Verilog source codes and test benches. The modules are easily instantiated in the designers' top level code for a complete system solution.
- Multiple Interface Connections: The SelectLink Channel is not limited to a particular electrical interface (physical layer), and can be used with any of the SelectI/O standards. For chip-to-chip interface, high-speed single-ended standards, such as SSTL or HSTL, can be used. For board-to-board interface, differential I/Os such as LVDS or LVPECL, can be used to provide noise immunity and EMI tolerance.
- Flexible Physical Layer Connection: The max data rate does not depend on the propagation delay of the physical layer. The physical layer connection may be any length, provided skew tolerance and signal integrity are maintained.

System Building Blocks

Figure 1 shows a system level block diagram with the two main modules in the SelectLink channel: Transmitter and Receiver.

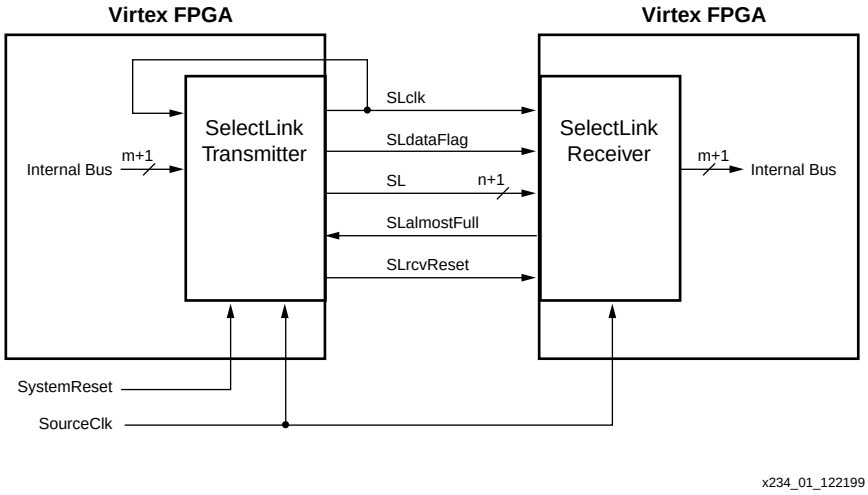

Figure 1: System Level Block Diagram

Transmitter Module

Figure 2 shows a block diagram for the Transmitter module.

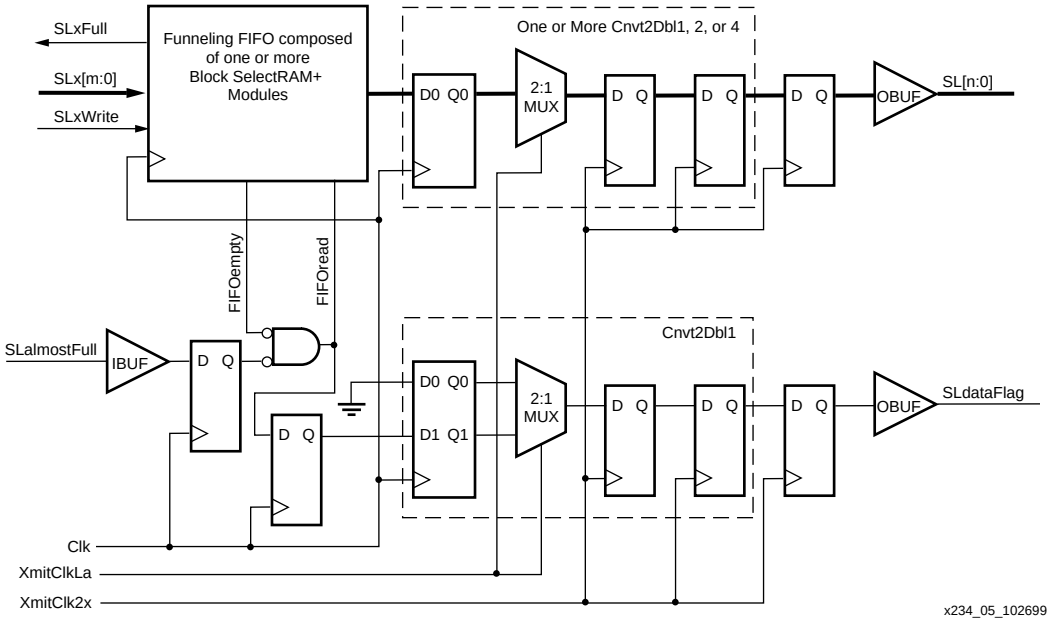

Figure 2: Transmitter Module Block Diagram

True Dual-Port BlockRAM is used in the transmitter module to create a data-width conversion FIFO that has different width write and read busses. This feature provides an efficient way to "funnel" internal data bus to a narrower external data bus. Words read from the FIFO are converted to double data rate (DDR) with module Cnvt2DblN. Multiple copies of the same Cnvt2DblN module are used to span the full width of the bus.

Figure 3 shows the details of clock generation in the transmitter module. The 2x clock is generated in the transmitter to create the double data rate stream. The DLL LOCKED status signals from the DLL are available to the user at the top level of the design hierarchy.

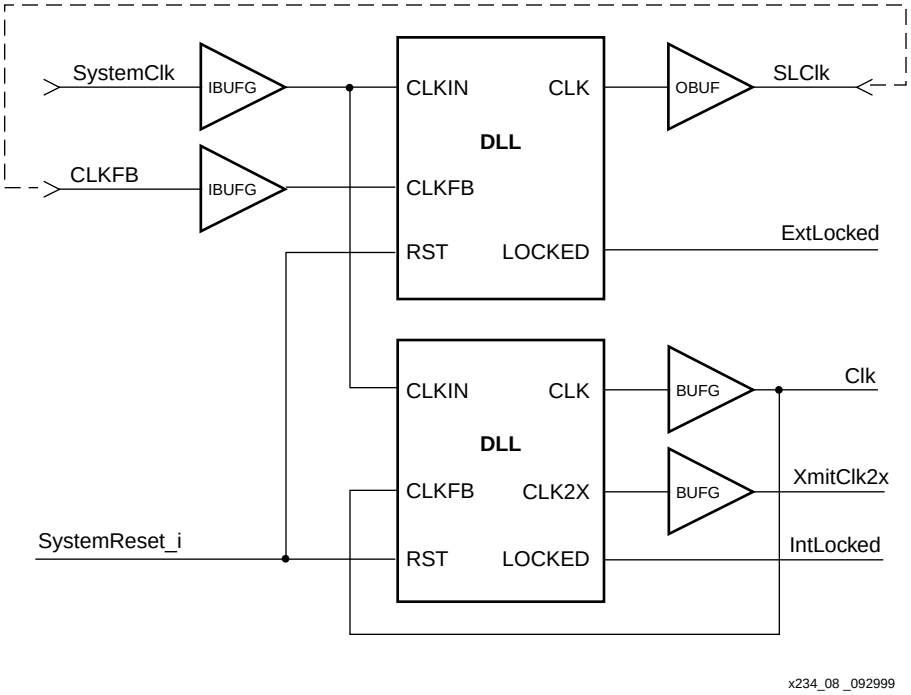

Figure 3: Transmitter Module Clock Generation

Receiver module

Figure 4 shows a block diagram for the Receiver module.

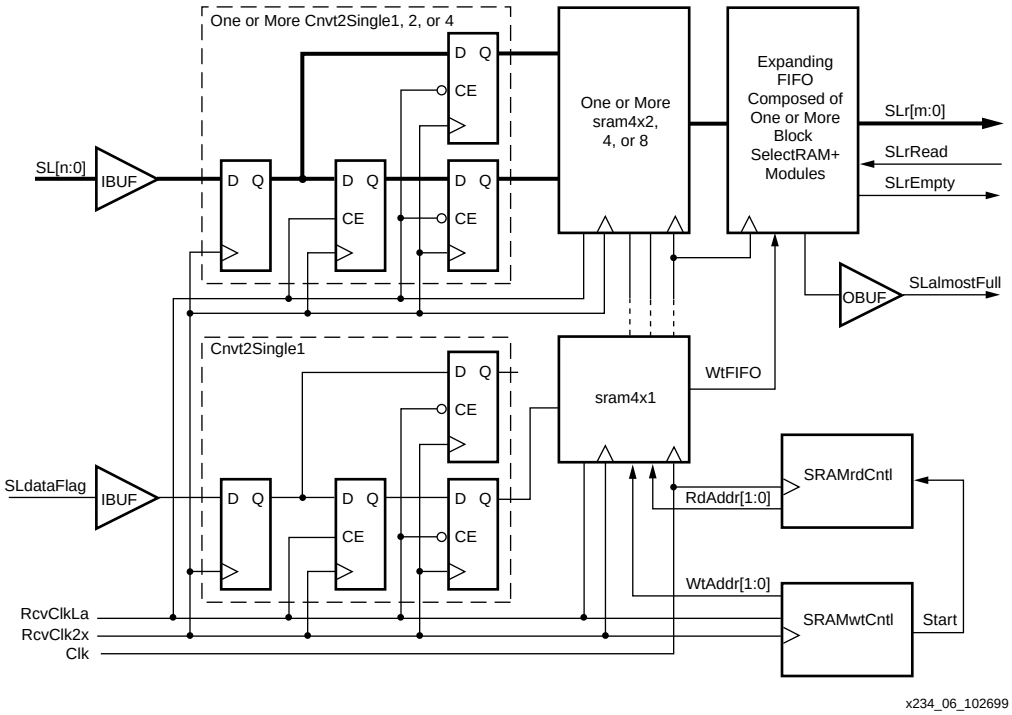

Figure 4: Receiver Module Block Diagram

The receiver module reverses the funneling and data rate conversions performed by the transmitter module. It also performs the necessary phase shifting of the data, which has been delayed by the data channel path, so that it again aligns with the signal clock.

The received data is converted from double to single rate with module Cnvt2SingleN. Multiple copies of the same Cnvt2SingleN modules are used to span the full width of the bus. A four-word deep FIFO, created with CLB flip-flops, is used to phase shift the data. Multiple copies of the same four-word deep FIFO are used to span the full width of the bus. After the data has been phase corrected, it is buffered and expanded to the full internal user bus width with a data-width conversion FIFO implemented with True Dual-Port BlockRAM.

Figure 5 shows details of clock generation in receiver module. The 2x clock is generated in the receiver to recover the double data rate (DDR) stream. The DLL LOCKED status signals from the DLL are available to the user at the top level of the design hierarchy.

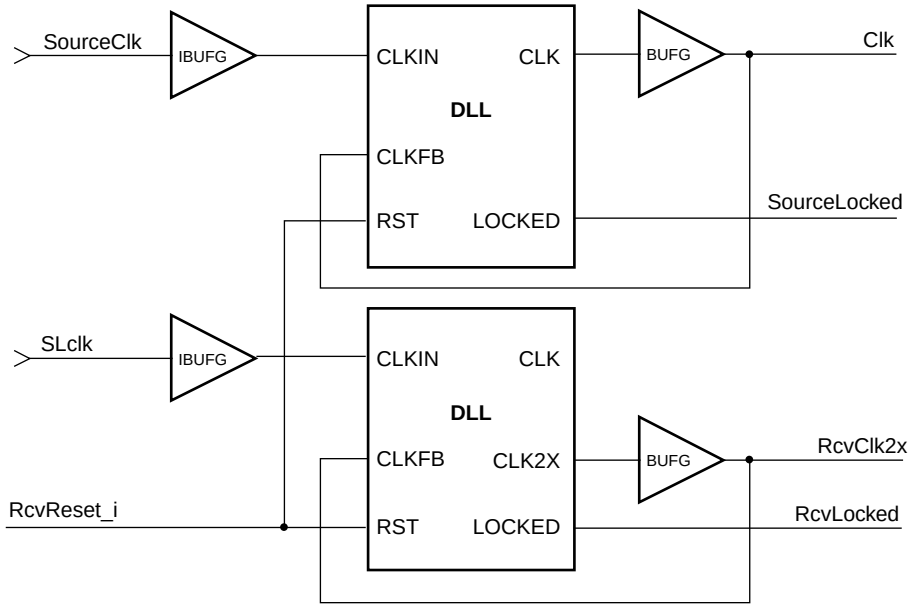

Figure 5: Receiver Module Clock Generation

System Performance

Table 1 lists the maximum SelectLink clock frequency that can be expected for the different Virtex/Virtex-E speed grades. While exact performance is determined only by implementing a complete design, this table may be used as a guideline.

Table 1: Maximum SelectLink Clock Frequencies

Family (Speed Grade)	Maximum f_{SLclk} (MHz)	Mbit/sec/pin
Virtex (-4)	70	140
Virtex (-5)	85	170
Virtex (-6)	100	200
Virtex-E (-6)	133	266
Virtex-E (-7)	155.5	311

The SelectLink latency is defined as the number of periods between the time a data is written on the SLx bus and the time it appears on the SLr bus. Latency is a function of the ratio of the internal and external bus widths, and the propagation time of the external bus. Table 2 shows latency as a function of bus width ratios when the external bus propagation time is less than one SLclk period. If the bus propagation time exceeds one period, add one to the value in Table 2 for each additional period, or portion thereof.

Table 2: Latency as a Function of Bus Width Ratio

Internal Width/External Width	Latency in SLclk Periods
2/1	11
4/1	12
8/1	14
16/1	18
32/1	26

Virtex Advantages

The SelectLink technology is a Xilinx exclusive technology that enables system designers to easily create a high-performance, high-bandwidth communication link between any two Virtex or Virtex-E devices. The web-based design tool generates the Verilog source code and the related test benches in seconds based on user-specified parameters customized for the particular system designs. No other PLD vendor offers similar technology to help designers reduce time-to-market while addressing high-bandwidth requirements for their system designs. With abundant flexibility to suit individual designs, SelectLink technology is capable of providing the following benefits.

- High-performance Virtex/Virtex-E communication link:
  - Programmable bandwidth of 300+ Megabit Per Second (Mb/s) per pin.
    - Up to 80 Gb/s total bandwidth
    - 19.2 Gb/s with 64-bit width using SSTL2
- DDR (double data rate) technique which allows clock and data lines to have equal bandwidth and signal quality.
- User friendly configuration interface to define the customized parameters:
  - Internal and external bus-widths
  - FIFO resources
  - I/O standards: LVDS, HSTL, etc.
- Proven pre-engineered designs to reduce Time-To-Market:
  - DDR, Clock Forwarding, DLL, FIFO, Funneling…
- Efficient web-based HDL generation methodology:
  - User enters internal and external bus-widths, FIFO resources, and I/O standard selection HDL modules generated in seconds

The Virtex series offers system designers the high-performance SelectLink technology that is easily customized using the web-based user-friendly design tool. This enables designers to take advantage of the reduced design cycle and high-performance communication link, delivering a high-bandwidth system design. More details of the SelectLink design tool can be found in the following location: **http://www.xilinx.com/applications/slcv/selectlink.htm**.

References

Related Xilinx Documents

XAPP234: "Virtex SelectLink Communications Channel" at:
http://www.xilinx.com/xapp/xapp234.pdf

XAPP133: "Using The Virtex SelectI/O" at: http://www.xilinx.com/xapp/xapp133.pdf

XAPP230: "The LVDS I/O Standard" at: http://www.xilinx.com/xapp/xapp230.pdf