IBIS: Description and Usage

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Introduction

The need for higher system performance leads to faster output transitions. Signals with fast transitions cannot be considered purely digital; it is important to understand their analog behavior for signal integrity analysis.

In order to simulate the signal integrity on printed circuit boards (PCB) accurately and to solve design problems before the PCB is fabricated, models of the I/O characteristics are required. SPICE models are most frequently used for this purpose. A manufacturer's SPICE models, however, contain proprietary circuit-level information. Therefore, simpler models are devised to extract SPICE parameters for the proprietary information to remain protected. One such standard is the I/O Buffer Information Specification (IBIS) format originally suggested by Intel.

In the early 1990's, the IBIS Open Forum was formed and the first IBIS specification was written to promote tool independent I/O models for system signal integrity analysis.

IBIS is now the ANSI/EIA-656 and IEC 62014-1 standard. IBIS accurately describes the signal behavior of the interconnections without disclosing the actual technology and circuitry used to implement the I/O. The standard is basically a black-box approach to protecting proprietary information.

IBIS Model

IBIS models are used by designers for system-level analysis of signal integrity issues, such as the evaluation and matching of loads to drivers for ringing and ground bounce, examining effects of cross talk, and predicting RFI/EMI. It is useful in that complete designs can be simulated and evaluated before additional costs are incurred for PCB fabrication and assembly time.

IBIS models consist of look-up tables that predict the I/V characteristics and dV/dt of integrated circuit inputs and outputs when combined with the PCB wiring. The predictions are performed for the typical case, minimum case (weak transistors, low V_{CC}, hot temperatures), and maximum case (strong transistors, high V_{CC}, cold temperatures).

IBIS models have limitations in that they do not contain internal delay modeling and are limited in package modeling. IBIS models contain package parasitic information for simulation of ground bounce. Although the data is available within the model file, not all simulators are able to use the data to simulate ground bounce. Simulation results may not agree with the actual results due to package, die, and PCB ground plane modeling problems. Similarly, because simultaneous switching outputs (SSOs) are also difficult to model, only a first approximation is provided to the designer.

IBIS Generation

IBIS is generated either from SPICE simulations, or actual measurements of final devices. IBIS models that are derived from measurements do not have process corner information, unlike IBIS models that are derived from SPICE simulations. The measurements are of only a few parts, and the extremes of production will not be represented by such a method.

SPICE is a transistor model based on detailed equations using device geometry, and properties of materials. A SPICE netlist of the CMOS buffer is required for V/I and dV/dt curve simulations. These SPICE simulations are then converted to IBIS format/syntax.

Advantages of IBIS

SPICE requires a greater knowledge of the internal workings of the circuits being modeled, and as such, errors may be made in simulation indicating a problem when there is none. IBIS models are easy to use, and because many of the decisions required for simulation parameters have been organized. IBIS simulations are faster compared to SPICE simulations, because IBIS does not contain circuit details. The voltage/current/time information provided in the IBIS model is only for the external nodes of the building block, making IBIS ideal for system-level interconnects design. Although IBIS models are not as accurate as SPICE models, they are entirely adequate for system-level analysis.

IBIS File Structure

An IBIS file contains two sections, the header and the model data for each component. One IBIS file can describe several devices. The following is the contents list in a typical IBIS file:

- IBIS Version
- File Name
- File Revision
- Component
- Package R/L/C
- Pin - name, model, R/L/C
- Model (i.e, 3-state)
- Temperature Range (typical, minimum, and maximum)
- Voltage Range (typical, minimum, and maximum)
- Pull-Up Reference
- Pull-Down Reference
- Power Clamp Reference
- Ground Clamp Reference
- V/I Tables for:
  - Pullup
  - Pulldown
  - Power Clamp
  - Ground Clamp
- Rise and Fall dV/dt for minimum, typical, and maximum conditions (driving 50 ohms)
- Package Model (optional) XXXX.pkg with RLC sections.

New Advanced Features in IBIS 3.2

- Multi-section uncoupled package description
  - Transmission line and package stubs
- Single-section (lumped) full-matrix coupled package description
- Electrical board description (EBD)
- Multi-stage buffer (Driver Schedule)
- Dynamic clamping and bus hold capabilities (on-die termination)
- Series pin-to-pin and FET bus switch modeling
- Model selector for programmable buffers
- Extended model specifications and simulation hooks
  - Ringback and hysteresis specification

Example IBIS File

```
|*****************************************************************
| Xilinx Virtex IBIS File
|*****************************************************************
|
[IBIS ver]       2.1
[File name]      virtex.ibs
[File Rev]       0.45
[Date]           Aug. 10, 1999
[Source]         Hspice simulations (23e: TT, SS, FF)
[Notes]          Xilinx IBIS model for Virtex I/O
The package models are provided for BG432, BG352, BG256, HQ240, PQ240, TQ144,
FG676 and FG680 package types, with BG432 being selected as a default. Please
make your own selection of the packages by commenting out the unused ones.
COMMENTS: Models include process corners for MIN and MAX.

[Disclaimer]     The data in this model is derived from SPICE simulations
using modeling information extracted from the target process. While a great
deal of care has been taken to provide information that is accurate, this
model is considered preliminary as it has not been verified by actual silicon
measurement. Treat the data in this model as preliminary until actual silicon
verification is performed.
[Copyright]      Copyright 1999, Xilinx Inc., All rights reserved
|
|*****************************************************************
|                    Component Virtex
|     >>> Make Your Selection of the Package type Below <<<
|*****************************************************************
|
[Component]      VIRTEX
[Manufacturer]   Xilinx Inc.
[Package]
| For Package type BG432:
| variable       typ                min                max
R_pkg            0.2500             0.1600             0.3500
L_pkg            4.9000nH           2.4000nH           7.4000nH
C_pkg            1.0500pF           0.8000pF           1.3000pF
|*****************************************************************
|                             Model LVCMOS2
|*****************************************************************
|
[Model]          LVCMOS2
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-Low
Vinl =   0.800V
Vinh =   1.700V
Vmeas =   1.2500V
Cref =  35.0000pF
Rref =   1.0000M
Vref =  0.000V
C_comp           6.5000pF           5.0000pF           8.0000pF
|
|
[Temperature Range]       27.0000            100.0000           0.000
[Voltage Range]          2.5000V            2.3750V            2.6250V
[Pulldown]
| voltage     I(typ)             I(min)             I(max)
|
  -2.5000       -0.9000mA          -0.6000mA          -1.1000mA
  -2.3000       -1.1000mA          -0.7000mA          -1.2000mA
  -2.1000       -1.3000mA          -0.9000mA          -1.5000mA
... continued|
```

```
[Pullup]
| voltage     I(typ)              I(min)              I(max)
|
  -2.5000        0.2940A             0.2246A             0.3536A
  -2.3000        0.2660A             0.2021A             0.3205A
  -2.1000        0.2371A             0.1795A             0.2865A
... continued|
[GND_clamp]
| voltage     I(typ)              I(min)              I(max)
|
  -2.5000       -0.8521A            -0.8613A            -0.8476A
  -2.4000       -0.7980A            -0.8100A            -0.7926A
  -2.3000       -0.7440A            -0.7588A            -0.7376A
... continued|
[POWER_clamp]
| voltage     I(typ)              I(min)              I(max)
|
  -2.5000        1.6880nA            22.4700nA            1.1640nA
  -2.4000        1.7460nA            22.2900nA            1.2220nA
  -2.3000        1.5720nA            22.1200nA            1.2220nA
... continued
```

IBIS I/V and dV/dt Curves

A digital buffer can be measured in receive (3-state mode) and drive mode. IBIS I/V curves are based on the data of both these modes. The transition between modes is achieved by phasing in/out the difference between the driver and the receiver models, while keeping the receiver model constantly in the circuit.

The I/V curve range required by the IBIS specification is $-V_{CC}$ to (2 x V_{CC}). This wide voltage range exists because the theoretical maximum overshoot due to a full reflection is twice the signal swing. The ground clamp I/V curve must be specified over a range of $-V_{CC}$ to V_{CC}, and the power clamp I/V curve must be specified from V_{CC} to (2 x V_{CC}).

The three supported conditions for the IBIS buffer models are typical values (required), minimum values (optional), and maximum values (optional). For CMOS buffers, the minimum condition is defined as high temperature and low supply voltage, and the maximum condition is defined as low temperature and high supply voltage.

An IBIS model of a digital buffer has four I/V curves:

- The pull-down I/V curve contains the mode data for the driver driving low. The origin of the curve is at 0 V for CMOS buffers.
- The pull-up I/V curve contains the mode data for the driver driving high. The origin of the curve is at the supply voltage (V_{CC} or V_{DD}).
- The ground clamp I/V curve contains receive (3-state) mode data, with the origin of the curve at 0 V for CMOS buffers.
- The power clamp I/V curve contains receive (3-state) mode data, with the origin of the curve at the supply voltage (V_{CC} or V_{DD}). For 3.3 V buffers that are 5 V tolerant, the power clamp is referenced to 5 V while the pullup is referenced to 3.3 V.

Ramp and dV/dt Curves

The Ramp keyword contains information on how fast the pull-up and pull-down transistors turn on/off. The dV/dt curves give the same information, while including the effects of die capacitance (C_comp). C_comp is the total die capacitance as seen at the die pad, excluding the package capacitance.

dV/dt curves describe the transient characteristics of a buffer more accurately than ramps. A minimum of four dV/dt curves is required to describe a CMOS buffer: pull-down ON, pull-up OFF, pull-down OFF, and pull-up ON. dV/dt curves incorporate the clock-to-out delay, and the length of the dV/dt curve corresponds to the clock speed at which the buffer is used. Each dV/dt curve has t = 0, where the pulse crosses the input threshold.

IBIS Simulations

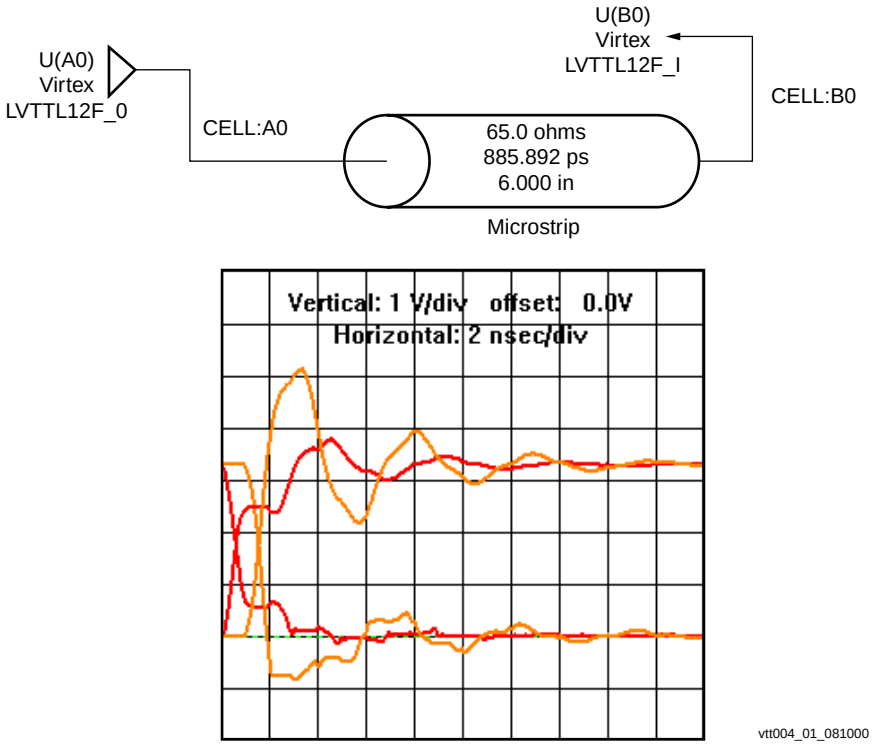

Figure 1: **Unterminated Example**

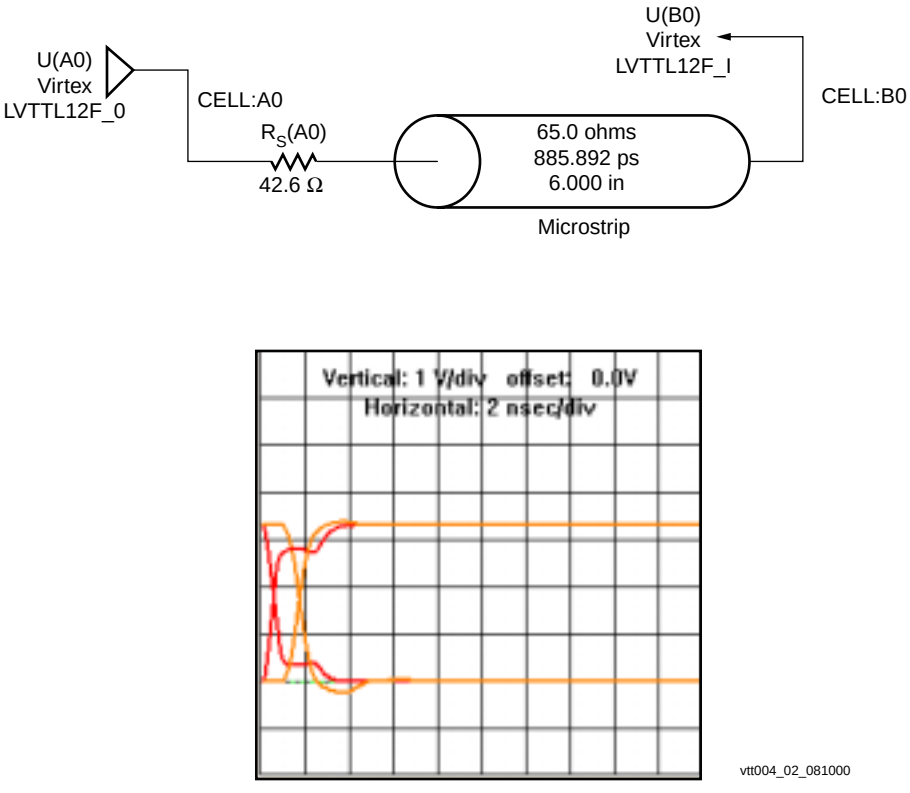

Figure 2: **Series Termination Example**

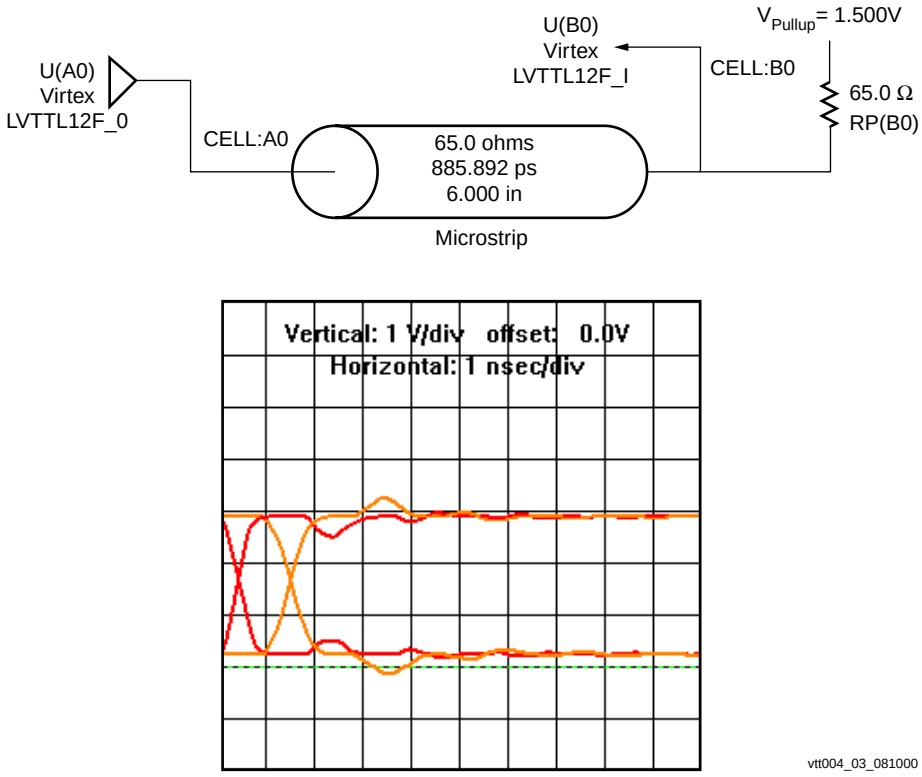

Figure 3: **Parallel Termination Example**

IBIS Simulators

Several different IBIS simulators are available today, and each simulator provides different results. An overshoot or undershoot of ±10% of the measured result is tolerable. Otherwise, the model must be modified based on measurements. Differences between the model and measurements occur, because not all parameters are modeled. Simulators for IBIS models are provided by the following vendors:

- Cadence
- Avanti Corporation
- Hyperlynx
- Mentor
- Microsim
- Intusoft
- Veribest
- Viewlogic

Xilinx IBIS Advantages

Xilinx provides preliminary IBIS files before tapeout, as well as updated versions of IBIS files after the ICs are verified. Preliminary IBIS files are generated from SPICE models before tape out. After the IC (device) is verified, appropriate changes are made to the existing IBIS files. These IBIS files are available to customers at the following web site:

http://www.xilinx.com/support/sw_ibis.htm

In comparison, Altera does not develop the IBIS models for their in-house devices. They utilize an outside service. The IBIS models are generated after the IC (device) is verified; as a result, they are not available to customers as quickly.

Reference

http://www.eia.org/eig/ibis/ibis.htm

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/22/00	1.0	Initial Xilinx release.