Virtex-II Digital Clock Manager

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Summary

This Tech Topic describes the Virtex™-II Digital Clock Manager (DCM) features, capabilities, benefits, and applications. The DCM is a complete system-level clock manager that simultaneously enables internal and external clock de-skew, high-resolution phase adjustment, and flexible frequency synthesis. A competitive analysis of the Virtex-II DCM versus Altera's Apex 20KE PLL is also included.

Introduction

Higher system bandwidth calls for high data rates between devices requiring advanced clock management systems. High frequency clocks on printed circuit boards (PCBs) result in greater signal integrity issues, e.g., electromagnetic interference (EMI) and crosstalk. In designs requiring multiple high frequency clocks, reduction of the number of high frequency clocks on the PCB can be achieved with clock management circuitry. The Digital Clock Manager (DCM) in Virtex-II devices serves this purpose. The DCM simultaneously enables de-skew of both internal and external clocks, high-resolution phase adjustment, and flexible frequency synthesis accessed in a single DCM.

DCM Features

The Virtex-II DCM provides a complete on-chip and off-chip clock generator(s), offering powerful clock management features:

- **Clock De-Skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM uses fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also uses fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four DCM clock outputs can drive global clock multiplexer buffer inputs simultaneously. All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers. In addition, the DCM output can be used to generate board-level clocks.

The configuration DONE signal indicates the completion of configuration of the Virtex-II device. This DONE signal can be delayed until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked
- STATUS output pins: active High

Clock De-Skew

Synchronous systems depend on precise clock distribution for high performance. The de-skew circuitry of the DCM ensures low skew clock signal distribution both within the Virtex-II device (using the clock distribution network) and externally on a system/board level.

The Virtex-II DCM offers a fully digital, dedicated on-chip de-skew circuit providing zero propagation delay, low clock skew between output clock signals distributed throughout the device and advanced clock domain control. DCMs can be used to implement several circuits that improve and simplify system level design.

Figure 1 shows all of the inputs and outputs of the DCM including control/status signals.

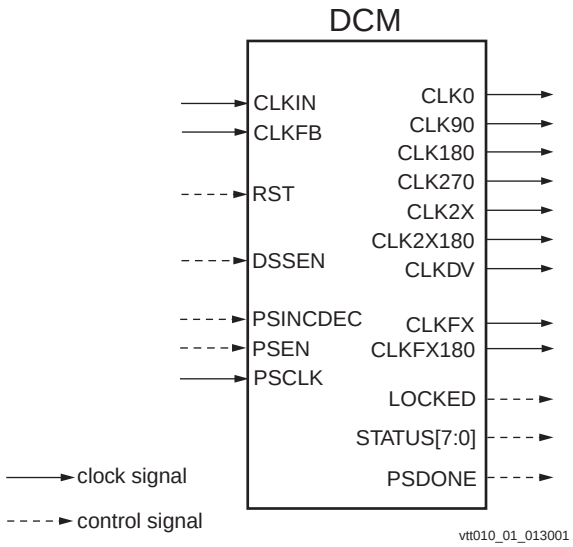

Figure 1: **DCM Block Diagram**

The de-skew feature can also act as a clock mirror. By driving the CLK0 or CLK2X output off-chip and then back again as input, the de-skew feature can be used to de-skew a board-level clock serving multiple devices. By taking advantage of the de-skew circuit to remove on-chip clock delay, the designer can greatly simplify and improve system-level design involving high-fanout, high-performance clocks.

The well-buffered global clock distribution network minimizes clock skew, regardless of loading differences. By monitoring a sample of the output clock (CLK0 or CLK2X), the de-skew circuit automatically compensates for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device. Figure 2 shows the waveforms of the de-skew outputs with an input frequency of 100 MHz.

Frequency Synthesis

System performance increases with new technology leading to the need for system clock multiplication and division. Frequency synthesis in the DCM offers the designer flexibility to choose a multiplication and division factor ranging from 1 to 4096. This feature can help reduce the number of high-speed system-level clocks. Frequency synthesis enables a single system-level clock to be used to generate any frequency within the operating range.

Basic frequency synthesis is also available in the DCM, for example, clock doubling (CLK2X, CLK2X180), or clock division (CLKDV) of the user source clock by up to 16. The divisors can be 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, or 16.

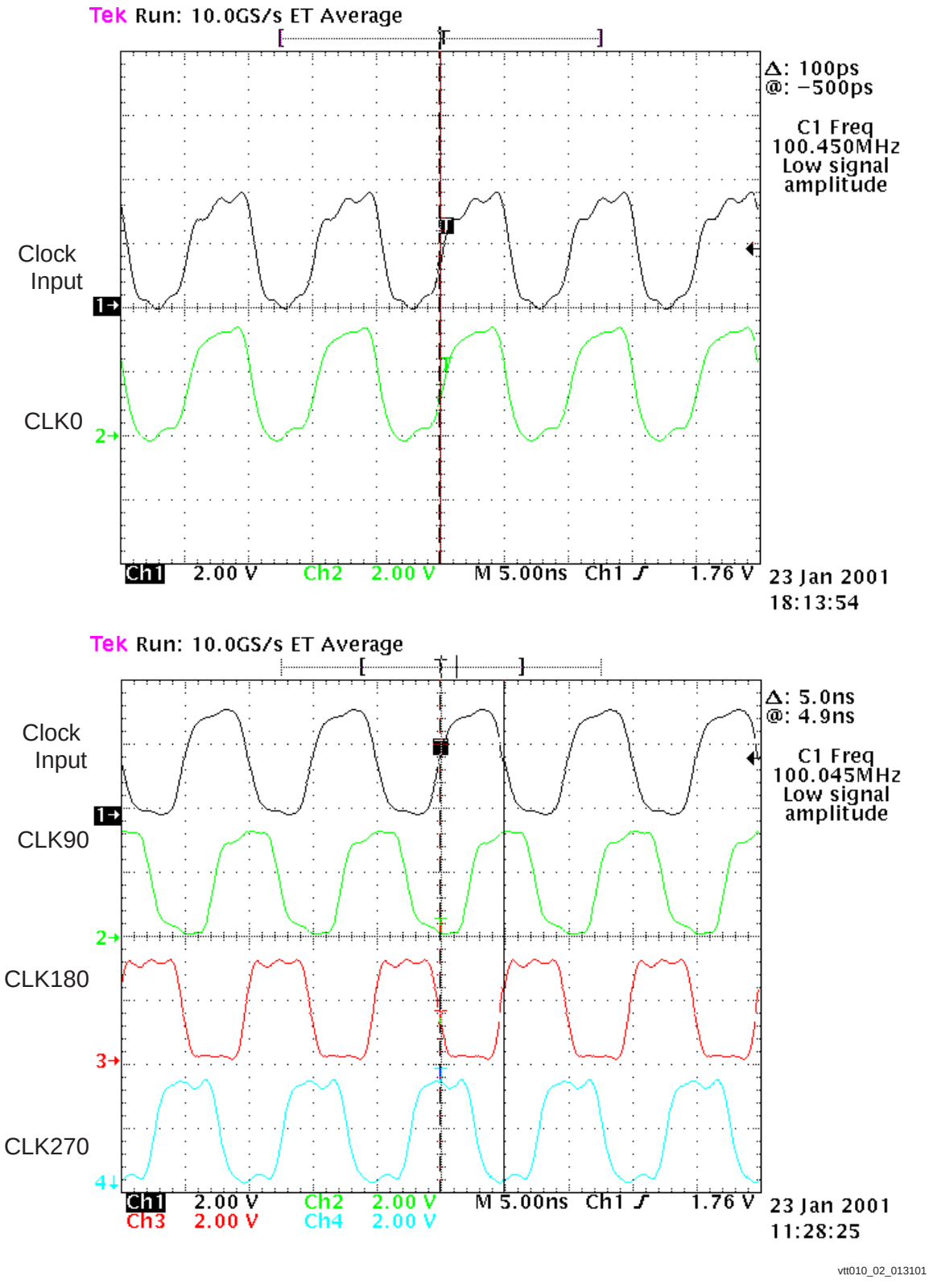

Figure 2: **DCM De-Skew Outputs**

Clock multiplication provides a number of design alternatives. For instance, a 100-MHz source clock doubled by the DCM can drive an FPGA design operating at 200 MHz. This technique simplifies board design because the clock path on the board no longer distributes such a high-speed signal. This results in lower signal integrity issues on the board. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

Flexible Frequency Synthesis is implemented by using the CLKFX and CLKFX180 outputs. The frequency of these clocks equals the input clock frequency multiplied by M/D. M, the numerator, is the multiplication factor and D, the denominator, is the division factor.

These two counter-phase frequency synthesized outputs can drive global clock routing networks within the device. The well-buffered global clock distribution network minimizes clock skew due to differences in distance or loading.

Input and output frequency ranges are specified in the data sheet. To de-skew these outputs, a feedback must be provided to the CLKFB input of the DCM (either CLK0 or CLK180).

As an example, input frequency = 50 MHz, M = 333, D = 100 (note that M and D values have no common factors and, hence, cannot be reduced). The generated output frequency is correctly 166.50 MHz, even though 333 x 50 MHz = 1.665 GHz and 50 MHz/100 = 500 kHz are both far outside the range of the frequency output.

Figure 3 shows the waveforms of the frequency synthesized outputs with M=3 and D=1 and an input clock frequency of 100 MHz.

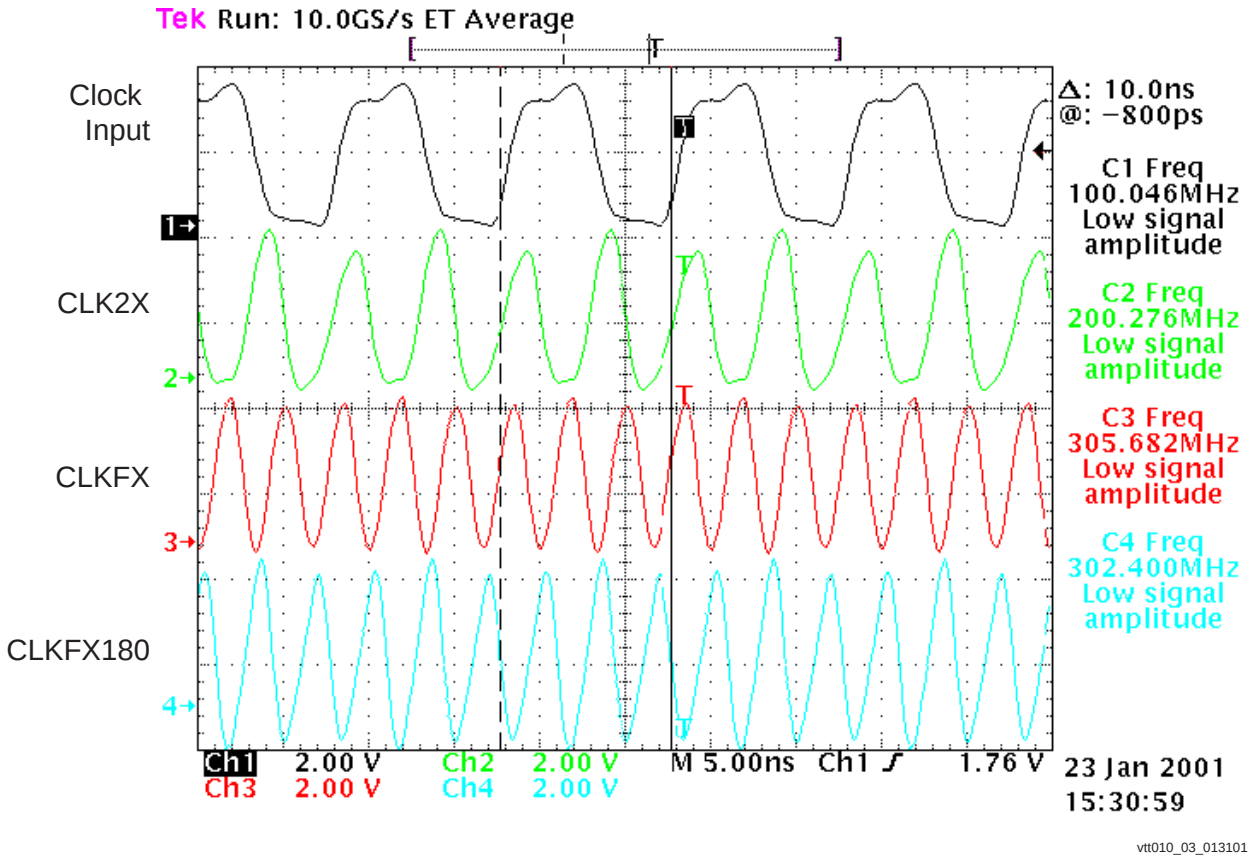

Figure 3: **DCM Frequency Synthesized Outputs**

Phase Shifting

High-resolution phase shifting can be used to adjust setup and hold times of I/Os. The DCM also provides quadrature phases of the source clock (CLK0, CLK90, CLK180, and CLK270) which can be used simultaneously. The DCM self-adjusts to maintain a constant and precise phase shift across temperature and voltage.

Fine phase shifting affects all the outputs of the DCM. A phase-shifted output with a resolution of 50 ps or 1/256th of the input clock period can be created. The phase shift can be fixed (established by configuration) or dynamically adjusted after configuration. The dynamic phase adjustment feature can be used to optimize clock-to-out by adjusting the setup and hold times, while the system is running. Figure 4 shows the phase shift effects in the fixed and variable modes of operation.

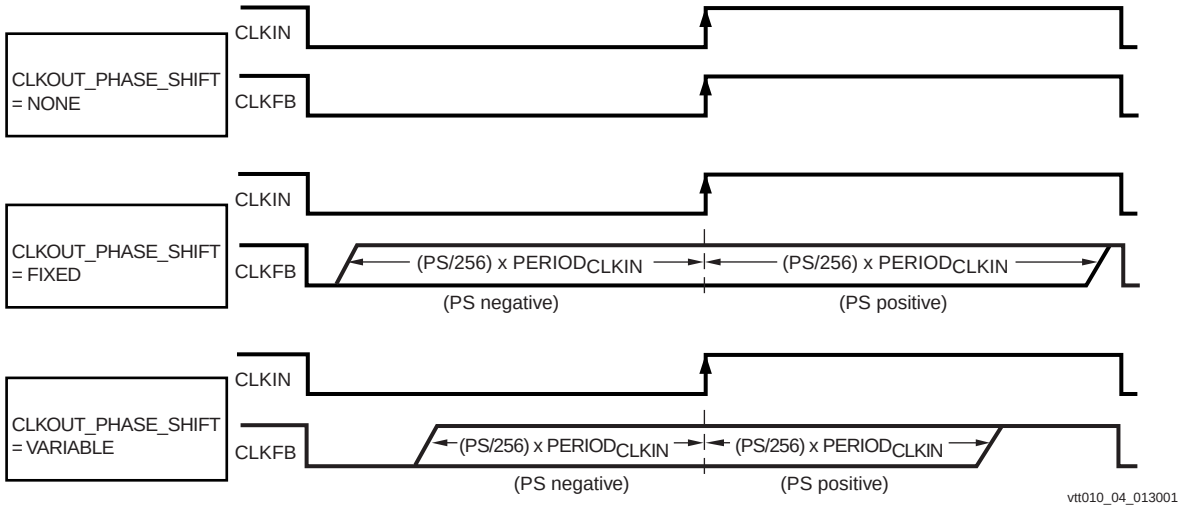

Figure 4: **Phase Shift Outputs**

The equation for the phase shift is as follows:

CLKIN_CLKFB_skew = (Phase Shift/256) x PERIOD CLKIN

The user interface describes the phase shift as a fraction of the clock period (N/256). The phase shift granularity is the greater of the two limiting factors, namely, minimum delay line step size (~50 ps) and minimum phase shift step size (1/256 x input clock period). The maximum phase shifting range is the lesser of the two limiting factors, namely, maximum delay line range (~10 ns for FIXED mode and ~5 ns for VARIABLE mode), and maximum phase shift range (255/256 = ~1 clock period).

Figure 5 shows the phase shift in the DCM de-skew outputs with a phase shift value of 33 ((33 x 10 ns)/256 = 1.3 ns, where 10 ns is the clock period). Figure 6 shows the waveforms of DCM outputs with both the phase shift and the frequency synthesis feature being used simultaneously. InFigure 6, the phase shift value is -30 ((30x 10 ns)/256 = 1.2 ns, where 10 ns i s the clock period) and M = 5, D = 3.

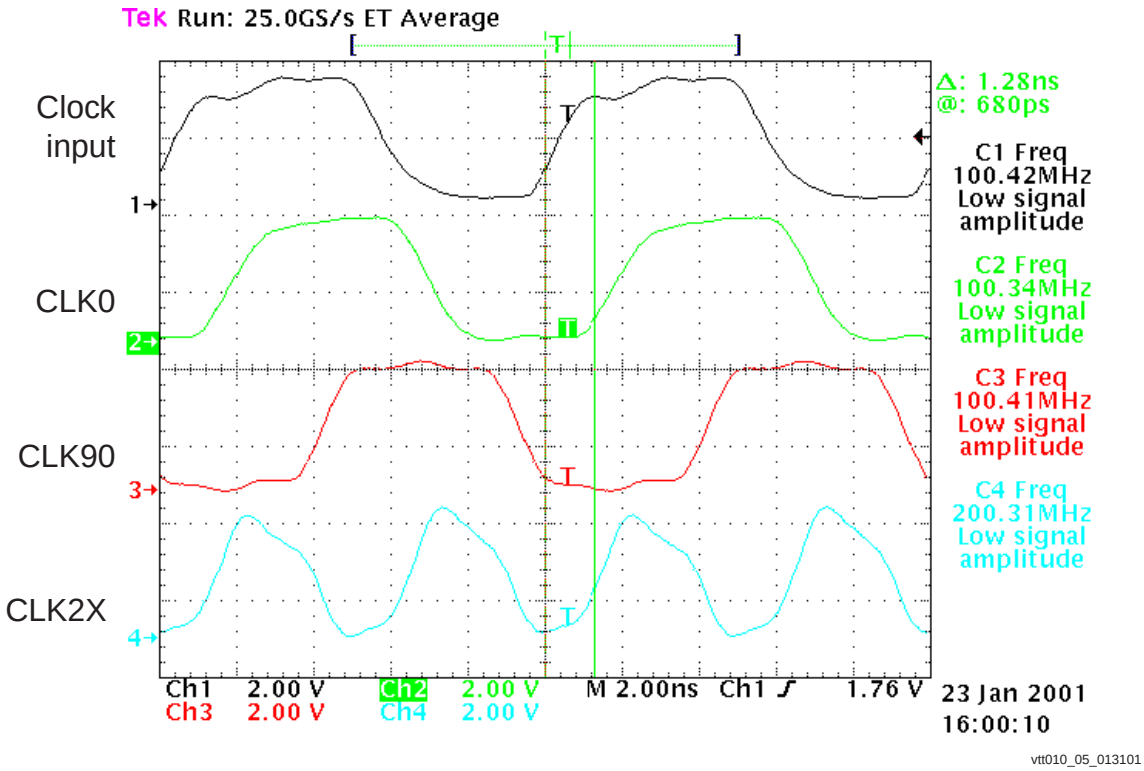

Figure 5: **DCM Phase Shifted Outputs**

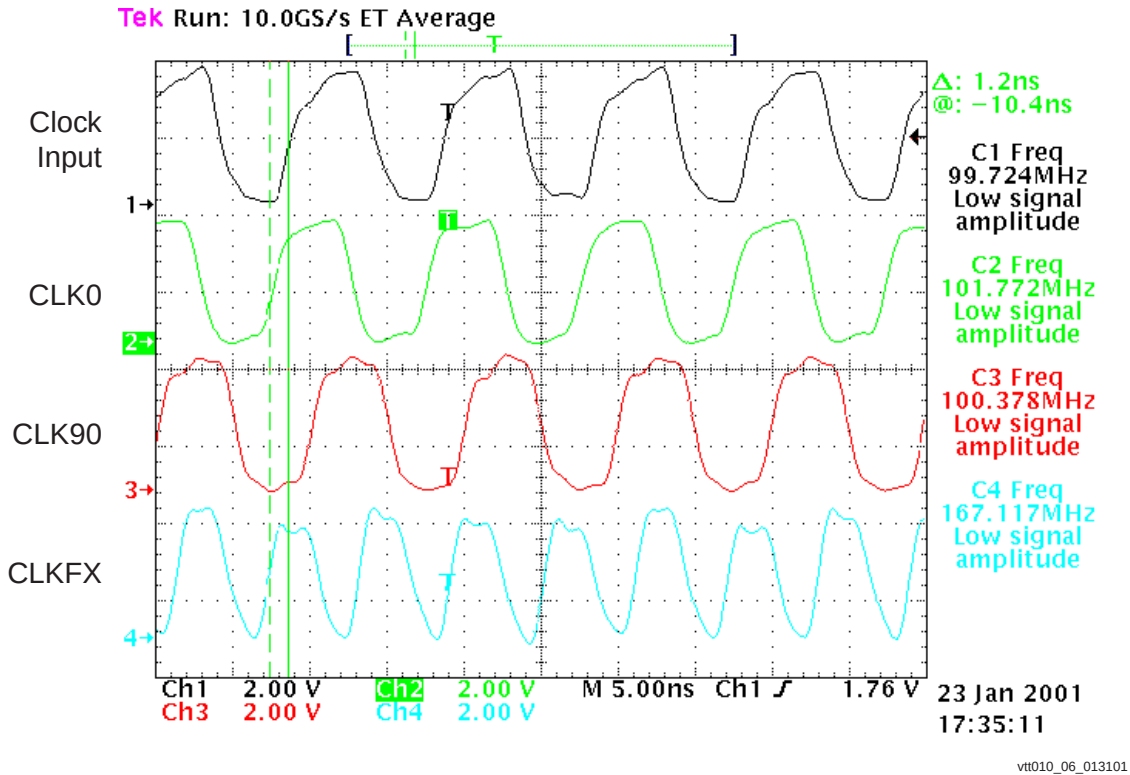

Figure 6: **DCM Phase Shiftd and Frequency Synthesized Outputs**

DCM Applications

The advanced frequency synthesis feature can be used to generate frequencies in the following key applications:

- 10b/8b, 100 MHz input and 125 MHz output
- FEC code rates, e.g., 528/512, 8/7

The phase shifter high-resolution phase adjustment feature can be used for:

- Modifying clock-to-out
- Maximizing setup and hold time margins
- Clock and data recovery in logic plane for OC-3 and A/B
- Master/slave, hot/standby switching

Competitive Analysis

The following is a competitive analysis of the Virtex-II DCM versus Altera's Apex 20KE PLL:

- **Clock De-Skew**: The Virtex-II DCM de-skews clocks to within ±150 ps. There is currently no spec for the APEX 20KE PLL de-skew accuracy. Creating de-skewed external clocks (clock mirroring/forwarding) with the APEX 20KE PLL is very limited: no phase shifting and no clock multiplication is allowed; also, clk2out delay plus board trace delay for the feedback clock must be less than the lesser of 5 ns or 1/2 the clock period. The DCM has no restrictions on the delay in the feedback clock path. The DCM also allows all DCM features to be used whether performing an internal or external de-skew.
- **Clock Frequency**: In the APEX 20KE PLL, the M/D ratio cannot be greater than 133. The Virtex-II DCM can multiply up from its minimum input clock frequency to its maximum output clock frequency (> 300x). In the APEX 20KE PLL, a single additional special synthesis rate is provided for T1/E1 conversion (193/256 or 256/193).
- **Phase Shift**: Both APEX 20KE PLL outputs have identical phase shifts and only one of 90, 180, or 270 can be used at a time. All four Virtex-II DCM coarse shifted outputs of CLK0, CLK90, CLK180, and CLK270 can be used simultaneously (note that CLK90 and CLK270 are available only in low-frequency mode).
- **Fine Phase Shifting**: In the APEX 20KE PLL, “fine” phase shifting is available down to 0.4-1.0 ns resolution. This resolution varies with input clock frequency, M and D values, and possibly with environmental conditions. In the Virtex-II DCM, fine phase shifting is available at a precise resolution of 50 ps or 1/256th of the input clock period (whichever is greater, and never exceeding ~180 ps) and has zero variation with M and D values or with environmental changes (temperature and voltage). Additionally, the APEX 20KE PLL “fine” phase shifting can be used only on frequency synthesized clocks for which M/D or D/M is an integer. The DCM fine phase shift feature works for all DCM outputs, regardless of the M and D values or other settings.
- **Dynamic Phase Adjustment**: The Virtex-II DCM is the only FPGA clock management solution to offer dynamic phase adjustment (fine phase adjustment after configuration).
- **Clock Management**: Virtex-II FPGAs offer 12 DCMs in parts 2v3000 and larger, 4 DCMs in the smallest parts (2v40 and 2v80), and 8 DCMs in the mid-range parts. APEX 20KE offers 4 PLLs in parts EP20K300E and larger, 2 PLLs in smaller parts.
- **Global Clock Network**: In Virtex-II FPGAs there are 16 total global clock nets, with 8 being simultaneously available within each quadrant. Each Apex 20KE device has a total of 4 global clock nets.
- **Clock Outputs**: All nine clock outputs from each Virtex-II DCM can be brought to external pins. Any four clock outputs from each DCM can drive global clock nets. There are only two clock outputs available from each APEX 20KE PLL. Each PLL output can drive only one global clock net. Additionally, only 1/2 of the PLLs can drive external pins, and each of those “special” PLLs can drive only one external pin each (only for a frequency below the normal PLL maximum output frequency). In Virtex-II devices, every DCM output has access to all eight global clock nets on its edge of the device. Additionally, every DCM output can drive one or more external pins, and do so within its full operating range.

- **PCB Design Considerations**: The Virtex-II DCMs require no special PCB board design considerations beyond normal considerations for routing high speed signals. The APEX 20KE PLLs require extensive care to be taken with PCB board design. There is a dedicated VCC and GND pin pair for each PLL and for each PLL output clock. These pins must be connected to isolated VCC and GND traces on the PCB board. This isolation requires either A) separate VCC and GND planes in the PCB board that are isolated from the VCC and GND planes used for digital logic, or B) partitioning of the existing VCC and GND planes to provide “islands” (surrounded by dielectrics of at least 100 mil width) for each VCC and GND pin pair.

  Additionally, APEX 20KE PLL PCB board design requires a 10 µF tantalum capacitor and a ferrite bead (the impedance value of which depends on the clock frequencies being used) to be placed in a specific location on the board for decoupling these isolated VCC and GND traces. Furthermore, each VCC and GND pin pair must be decoupled with three more specified capacitors.

  All of this care is required in order for the PLL output clocks to meet the listed operating specifications. Again, the Virtex-II DCMs, which are completely digital circuits, require no such PCB design complexities and additional expense.
- **DLL Circuit Input**: In the Virtex-II DCM, the Delay-Locked Loop (DLL) circuit can accept input clock frequencies from 24-420 MHz, and the frequency synthesized circuit can accept input clock frequencies from 12-320 MHz. Within the overlap of these ranges (24-320 MHz), the DLL and DFS can be used simultaneously, achieving de-skew of the DFS clock outputs. The input clock frequency range for the APEX 20KE PLL is 1.5 - 160 MHz.
- **DLL Circuit Output:** In the Virtex-II DCM, the DLL circuit can output clock frequencies from 1.5-420 MHz, and the DFS circuit can output clock frequencies from 24-320 MHz. In the APEX 20KE PLL, one output has a range from 1.5-200 MHz, the other a range from 20-200 MHz. The PLL is limited to 150 MHz for external clock outputs. With certain PLLs, a few select higher frequencies are available internally when using Low Voltage Differential Signaling (LVDS).
- **Duty Cycle Accuracy**: The Virtex-II DCM output clocks have 50/50 duty cycles to within ±200 ps (For CLK0, CLK90, CLK180, and CLK270, duty cycle correction can be disabled with an attribute). There is no published spec for APEX 20KE PLL output duty cycle accuracy.
- **Jitter**: The Virtex-II DCM CLK0 output offers the lowest output jitter of any FPGA-based clock management solution. It adds no more than ±100 ps of jitter to its input clock. Other DCM clock outputs can have larger output jitter; characterization is still underway. The DFS outputs, in particular can have up to ±400 ps of jitter (total, not additive) depending on the M and D values and the jitter of the input clock. The lowest total jitter that the APEX 20KE PLL can offer i±250 ps, assuming an input clock with < 100 ps of jitter.
- **Output Clock De-Skew**: The Virtex-II DCM output clocks are de-skewed to within ±200 ps. There is no published spec for APEX 20KE PLL output clock de-skew accuracy.
- **Lock Time**: In the Virtex-II DCM, the DLL circuit still locks within 120 µs at its lowest frequency, and faster for higher frequencies. Although the APEX 20KE PLL lock time is less, the PLL begins to lock only after the device has finished configuring. The DCM begins locking during configuration and, in most cases, completes before the device has finished configuring. Note that the DFS circuit can require longer lock times for large M values.

References

Source from the Altera web site:

- “Using the ClockLock and ClockBoost PLL Features in APEX Devices,” Application Note 115, October 2000, ver. 2.01

DCM Summary

A Phase Locked Loop (PLL) can remain in lock only over a narrow range of frequencies, depending on the resonator. For a crystal-based PLL, this range is less than 200 ppm. For an LC tank-based PLL, this range is less than a few percent. For an RC oscillator-based PLL, this range is less than 20 percent.

The de-skew circuitry can be used for quadrate phase adjustment in addition to clock de-skew. All of the above features can be accessed simultaneously in a single DCM.

The de-skew circuitry of the DCM can track frequencies that change up to a maximum limit of less than 1 ns cycle to cycle.

The operation of a PLL is affected by voltage, temperature, and shot noise in its oscillator. Therefore, PLLs require special power and ground pins and external networks on the PCB.

The DCM is a digital signal processor, processing phase information every clock cycle with completely predictable results. When operating within the specified environmental limits, the DCM is not affected by voltage and temperature changes. Unlike a PLL, the DCM does not require special power and ground pins or external networks on the PCB.

The dynamic high-resolution phase shifting feature of the DCM makes Virtex-II devices the only FPGAs in the industry to offer a superior clock management solution. The smaller density Virtex-II devices could be used just for the DCM replacing devices, such as the Cypress RoboClock, or the IDT's TurboClock. See Table 1.

Table 1: **Virtex-II DCM Phase-Shifting Features**

Feature	Virtex-II DCM	CYPRESS Roboclock+ CY7B9911V
Maximum Frequency	420 MHz	110 MHz
Output Skew Range	±360^{o} (Full Period)	18 ns
Skew Resolution	Period/256	~1 ns/step
In-System Adjust	Yes	No
Device Integration	Up to 12 DCMs Integrated On-Chip	32-pin PLCC
Customer Value	Higher Performance Increased Flexibility Higher Integration	

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/01/01	1.0	Initial Xilinx release.