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XCITE™ Technology: Digitally Controlled Impedance (DCI)

Summary

This Tech Topic discusses the use of Xilinx Controlled Impedance Technology (XCITE™), the world's first Digitally Controlled Impedance (DCI), as the Virtex-II solution to ensure optimal signal integrity. XCITE technology improves system performance, resolves PCB design challenges, enhances reliability, and lowers cost.

Introduction

Optimal signal integrity is a requirement for maximum system performance. As performance demands increase, more time and effort must be spent on the printed circuit board (PCB) design to ensure the necessary level of signal integrity for the desired I/O bandwidth. Nearly all high-speed I/O standards now require that PCB traces be designed with a specific impedance. In addition, these standards require termination resistors of precise values on each I/O pin to match the trace impedance. Impedance matching eliminates the reflections and ringing that degrade signal integrity and affect system performance.

The PCB design challenge is further complicated by increased device I/O counts. Devices with several hundred I/Os are now commonplace. Placing termination resistors on each of these I/Os within reasonable proximity to the device is a daunting, if not impossible PCB layout task. External termination schemes can also necessitate additional board layers, resulting in higher board cost and development time.

XCITE eliminates the need for external termination resistors by incorporating adaptive series and parallel termination resistors on the FPGA itself. The on-chip resistor values are completely user definable via an external pair of reference resistors. The digital implementation of this technology guarantees that the on-chip resistor values do not vary when temperature or supply voltage shifts. XCITE also reduces board size and increases overall system reliability by eliminating potentially thousands of external resistors.

DCI Description

The idea of putting termination resistors on-chip is not entirely new. However, implementations in the past involved fixed resistances which suffered from very high tolerances due to temperature and process variations. As a result, these solutions were not effective at matching impedances precisely enough to ensure adequate signal integrity. XCITE solves this problem by using an adaptive termination scheme, whereby the XCITE circuit probes two external reference resistors to constantly adjust the termination impedance for all DCI I/Os.

Adaptive termination resistors are achieved by enabling or disabling varying numbers of parallel resistors in the I/O Block (IOB). External reference resistors of value equal to the characteristic impedance of the PCB trace are constantly measured against the resistance of the XCITE termination. During startup, a coarse impedance adjustment is made, matching the XCITE termination value to that of the reference resistor. This accounts for process variation. During device operation, fine adjustments are continually made to compensate for temperature and voltage variations.

XCITE termination, available on both inputs and outputs, can be configured in parallel and series schemes. It is even possible to parallel terminate to a half-level voltage (as in HSTL I and HSTL II). Figure 1 and Figure 2 illustrate the available DCI terminations.

Another benefit of on-chip termination is the proximity of the termination relative to its associated I/O. For a termination resistor to be effective, it must be very close (within 1 cm) to the I/O it is terminating. Distances greater than this cause stub reflection due to impedance

mismatch. Achieving this short distance with a package that has over 1100 I/Os is impractical (e.g., FF1517 package). Since XCITE brings termination onto the die itself, impedance is matched over the full length of the signal path, making signals reflection-free.

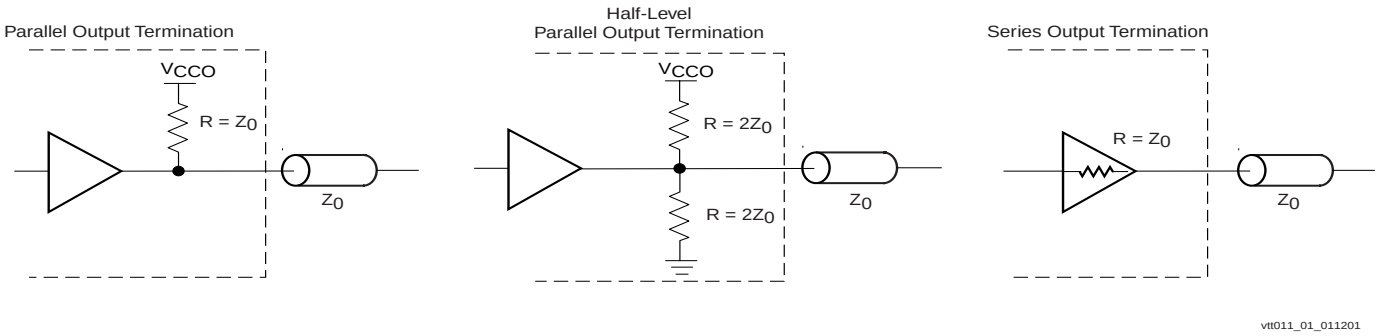

Figure 1: **DCI Output Terminations**

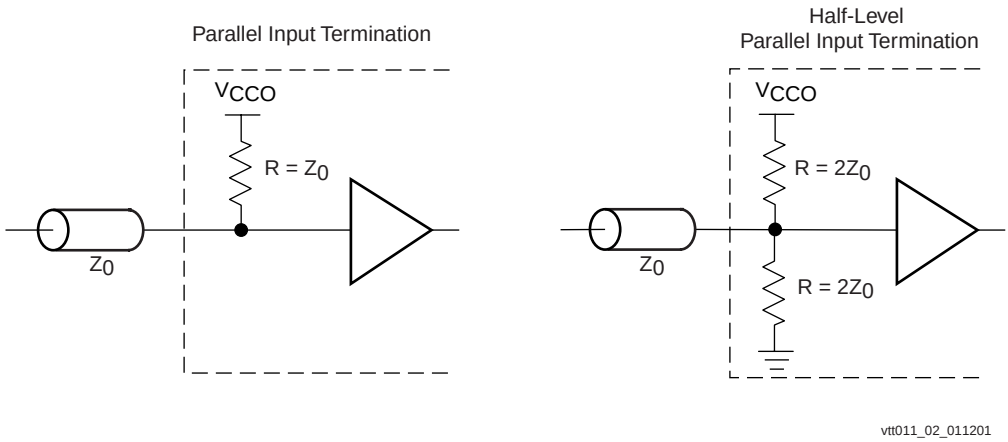

Figure 2: **DCI Input Terminations**

Virtex-II Advantages

The Virtex-II FPGA series offers DCI I/O on *all* user I/O pins. XCITE technology provides these significant system benefits:

- **Maximum I/O Bandwidth**: Incorporating adaptive termination resistors on-chip guarantees the highest level of signal integrity, which directly translates to higher I/O bandwidth.
- **Board Cost Reduction**: The PCB traces and vias necessary to support discrete resistors can as much as double the complexity of a board. This increases the number of signal layers and, consequently, the board designer's layout time. Board real estate is also affected, and together these factors drive up the cost of a board. DCI reduces the complexity and real estate usage, thus reducing the cost of boards.
- **Increased System Reliability**: Each component in a system can fail. The more discrete components that reside on a board, the higher the risk of a system failure. XCITE enhances system reliability by both bringing down component count and simplifying board construction.
- **Elimination of Stub Reflection**: When using discrete termination resistors, the distance between the package pin and resistor can cause reflections due to impedance mismatch. DCI improves discrete termination techniques by eliminating this distance entirely. Stub reflection is no longer a concern.

- **Immunity to Temperature and Voltage Changes**: The output impedance of traditional logic drivers varies considerably over the range of possible temperatures and voltages. These variations can lead to significant impedance mismatches even in carefully terminated systems. DCI adjusts for these variations to ensure that impedance remains matched over all temperatures and voltages.
- **Support for Multiple High-Speed Standards**: Virtex-II devices offer input and output DCI for the following IO standards: GTL, GTL+, HSTL I, HSTL II, HSTL III, HSTL IV, SSTL2, SSTL3, and LVCMOS.
- **Banking Versatility**: Each bank can be configured as a different XCITE or SelectI/O™ standard. Standards with compatible voltages and resistances can coexist in the same bank.

References

The following references provide additional details on DCI:

- Virtex-II Handbook; see the section on DCI (pp 273):

  http://www.xilinx.com/products/virtex/handbook/index.htm
- Virtex-II Data Sheet:

  http://www.xilinx.com/partinfo/databook.htm

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/31/01	1.0	Initial Xilinx release.