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HDLC Controller Solutions with Spartan-II FPGAs

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Using the Spartan™-II Family in combination with a Soft IP to effectively penetrate the HDLC Controller market in place of the traditional ASSP

Summary

The Spartan-II product family brings the density, extensive features, high performance and low cost which makes it the preferred HDLC Controller solution within different data networking applications. A Spartan-II FPGA based HDLC Controller solution with efficient partitioning of hardware and software functions provides the necessary scalability and flexibility to make it the first PLD to effectively penetrate the ASSP marketplace.

Introduction

In the past, programmable logic devices have had limited success in penetrating the ASSP market because PLDs have lacked the density, features, performance, and most importantly been a costly approach. Bringing programmability and its traditional benefits to a design solution is always an expensive proposition and PLDs have traditionally lost the battle to the cost-optimized custom solution or ASIC. The playing field however has been leveled due to the use of cutting edge process technologies. This approach has allowed PLDs to significantly reduce die sizes, and therefore lower the cost of the overall solution. This rapid transition in process technology has allowed PLD vendors to service the needs of today's ASSP designers.

Spartan-II FPGAs offer more than 100,000 system gates at under \$10 and are the most cost-effective PLD solution ever offered. They build on the capabilities of the very successful Virtex family and support all the associated features, including SelectIO™, BlockRAM™, Distributed RAM, DLLs, and clock speeds up to 200 MHz. The Spartan-II family is extremely well positioned to offer a low-cost programmable ASSP alternative and expand the time-to-market advantage that PLDs traditionally offer. It also increases the value of the ASSP by allowing end users to customize their solutions.

The Spartan-II family, combined with a vast soft IP portfolio is the first programmable logic solution to effectively penetrate the ASSP marketplace. The HDLC Controller solutions from Memec Design Services (MDS) and CoreEL MicroSystems ported on a Spartan-II device is a good example highlighting the concept of a programmable ASSP. Both MDS and CoreEL MicroSystems are members of the Xilinx AllianceCORE™ program and have a wealth of IP cores in other applications.

MDS is the design and engineering division of the Memec global semiconductor distribution group of companies. The MDS mission is to offer clients a complete suite of Programmable Logic engineering services, ranging from design evaluations all the way through to complete turnkey device solutions. Using MDS will reduce the time it takes to get new products to market, improving productivity and profitability for original equipment manufacturers in ever-increasing competitive business arenas. MDS is also a major developer of Intellectual Property for Xilinx FPGAs. For more information, visit the MDS website at www.xilinx.com/products/logicore/alliance/memec/memec.htm.

The Single Channel XF-HDLC Controller core is developed, sold, and supported by MDS. It is targeted for frame relay, ISDN and X.25 protocols and logic consolidation applications. Several leading manufacturers are already using MDS's Xilinx-based HDLC Controller technology in production systems. The Single Channel XF-HDLC Controller core is available immediately for use in Spartan-II FPGAs and can be purchased directly from MDS.

Founded in 1992, CoreEL MicroSystems, Inc. is a Delaware corporation with headquarters in Fremont, CA and engineering operation in India under CG-CoreEL Logic Systems Ltd. Since 1995, CoreEL has focused its business in designing, developing and marketing networking and telecom system level megacells, called Corecells, for integration into ASIC or FPGA to create system-on-a-chip products. CoreEL also provides complete product design service based on its Corecells for its customers. More information is available at www.xilinx.com/products/logiccore/alliance/coreel/coreel.htm.

The PPP8 HDLC (CC318f) Controller core, developed, sold, and supported by CoreEL, implements Point-to-Point Protocol (PPP) encapsulation of packets and is used in bridges, routers and switches providing high bandwidth WAN links. The CC318f is fully compliant with the RFC1619 POS (PPP Over SONET) specification and is being used by several leading manufacturers in production systems. The CC318f core is available right away for use in Spartan-II FPGAs, and can be obtained directly from CoreEL.

What is HDLC?

High-level Data Link Control (HDLC) is a bit-oriented synchronous data link layer protocol developed by the International Standards Organization (ISO). This is based on IBM Corporation's Synchronous Data Link Control (SDLC) protocol and specifies a data encapsulation method on synchronous serial links using frame characters and checksums.

HDLC is in itself a group of several protocols or rules for transmitting data between network points (sometimes called nodes). The data is organized into a unit (called a frame) and sent across a network to a destination that verifies its successful arrival. The HDLC protocol also manages the flow or pace at which the data is sent. HDLC is one of the most commonly used protocols in what is layer 2 (Data Link Layer) of the industry communication reference model called Open Systems Interconnection (OSI). (Layer 1 is the detailed physical level (PHY) that involves actually generating and receiving the electronic signals. Layer 3 is the higher level that has knowledge about the network, including access to router tables that indicate where to forward or send data. On sending, programming in layer 3 creates a frame that usually contains source and destination network addresses. HDLC, which resides on layer 2, encapsulates the layer 3 frame, adding data link control information to a new and larger frame.)

In HDLC, the protocol that is essentially SDLC is known as Normal Response Mode (NRM). In NRM, a primary station (usually at the mainframe computer) sends data to secondary stations that may be local or may be at remote locations on dedicated leased lines in what is called a multi-drop or multi-point networks.

Some variations of HDLC are also used for the public networks that use the X.25 communications protocol and for frame relay, a protocol used in both local area networks and (public and private) wide area networks.

In the X.25 version of HDLC, the data frame contains a packet. (An X.25 network is one in which packets of data are moved to their destination along routes determined by network conditions as perceived by routers and reassembled in the right order at the ultimate destination.) The X.25 version of HDLC uses peer-to-peer communication with both ends able to initiate communication on duplex links. This mode of HDLC is known as Link Access Procedure Balanced (LAPB).

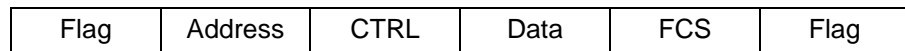
The **Table 1** summarizes the HDLC variations and who uses them.

Table 1: HDLC Variations

HDLC Subset	Uses
NRM (Normal Response Mode)	Multipoint networks that typically use SDLC
LAP (Link Access Procedure)	Early X.25 implementations
LAPB (LAP, Balanced)	Current X.25 implementations
LAPD (LAP for the ISDN D-channel)	ISDN D channel and frame relay
LAPM (LAP for Modems)	Error-correcting modems (specified as part of V.42)

HDLC specifies a packetization standard for serial links and supports several modes of operation, including a simple sliding window mode for reliable delivery. Since the Internet provides retransmission at higher levels (i.e., TCP), most Internet applications use HDLC's unreliable delivery mode, unnumbered information.

HDLC Protocol's frame structure:



The beginning and end of HDLC frames are marked by flag characters—01111110 binary. No flag character may appear in the intervening data. To enforce this requirement, the data may need to be modified (in a transparent manner). On bit-synchronous links, a binary 0 is inserted after every sequence of five "1s" (bit stuffing). Thus, the longest sequence of "1s" that may appear of the link is 0111110—one less than the flag character. The receiver, upon seeing five "1s", examines the next bit. If "0", the bit is discarded and the frame continues. If "1", then this must be the flag sequence at the end of the frame.

At the end of the frame, a Frame Check Sequence (FCS) is used to verify the data integrity. The FCS is a CRC calculated using the polynomial $x^{16} + x^{12} + x^5 + 1$. Between HDLC frames, the link remains idle. Most synchronous links constantly transmit data; these links can transmit all "1s" during the inter-frame period (mark idle), or all flag characters (flag idle).

Many variants of HDLC have been developed. Both PPP and SLIP use a subnet of HDLC's functionality. ISDN's D channel uses a slightly modified version of HDLC. Cisco routers' default serial link encapsulation is HDLC.

HDLC Protocol Controllers

HDLC Controllers are devices which execute the HDLC protocol. Some of the key operations include handling bit oriented protocol structure and formatting data as per the packet switching protocol defined in the X.25 recommendations of the CCITT. It includes transmitting and receiving the packeted data serially, while providing the data transparency through zero insertion and deletion. These controllers generate and detect flags that indicate the HDLC status. They provide 16-/32-bit CRC on data packets using the CCITT defined polynomial, and recognize the single byte address in the received frame.

HDLC Controller Applications

Being generic, but critical in the function they perform, HDLC Controllers are used in various data networking operations. Some of the key applications are:

- Frame relay switches – high density access, FRADs.
- ISDN – basic-rate or primary-rate interfaces, D-channel.
- X.25 and V.35 protocols.
- Internet/edge routers, bridges and switches – for high bandwidth WAN links.
- Cellular base station switch controller.
- Error-correction in modems.

- T1/E1, T3/E3 – channelized, clear channel (unchannelized).
- xDSL – each port can support up to 10Mbps.
- Dual HSSI.
- SONET termination.
- Digital sets, PBXs and private packet networks.
- C-channel controller to Digital Network Interface Circuits.
- Data link controllers and protocol generators.
- Inter-processor communication.
- Logic Consolidation.
- CSU/DSU.
- Protocol converter.
- Packet data switch.
- Distributed packet-based communications system.
- Multiplexer/Concentrators – remote access, multiservice access.

Xilinx IP Partners

The Spartan-II family inherits unique features, density, an extensive synthesizable IP portfolio and the cost structure to effectively compete against ASSPs. The programmable solution provided by the Spartan-II family requires a soft IP core. This is provided through the AllianceCORE™ program, which is a cooperative effort between Xilinx and independent third-party core developers. It is designed to produce a broad selection of industry-standard solutions dedicated for use in Xilinx's FPGAs. A programmable logic version of a core must have value over an ASIC/ASSP version of the same function. It must be cost effective and make sense for use in a programmable device in a production system. As a result, Xilinx does not promote generic, synthesizable cores as AllianceCORE products. Instead, they are generally provided as black boxes. This guarantees that the implementation is optimized for density while still meeting performance, preserving the time-to-market value of programmable logic. Allowing quick implementation of unique logic on the same device provides flexibility. Partners may provide cores customized to meet specific design needs. Source code versions of the cores are often available from the partners at additional cost for those who need ultimate flexibility.

With the availability of the Spartan-II family, the HDLC Protocol Controller solution can be implemented using a single Spartan-II device and the IP provided by MDS and CoreEL MicroSystems, who are AllianceCORE partners. It is worthy to note that the cores provided by the two core partners have separate features, which allows both solutions to serve separate markets.

Memec Design Services

The *Single Channel XF-HDLC Controller core* conforms to the ISO/IEC 3309 specification, and provides the entire functionality of the HDLC Controller. The core:

- provides 16-/32-bit CCITT-CRC generation and checking
- performs flag and zero insertion and detection
- allows Full Duplex Operation
- has a DC to 53 Mbps (STS-1) data rate
- has a full synchronous operation
- interface can be customized for user FIFO and DMA requirements.

The XF-HDLC core performs the most common functions of an HDLC controller. Data bytes are clocked into the device based on a divided version of the transmit clock. This data is then serialized and framed according to the rules of HDLC and sent out through the serial transmit data pin. Receive frames are clocked into the receive data pin synchronous to the receive clock. The framing overhead is then stripped off and the data bytes are converted from serial to parallel and passed on through the parallel receive bus.

Figure 1 explains MDS's HDLC Controller block diagram. MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, and then an additional global buffer would have to be used. In any instance, where one of the cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core.

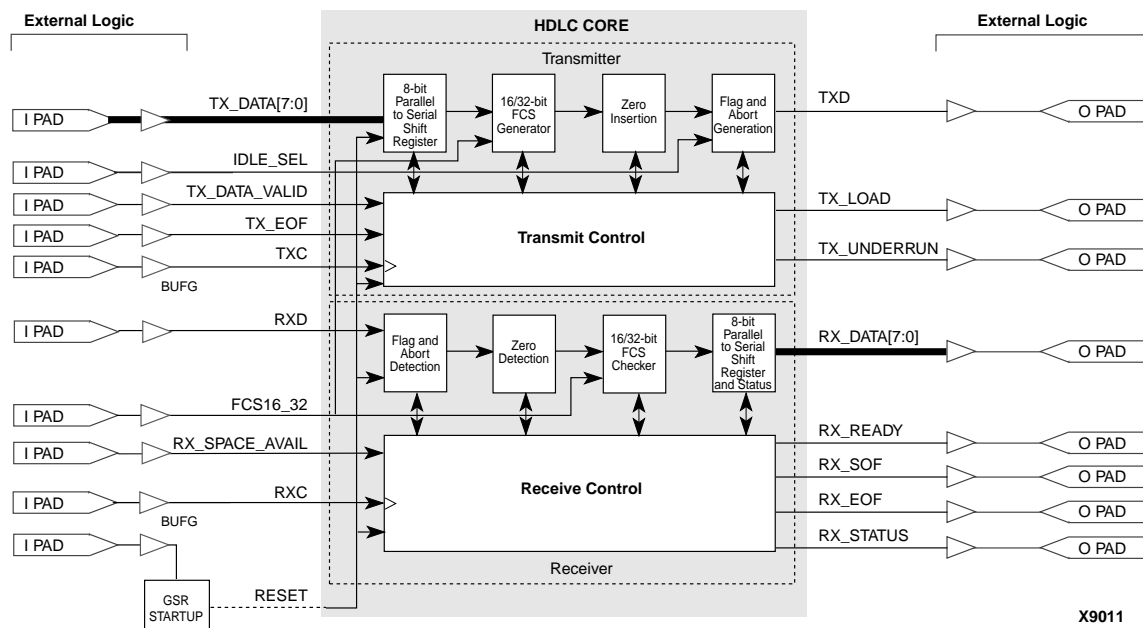


Figure 1: HDLC Controller Block Diagram (Courtesy: Memec Design Services)

This philosophy allows external logic to use that clock without using another global buffer. As a result of this philosophy, the cores are not self-contained. External logic must be connected to the core in order to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality.

CoreEL MicroSystems

The *PPP8 HDLC core (CC318f)* provided by CoreEL MicroSystems conforms to RFC1619 PPP over SONET specification. The core:

- supports programmable Address, Control and Protocol fields
- supports 8-bit Packet and PHY framer interface
- allows a 16-/32-bit FCS generation and verification and provides a MTU and compression enable and a scramble and de-scramble enable signal
- detects the address field, control field, escape sequence and FCS packet errors
- provides statistics for address field, control field, protocol field, FCS field and escape

- sequence packet errors
- provides statistics features like the number of packets, runt packets, valid packets and excess length packets (i.e. frame length greater than MTU)
- detects error conditions like Transmission Break on Transmit side
- discards packets received with Address, Control or Protocol field error
- optionally compresses Address, Control fields and Protocol field
- generates discard packet signal for the packet with FCS error or invalid packet on packet interface

Figure 2 and Figure 3, respectively, explain the transmitter and receiver block diagram of the CC318f HDLC Controller core from CoreEL MicroSystems.

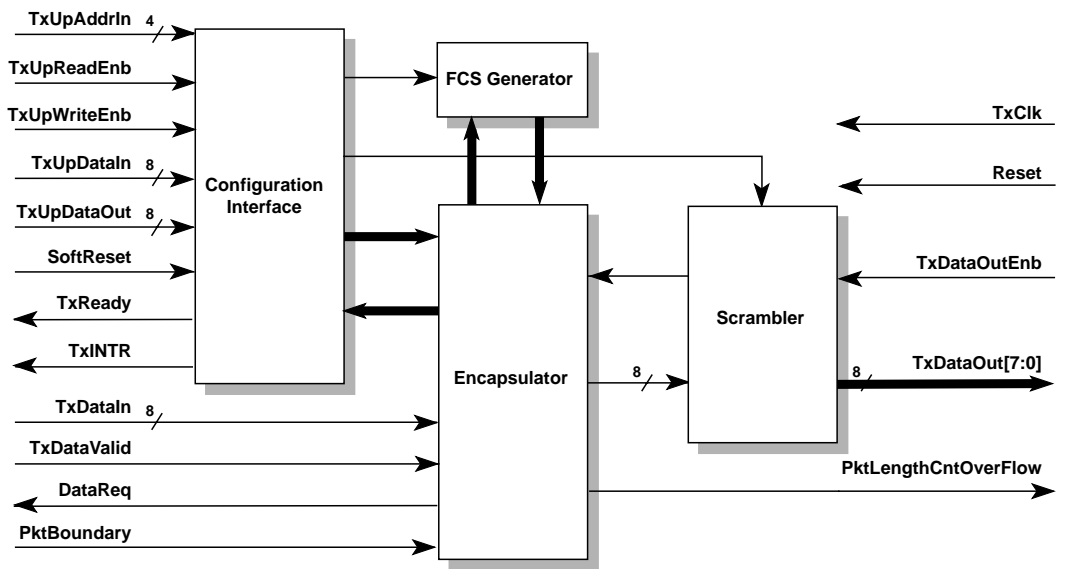


Figure 2: CC318f Transmitter Block Diagram (Courtesy: CoreEL Microsystems)

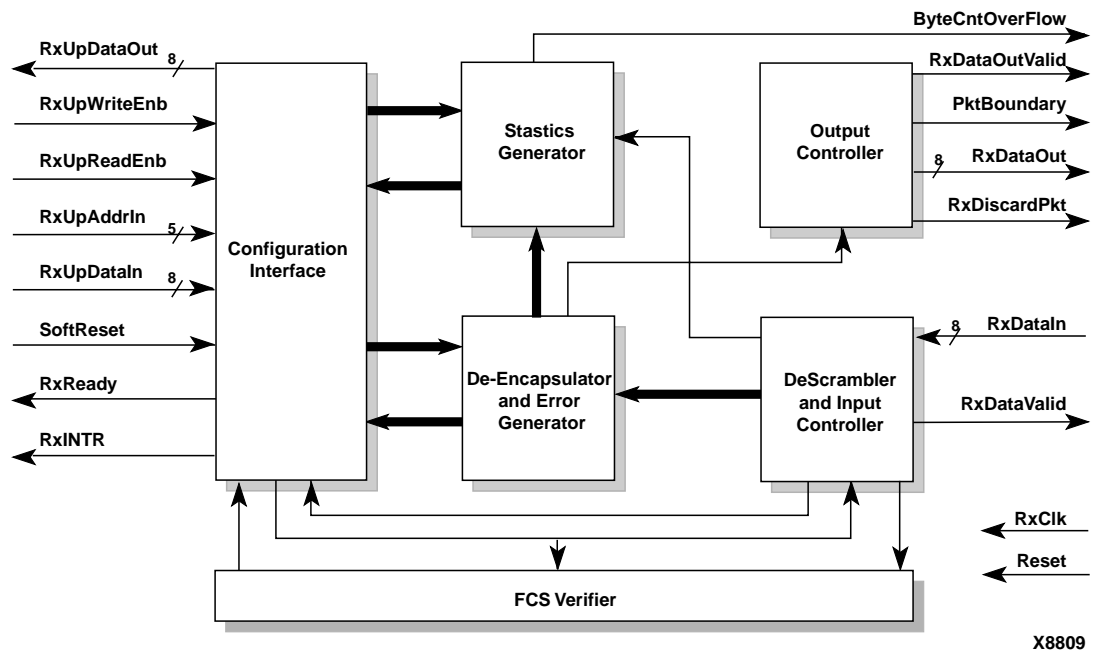


Figure 3: CC318f Receiver Block Diagram (Courtesy: CoreEL Microsystems)

The CC318f core implements PPP encapsulation of packets such as IP and IPX. The core is divided into separate transmitter and receiver modules. The transmit module receives IP Packets on an 8-bit inter-face and encapsulates them in PPP format. It provides a byte-wide interface to the PHY and packet interfaces. It supports programmable address, control and protocol fields with programmable compression enables for each field. It supports programmable 16-/32-bit FCS fields and transmits RFC1619-compliant frames on the PHY interface. It also detects error conditions like transmission break and abruptly terminates the packet without inserting the FCS field. The receive module extracts the PPP encapsulated packets, analyzes the respective fields, generates errors, and offers various statistics features. It provides a byte-wide interface to the PHY and packet interfaces. It supports programmable address, control and protocol fields with programmable compression enables for each field. It supports programmable 16-/32-bit FCS fields and receives frames on the PHY interface in compliance with RFC1619. It silently discards packets with address, control or protocol field errors. The receiver does not discard invalid packets or packets with FCS errors. Instead, it flags these on the RxDiscardPkt signal on the packet interface.

Figure 4 shows an application of the HDLC PPP core.

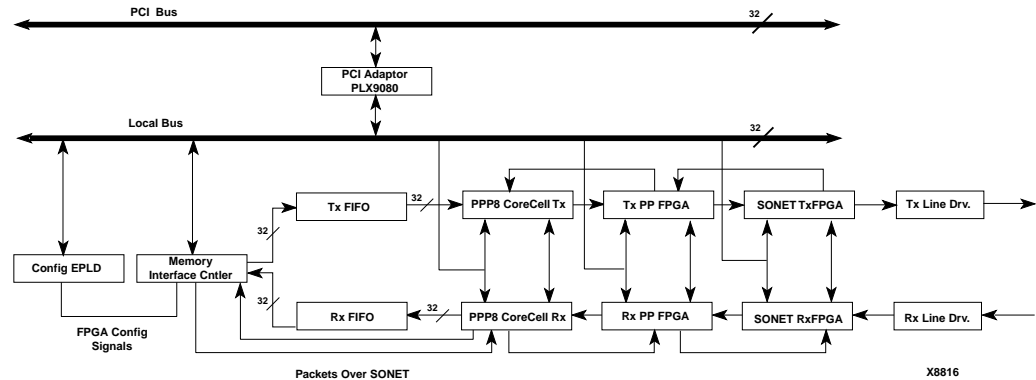


Figure 4: Application of HDLC PPP Cores (Courtesy: CoreEL MicroSystems)

Comparing the Spartan-II HDLC Controller Solution with Stand-alone ASSPs

The HDLC Controller solution from MDS and CoreEL MicroSystems ported on the Spartan-II devices demonstrates the **programmable ASSP** concept.

The dynamics in the ASIC/ASSP marketplace are opening up new opportunities for PLDs and is allowing them to compete against ASSPs. Due to its extensive features and cost effectiveness, the Spartan-II solution has all the unique ingredients that enable Xilinx to succeed against traditional ASSPs. The underlying programmable nature to the solution further bolsters the value of a Programmable ASSP. An end customer can choose to use the HDLC Controller solution as sold by Xilinx or choose to augment or change the solution to best suit their needs. This is a testimonial to the tremendous potential that PLD vendors have for addressing the ASSP marketplace.

A programmable ASSP like the Spartan-II family offers significant advantages over a stand-alone ASSP. Using the Spartan-II family in conjunction with appropriate IP cores allows the designer to choose the right feature set and optimize the programmable ASSP, to achieve the best possible results. Designers can also integrate their value proposition within the same piece of silicon, to allow product customization and reduce costs. For example, an HDLC Controller solution supplied by a stand-alone ASSP vendor may include a 32-bit, 33 MHz PCI Controller. The designer on the other hand may require a 32-bit, 66 MHz or a 64-bit, 33 MHz PCI Controller. The ASSP vendor charges a much higher price in comparison to the Spartan-II solution, without providing the intended service. With the Spartan-II solution, the same device can be programmed through a soft IP to be an HDLC Controller, and be reprogrammed as either a 32-bit, 66MHz or a 64-bit, 33MHz PCI Controller. This allows the designer to mix and match the appropriate HDLC Controller to the PCI Controller based on the needs of the system. This flexibility comes at a significantly lower cost when compared to the fixed ASSP solution, due to the inherent low cost of the Spartan-II family. Shown in Figure 5 is the value proposition of a Spartan-II solution against a stand-alone ASSP.

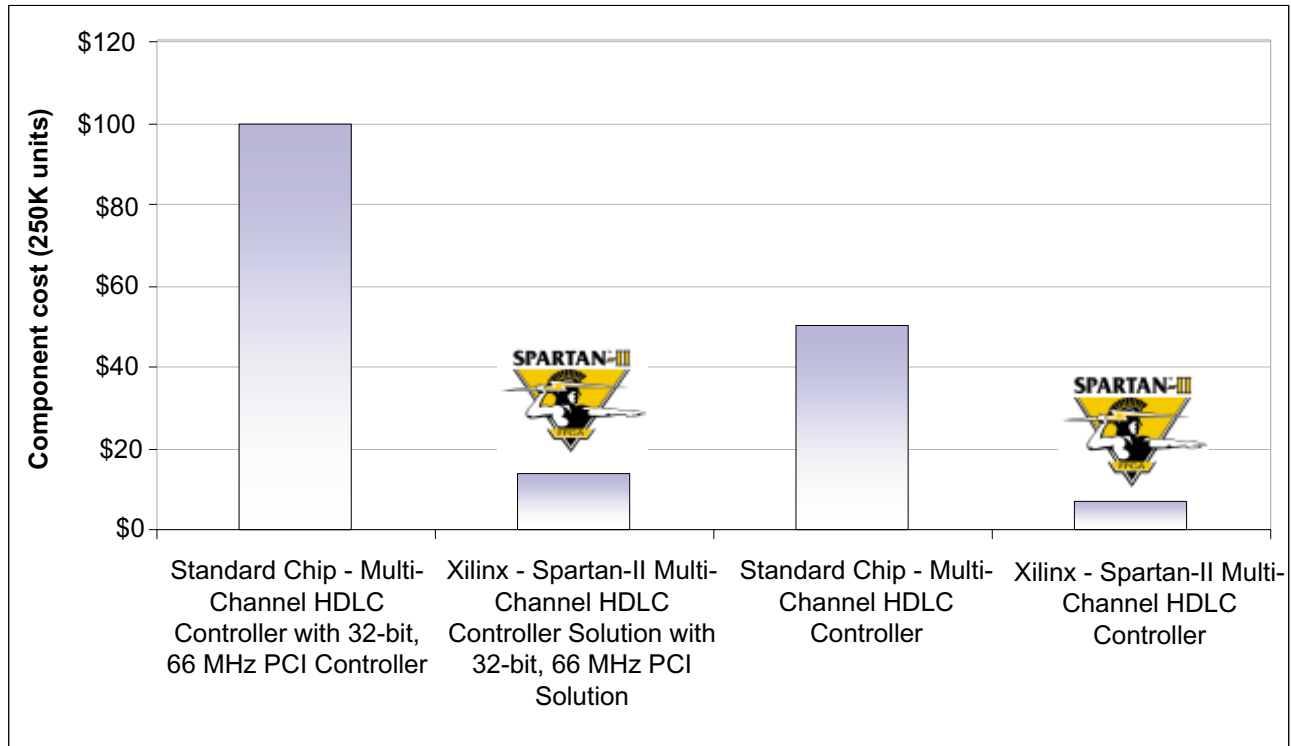


Figure 5: Value Proposition - Xilinx PCI Solution, Xilinx HDLC Controller Solution vs. Stand-alone ASSPs

The Spartan-II family accommodates specification changes and can easily be used in volume production. Conflicting specifications and lack of a clear direction create the need for programmable ASSP solutions. For example, the ASSPs providing HDLC Controller solutions are based on X.25 (CCITT) level-2 or OSI Layer-2, ISO3309 specification only. The solutions provided through the Spartan-II family and IP vendors caters to X.25 (CCITT) level-2, OSI layer-2, ISO3309, RFC1619 PPP over SONET and ITU recommendation (Q.921) specification standards. It would be nearly impossible and cost-prohibitive for an ASSP vendor to cater to all the various specifications. But, at the same time betting on the success of one single product may preclude them from being successful in the marketplace. These conditions create many opportunities for the Spartan-II family – the industry’s first programmable ASSP. Because of the high profit margins involved with these products, designers can easily continue using programmable ASSPs in volume production.

Most stand-alone ASSPs never behave as expected, due to reasons ranging from bugs in the silicon, system integration issues, software drivers, or even user error. Irrespective of the cause, verifying and identifying device problems can be very difficult with ASSPs, but a lot easier with programmable ASSPs. Having been built on the fabric of a proven FPGA technology and having silicon that is pre-verified and guaranteed to perform, potential problems in the Spartan-II family are narrowed down to a software-only issue. Xilinx provides powerful tools that improve the transparency of the final solution. With the help of HDL simulators, test benches, and run-time debugging tools like ChipScope designers can easily identify the problem. Because a programmable ASSP is inherently re-programmable, fixing the problem is also simple. This is a tremendous value-add feature that a stand-alone ASSP cannot offer. It is much simpler to integrate a HDLC Controller that is re-programmable, than an ASSP which performs its specific task.

Through the Xilinx On-line (a.k.a., IRL: Internet Reconfiguration Logic) program, a programmable ASSP, such as the Spartan-II family, allows a designer to gain market share by bringing them to market sooner than a stand-alone ASSP. Spartan-II FPGAs are based on SRAM technology and are customized by loading configuration data into internal memory cells

and therefore it is very easy to re-program them an unlimited number of times. Updating the functionality of the FPGA only requires that the designer include a mechanism for updating the configuration bitstream. Remotely updating software with any new enhancements and bug fixes, increases the life of the HDLC controller within any networking equipment. Designing systems that do remote upgrades can also provide new revenue opportunities. After the initial product is released, new hardware features can be developed, sold and distributed inexpensively to existing customers in much the same way as new versions of software can be distributed today. In addition, a standard "off-the-shelf" application can be developed so that features can be swapped in and out depending on what the end-user purchases or needs. The designer can hence take advantage of the fact that the solution now allows them to upgrade their hardware and stay in the market-place longer, thus maximizing profitability.

Significant features like value proposition against ASSPs, accommodation of specification changes, improved testing and verification and field upgradability as discussed above show the advantage presented by Spartan-II devices. The cost difference between a stand-alone ASSP and an equivalent Spartan-II solution is also considerable. Hence the Spartan-II family is a clear winner in not only the HDLC Controller market, but in other ASSP niche areas also.

The Spartan-II family is unaffected by the hurdles that an ASSP vendor needs to overcome and offers a cost-effective programmable ASSP solution; its inherent advantages extend the reach of the Spartan family to new levels and creates new opportunities for PLDs in the ASSP market.

Conclusions

HDLC Controllers are deployed within a number of different data networking applications. Soft IP for HDLC Controllers has been available for Xilinx FPGAs in older products like the XC4000XL family, and more recently for the very successful Virtex family. Being built on the capabilities of the Virtex family and due to its features and cost effectiveness, the Spartan-II devices extend the Spartan family's focus in competing against ASICs and ASSPs. Hence it is uniquely poised to penetrate the ASSP marketplace. An FPGA-based HDLC Controller solution with efficient partitioning of hardware and software functions provides the necessary scalability and flexibility to handle all these applications and allows for tracking of new standards.

References

*"The Spartan-II Family – The Complete Package", Krishna Rangasayee
Memec Design Services
CoreEL MicroSystems, Inc.*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/01/00	1.0	Initial Xilinx release.