In-System Programming Times for XC9500XL

XAPP141 April 29, 1999 (Version 1.0) Application Note

Summary

This application note discusses the in-system programming speed of the XC9500XL devices.

Xilinx Family

XC9500XL

Introduction

XC9500XL devices receive programming vectors and instructions via the JTAG Test Access Port. During programming, the address and data information is shifted in first and then a programming time is initiated to imprint the programming data into the selected flash cells. This is repeated for all flash memory addresses within the device.

Therefore, the time required to program an XC9500XL device includes two components: the information download time and the flash memory programming time. In the typical application, where the JTAG clock operates from 1MHz to 10 MHz, the flash memory programming time exceeds 90% of the total programming time.

Device Programming Times

Programming time varies greatly, depending on the programming environment. Table 1 summarizes the PC programming time for one, two and four devices.

Programming in a Production Environment

In a production environment, fast programming times translate to reduced costs, and most Automatic Test Equipment (ATE) used for board testing is capable of efficiently downloading information to the XC9500XL devices at the maximum speed of 10MHz. In order to minimize the production programming costs, XC9500XL devices are fully erased and ready for programming when shipped from the factory.

Programming in a Development Environment

The device programming times in a typical development environment are often longer than those for the production environment. First, there is overhead time spent in the real-time generation of programming vectors from the JEDEC bitmap. Then there are bandwidth limitations for outputting JTAG vectors using a general purpose computer. Lastly, there is the time required to erase the device.

The development environment programming times vary depending on whether the download cable is parallel (fastest) or serial, and depending on the configuration and type of base computer system.

Concurrent Programming

Multiple devices in a JTAG chain can be programmed concurrently by downloading all devices with the programming information and then concurrently programming all devices in the chain. Therefore, because the download time is small, the total time required to program all devices in a chain is only a little longer than the time required to program the largest device in the chain.

Conclusion

Whether programming in the development or the production environment, the XC9500XL CPLD family with ISP programming delivers consistant, fast programming times. This increases productivity while reducing valuable ATE test times.

Table 1: Programming Time (in seconds) using a 200 MHz Pentium Pro PC, Xilinx JTAG Programmer Software and a Xilinx Parallel Cable.

# Devices (concurrent mode)	XC9536XL	XC9572XL	XC95144XL
1	3	4	4.5
2	4	4.5	6
4	6	7	9