An Alternative Capacity Metric for LUT-Based FPGAs

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Summary

As an alternative to "gate counting", the capacity of look-up-table-based FPGAs can be measured more directly and objectively by examining the number of available "logic cells".

Introduction

Ideally, FPGA capacity metrics should provide an accurate indication of the amount of logic that can be implemented within a given FPGA device, and, at the same time, reflect the relative capacity of devices from competing manufacturers. Unfortunately, this ideal situation seldom occurs.

Most vendors, including Xilinx, describe device capacities in terms of "gate counts"; that is, the number of 2-input NAND gates that would be required to implement the same functionality. This metric has the advantage of being familiar to ASIC designers, and, in theory, allows the comparison of programmable logic device capacities to those of traditional, mask-programmed gate arrays.

However, FPGA devices do not consist of arrays of 2-input NAND gates; they have structures such as look-up tables, multiplexers, three-state buffers and flip-flops for implementing logic functions. Thus, "counting gates" is far from an exact science, and different vendors apply varying methodologies to determine their gate counts. All too often, gate counting becomes a game of "one-upmanship" among competing vendors. As a result, comparing gate count statistics supplied by different FPGA vendors can be misleading. (The methodology used by Xilinx to generate gate count metrics for Xilinx FPGAs is described in Application Note #059, "Gate Count Capacity Metrics for FPGAs".)

The majority of FPGAs in use today are SRAM-based FPGAs whose logic blocks are based on a combination of memory look-up tables (LUTs) and dedicated registers. FPGA families with LUT-based logic blocks include the Xilinx XC3000, XC4000 and XC5000 series, the Altera FLEX families, and the Lucent Technologies ORCA families. Although differing architecturally in many other respects, this commonality (that is, the use of LUTs and registers as the primary logic resource) can be exploited to develop a more direct and objective capacity metric than gate counts.

Logic Cells

As shown in Table 1, each FPGA vendor has its own name and acronym for the logic blocks that make up the array, and each FPGA family has its own organization for the resources in the block.

For purposes of establishing a common metric, a "logic cell" is defined as the combination of a 4-input look-up table and a dedicated register that reside in the same block, such that the output of the LUT can be the data input to the register.

Table 1: FPGA families and their logic array resources

Vendor	FPGA Family	Array Element	LUTs	Registers	Logic Cells per Array Element
Xilinx	XC3000	Configurable Logic Block (CLB)	(1) 5-input	2	1.625
Xilinx	XC4000	Configurable Logic Block (CLB)	(2) 4-input (1) 3-input	2	2.375
Xilinx	XC5000	Configurable Logic Block (CLB)	(4) 4-input	4	4
Altera	FLEX 8K	Logic Array Block (LAB)	(8) 4-input	8	8
Altera	FLEX 10K	Logic Array Block (LAB)	(8) 4-input	8	8
Lucent	ORCA 2C	Programmable Function Unit (PFU)	(4) 4-input	4	4

Table 2: XC4000 Series FPGA Capacity Metrics

Device	Number of CLBs	Number of Logic Cells
XC4003E	100	237.5
XC4005E/XL	196	465.5
XC4006E	256	608
XC4008E	324	769.5
XC4010E/XL	400	950
XC4013E/XL	576	1368
XC4020E/XL	784	1862
XC4025E	1024	2432
XC4028EX/XL	1024	2432
XC4036EX/XL	1296	3078
XC4044XL	1600	3800
XC4052XL	1936	4598
XC4062XL	2304	5472
XC4085XL	3136	7448
XC40125XV	4624	10,982

Table 3: XC5000 Series FPGA Capacity Metrics

Device	Number of CLBs	Number of Logic Cells
XC5202	64	256
XC5204	120	480
XC5206	196	784
XC5210	324	1296
XC5215	484	1936

Table 4: FLEX 8000 series FPGA Capacity Metrics

Device	Number of LABs	Number of Logic Cells
EPF8282	26	208
EPF8452	42	336
EPF8636	63	504
EPF8820	84	672
EPF81188	126	1008
EPF81500	162	1296

Table 5: FLEX 10K Series FPGA Capacity Metrics

Device	Number of LABs	Number of Logic Cells
EPF10K10	72	576
EPF10K20	144	1152
EPF10K30	216	1728
EPF10K40	288	2304
EPF10K50	360	2880
EPF10K70	468	3744
EPF10K100	624	4992

Table 6: ORCA 2C Series FPGA Capacity Metrics

Device	Number of PFUs	Number of Logic Cells
2C04	100	400
2C06	144	576
2C08	196	784
2C10	256	1024
2C12	324	1296
2C15	400	1600
2C26	576	2304
2C40	900	3600

Using this definition, the XC5000 and ORCA 2C FPGAs have 4 logic cells per array element, and the Altera FLEX FPGAs have 8 logic cells per array element.

The XC4000 CLB contains two 4-input look-up table, one 3-input look-up table and two registers. Each 4-input LUT and each register are considered 1/2 of a logic cell, and a 3-input LUT has 3/4 the functionality of a 4-input LUT. Thus, each 3-input LUT can be considered as 3/8 of a logic cell. (This assumption is consistent with results obtained from system-level benchmarks.) Thus, each XC4000 CLB holds 2.375 logic cells.

The XC3000 CLB includes a single 5-input look-up table and two registers. A 5-input LUT, with 5/4 the functionality of a 4-input LUT, constitutes 5/4 x 1/2 = 5/8 of a logic cell. Thus, including the two registers, each XC3000 CLB holds 1.625 logic cells.

Table 7 lists the members of the XC4000, XC5000, FLEX 8000, FLEX 10K, and ORCA 2C families, sorted in ascending order by the number of logic cells in each device. These results illustrate the inconsistencies of the various manufacturers' claimed "gate counts". For example, the "40,000-gate" EPF10K40 device has the same number of logic cells as the "26,000-gate" 2C26 device, and both of these have fewer logic cells than the "25,000-gate" XC4025E FPGA.

Table 7: XC4000, XC5000, FLEX 8000, FLEX 10K, and ORCA 2C family FPGAs sorted by number of logic cells

Xilinx	Logic Cells	Altera	Logic Cells	Lucent	Logic Cells
		EPF8282	208		
XC4003E	237.5				
XC5202	256				
		EPF8452	336		
				2C04	400
XC4005E/XL	465.5				
XC5204	480				
		EPF8636	504		
		EPF10K10	576	2C06	576
XC4006E	608				
		EPF8820	672		
XC4008E	769.5				
XC5206	784			2C08	784
XC4010E/XL	950				
		EPF81188	1008		
				2C10	1024
		EPF10K20	1152		
XC5210	1296	EPF81500	1296	2C12	1296
XC4013E/XL	1368				
				2C15	1600
		EPF10K30	1728		
XC4020E/XL	1862				
XC5215	1936				
		EPF10K40	2304	2C26	2304
XC4025E	2432				
XC4028EX/XL	2432				
		EPF10K50	2880		
XC4036EX/XL	3078				
				2C40	3600
		EPF10K70	3744		
XC4044XL	3800				
XC4052XL	4598				
		EPF10K100	4992		
XC4062XL	5472				
XC4085XL	7448				
XC40125XV	10,982				

Logic Cell Structure and FPGA Capacity

There are many other factors that affect the achievable logic capacity of an FPGA device, and counting the number of available logic cells should be considered a first-order estimate of device capacity. For example, while the FPGA architectures included in Table 7 all have LUTs and registers in their logic blocks, the architectures vary in the way in which these resources are interconnected and in the type of additional resources that are included in the block. Some of the distinguishing factors include the following:

- Independent versus shared LUT inputs (if multiple LUTs are included in the block); in general, independent inputs provide greater flexibility leading to higher overall utilization.
- The inclusion of dedicated multiplexers and routing channels supporting the cascading of LUTs in order to

efficiently implement wide combinatorial functions.

- The inclusion of dedicated arithmetic carry logic and routing channels supporting the efficient implementation of arithmetic functions.
- The coupling between the LUTs and flip-flops (that is, are they always paired, or can they be used independently?).
- The availability and types of register controls, including clock inversion, clock enable, set, and reset controls.
- The number and flexibility of connections between the block's inputs and outputs and the neighboring programmable interconnect resources.

Furthermore, the architecture of the interconnect resources and its effect on overall device "routability" is another key factor not taken into account by this "logic cell count" capacity metric. In other words, an FPGA should not only contain a multiplicity of logic cell resources, it also must have sufficient routing resources to allow them to be used effectively. In general, all other things being equal, the FPGA architecture with the most routing resources will have the highest utilization levels.

Additional Resources

Both gate count and logic cell count capacity metrics suffer from another drawback - they only take logic block resources into account. Modern FPGAs include a host of other important features.

For example, the XC4000, ORCA 2C, and FLEX 10K architectures allow the integration of memory as well as logic resources within the FPGA device, and the XC5000 and FLEX 8000 architecture do not (Table 8). Furthermore, the XC4000 and ORCA 2C architectures use a "distributed memory" scheme, wherein LUTs may be used as blocks of memory instead of logic resources, while the FLEX 10K architecture employs dedicated memory blocks embedded within the logic array.

Other architectural resources can considerably boost the capacity and system integration capabilities of FPGA devices. For example, architectural features in the XC4000 Series that are not reflected in logic cell count capacity metrics include wide edge decoders, registers and logic in the I/O blocks, global buffers and clock distribution networks, and internal three-state buffers.

Footprint Compatibility Lessens Risk

Designers do not always "guess right" when initially selecting the FPGA family member most suitable for their design. Thus, "footprint compatibility" is an important feature for maximizing the flexibility of FPGA designs. Footprint compatibility refers to the availability of FPGAs of various gate densities with the same packages and with an identical pinout. When a range of footprint-compatible devices is available, users have the ability to migrate a given design to a higher or lower density device without changing the printed circuit board (PCB), thereby lowering the risk associated with initial device selection. If the selected device turns out to be too small, the design is migrated to a larger device. If the selected device is too big, the design can be moved to a smaller device. In either case, with footprint-compatible devices, potentially expensive and time consuming changes to the PCB are avoided. Footprint compatibility has been incorporated in all Xilinx component product lines.

Summary

As a first-order approximation of the relative device capacity of FPGAs with LUT-based logic cells, counting logic cells provides a considerably more direct and accurate comparison than relying on manufacturers' claimed gate counts.

However, there are considerable architectural distinctions between FPGA families. While this capacity metric can help "narrow the field" during FPGA device selection, users are encouraged to examine and compare all the internal resources of the various devices being considered for a design.

Of course, many additional factors beyond capacity determine the effectiveness of a given FPGA in a given application, including performance, price, packaging, availability, power consumption, reliability, and ease-of-use.

Table 8: XC4000, FLEX 10K, and ORCA 2C family FPGAs sorted by maximum number of memory bits

Xilinx	Max. Memory Bits	Altera	Max. Memory Bits	Lucent	Max. Memory Bits
XC4003E	3,200				
		EPF10K10	6,144		
XC4005E/XL	6,272				
				2C04	6,400
XC4006E	8,192				
				2C06	9,216
XC4008E	10,368				
				2C08	12,544
		EPF10K20	12,288		
		EPF10K30	12,288		
XC4010E/XL	12,800				
		EPF10K40	16,384	2C10	16,384
XC4013E/XL	18,432	EPF10K70	18,432		
		EPF10K50	20,480		
				2C12	20,736
		EPF10K100	24,576		
XC4020E/XL	25,008				
				2C15	25,600
XC4025E	32,768				
XC4028EX/XL	32,768				
				2C26	36,864
XC4036EX/XL	41,472				
XC4044XL	51,200				
				2C40	57,600
XC4052XL	61,952				
XC4062XL	73,728				
XC4085XL	100,352				
XC40125XV	147,968				