A Simple Method of Estimating Power in XC4000XL/EX/E FPGAs

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Summary

A simple method is presented for estimating power dissipation in XC4000X Series FPGAs. This method is targeted for early estimates during design conceptualization before detailed design information is available. A second application note, “Estimating Power Consumption in XC4000XL/EX/E devices”, will describe how to make more accurate estimates of power dissipation when more information is known about the design.

Xilinx Family

XC4000XL, EX and E devices

Introduces

Simple Method to Estimate Power Dissipation

Introduction

As the size of the largest programmable logic devices continues to grow, low power operation becomes increasingly important. Low power CMOS architectures provide designers with the following design options and benefits:

- Lower Temperature Operation
- Lower Cost Packages
- Higher Speed Operation
- Higher Levels of Utilization
- Higher Levels of Integration
- Lower Cost Power Supplies
- Ability to Meet Power Budgets
- Higher Device Reliability
- Fewer Noise Related Problems

Power scales as V^2 and as such, lower voltage devices provide lower power dissipation. This factor along with Xilinx’ segmented routing architecture are the reasons the XC4000XL FPGAs have very low power dissipation.

Accuracy of Power Estimation

The design process can typically be broken into 3 phases:

- Concept
- Detailed design
- Working board and design

During the concept phase of design, a rough estimate of power is usually sufficient. This is based on rough estimates of logic capacity and frequency of operation.

During the detailed design phase, you have more accurate logic capacity and frequency estimates available as well as detailed information about how the design is implemented in the FPGA. A second application note describes how to estimate power during this phase. After a board and the design have been completed, power may be measured during operation, providing an accurate measure of power dissipation.

This application brief is focused on estimating power during the initial or concept phase of design.

CMOS Power Consumption Factors

For CMOS integrated circuits, total power consumption (P_T) is the sum of three components:

$$P_T = P_{static} + P_{INT} + P_{IO} \quad \text{..... (1)}$$

P_{static} power dissipated by an inactive device connected to the supply rails. This results from leakage currents.

P_{INT} power consumed due to internal nodes switching (capacitance on each node is being charged and then discharged).

P_{IO} power dissipated due to charging and discharging of external load capacitors connected to device pins, and pull-ups used on inputs.

In cases where the frequency of operation is very low, static IC power, (not including use of pull-ups etc.), may become a significant factor. This can be determined directly from the datasheet by multiplying the quiescent current (I_{CCO}) by the power supply voltage (e.g. for XC4036XL, 4 mA * 3.3V = 13.2 mW).

Where the frequency of operation is high, total power is dominated by the sum of internal dynamic power and I/O power. Note that for the analysis given in this application brief, power dissipation due to pull-ups and pull-downs has been ignored.

Internal Power Dissipation (P_{INT})

As mentioned above, internal power dissipation results from charging and discharging the capacitance on any internal nodes that are switched. Different designs have different power consumption, depending on the capacitance of each net and how frequently it switches. The formula below was derived based on data taken from FPGAs filled

with 16-bit counters, all clocked in parallel. It provides an approximation for the concept phase of design.

Internal power can be approximated as:

$P_{INT} = V_{CC} * Kp * F_{MAX} * N_{LC} * Tog_{LC}$ .....(2)

Where:

V_{CC} = supply voltage (3.3V for XC4000XL)

Kp = constant depends on family; shown in Table 1

F_{MAX} = maximum clock frequency (Hz) in your design

N_{LC} = # of logic cells used in your design

Tog_{LC} = average % of logic cells toggling at each clock (typically 20% in most designs, 12.5% in 16-bit counters, 25% in 8-bit counters)

Table 1: Kp Power Factor

Device	Kp Power Factor ($x10^{-12}$)
XC4000XL	28
XC4000EX	47
XC4000E	72

Output Power Dissipation (POUT)

P_{OUT} depends on the capacitive load on each output as well as the frequency at which each output switches. This is shown with:

$$P_{OUT} = \sum_{n=1}^{N} (C_n \bullet V_n^2 \bullet F_n)$$

Where:

N = number of outputs

C_n = capacitance of the n'th output (F)

V_n = voltage swing on the n'th output (this equals V_{CC} for the XC4000XL, but is lower for the TTL mode, available on EX and E parts)

F_n = frequency at which the n'th I/O switches (Hz):

For XC4000XL devices Vn = Vcc so that:

$$P_{OUT} = \sum_{n=1}^{N} (C_n \bullet F_n \bullet V_{CC}^2)$$

To eliminate the summation, take the average load capacitance and note that $F_n = 1/2 * F_{MAX}$ (in this case we are considering clocked outputs which can only change or toggle once per clock cycle), giving

$P_{OUT} = 1/2 * C_{OUTavg} * F_{MAX} * Tog_{OUT} * N_{OUT} * V^2_{swing}$....(3)

Where:

Tog_{OUT} = % I/Os toggling at each clock

N_{OUT} = number of outputs in design

V_{swing} = the voltage swing on the output pin.

For XC4000XL Vswing is Vcc, for XC4000EX and XC4000E parts this can be either rail to rail for CMOS or less for TTL levels.

Example

The following example illustrates the use of the above formulas.

The design consists of some large counters (>32 bits), state machines, and random logic, and drives two 32 bit buses each loaded with 30 pF. It is expected that the I/Os will toggle every 4th clock on average. The main clock operates at 45 MHz. The capacity is estimated at 2000 logic cells and the target device is an XC4028XL.

First calculate the internal power. With large counters, state machines and random logic, estimate 15% of the nodes will change each clock cycle (tog_{LC} = 0.15). Using equation (2)

P_{INT} = 3.3 *28e-12 * 45e6 * 2000 * 0.15

= 1.25W

For the output power, note that outputs are switching state every 4th clock, giving Tog_{OUT} = 25%. From equation (3)

P_{OUT} = 1/2 * 30e-12 * 45e6 * 0.25 * 64* 3.3 * 3.3

= 0.12W

Using equation (1)

P_T = 1.25 + 0.12

= 1.37W

Summary

Use the following formulas to provide a rough estimate of power dissipation during the concept phase of design.

$P_T = P_{static} + P_{INT} + P_{OUT}$

$P_{INT} = V_{CC} * Kp * F_{MAX} * N_{LC} * Tog_{LC}$

$P_{OUT} = 1/2 * C_{OUTavg} * F_{MAX} * Tog_{OUT} * N_{OUT} * V^2_{swing}$

Use the more detailed equations described in the application note, "Estimating Power Consumption in XC4000XL/EX/E devices", when moving to the detailed design phase and more accuracy is required.

Appendix

Other useful information is presented below on a variety of topics related to power dissipation.

Deriving Output Power Dissipation

It is helpful to have a conceptual understanding of the output power before deriving the formula to describe it.

Assume that a capacitor of value C is fully discharged and connected to an I/O pin. At some point in time the output starts pulling high. Charge is transferred through the I/O to the capacitor. The amount of this charge equals the capac-

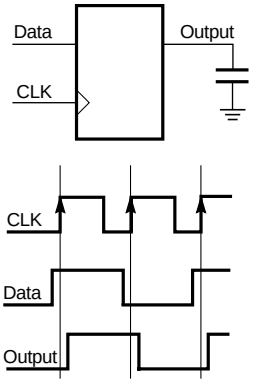

Figure 1: Clocked Output

itance multiplied by the final voltage on the capacitor. The earliest opportunity for this capacitor on the I/O to be discharged is during the next clock cycle. During this second clock cycle, the charge leaves the capacitor and transfers to ground.

In this way, it takes two clock cycles for the charge Q to be transferred through the FPGA to ground. It is important to realize that the power dissipated is all in the FPGA and not in the capacitor. Mathematically

Q = CV

I = Q/t

For outputs driven by a flip flop where the output toggles on each clock cycle:

I = CV/(2 * T) = 1/2 * CVF

Where:

Q = change in charge (coulombs)

C = capacitance (Farads)

V = voltage swing (Volts)

I = current (Amperes)

T = clock period (seconds)

t = time (seconds)

F = clock frequency (MHz)

Detailed Design Phase

At this stage sufficient information should be known to begin using power data at the device level of detail. For example:

Active flip-flops

Multiple clocks

Active Clock/Global Low Skew Buffers

RAM

Refer to the application note, “Estimating Power Consumption in XC4000XL/EX/E devices”, for more on detailed power calculations.

Working Board and Design

This is the first point at which power consumption may actually be measured. If the PCB’s design permits isolation of the target device’s power planes, then direct current measurements may be taken during operation. The alternative in situations where the design is not readily isolated on the PCB is to take temperature measurements of the case and the ambient, and then from the thermal characteristics of the package, the power dissipation may be calculated by solving these equations:

$$Pd = \Theta J_A(T_J\text{-}T_A)$$

$$Pd = \Theta J_C(T_J\text{-}T_C)$$

Where: Pd is the total device power dissipation in watts. T_j is the junction or die temperature, in °C. T_A is the ambient temperature expressed in °C, and lastly T_c is the temperature of the package body, or case.

During such measurements, care should be taken to operate the device with the expected worst case switching rates, both internally and externally.

Minimizing Operating Temperatures

Given a situation where a design is running hotter than allowed for a given target device, the following are potential solutions:

1. Migrate the design to a device which uses a lower supply voltage, typically utilizing an advanced process such as 0.25um or 0.35um.
2. Use packages which can better dissipate heat. These include thermally enhanced HQ and HT packages as well as ceramic packages.
3. Place thermal planes around and under the device on the PCB.
4. Use heat-sinks which allow increased dissipation of heat by increasing the effective surface area available for heat exchange.
5. Use mechanical air-flow guides for systems which already have some form of forced airflow.
6. Use IC mounted fans as a very last resort for designs with serious power problems. These are currently being used for some Intel products.
7. Slow the design down. Can the design operate using lower clock rates? Are there portions of the design which can be clocked at lower rates?

References

The reader is referred for more device related information to the following Xilinx publications: Application Note "Estimating Power Consumption in XC4000XV/XL/EX/E devices", the Programmable Logic Data-book section 10 'Packages and Thermal Characteristics', XCell: (XCell #22, Q3 1996) 'Power, Package & Performance'.

Design Support and Feedback

This application brief may undergo future revisions and additions. If you would like to be updated with new versions of this application note, or if you have questions, comments, or suggestions please send an email to:

hotline@xilinx.com

or a FAX addressed to "Power Consumption Application Note Developers" sent to 1+(408) 879-4442.

IMPORTANT: Please be sure to include which version of the application note you are using.

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