Questions & Answers

From the Xilinx Applications Engineering Staff

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Virtex I/Os

How do I pull the I/O pins to 5 Volts using external pullups?

To pull up the I/O pins to 5V externally, only three I/O standards are allowed: LVTTL, LVCMOS, and PCI33_5.

The internal I/O pullup can be considered to be a 50K resistor to Vcco (for 3.3-V or 2.5-V devices). If you try to pull an I/O to a voltage higher than Vcco, you need to do so with a resistor, with a smaller value than 50K. The devices have circuitry to disable the internal pullup if the I/O is pulled higher than about Vcco + 0.7V (a threshold voltage higher than Vcco), so if you pull an I/O up to 5V, there will be no static current into Vcco. But if you don't pull up the I/O past Vcco + 0.7V, then the internal pullup remains enabled and will "fight" with the external pullup.

Our recommendation is to use a 4.7K pullup resistor, but any value less than 4.7K will also work.

Software Installation

What do I do if my Alliance Series or Foundation Series 2.1i installation does not complete as a result of one of the following issues:

- The splash screen appears, then disappears without an error message.
- An unexpected error occurs during setup.

There may be several reasons for either of the error messages to appear. In general, ensure that you have administrative privileges and that there is plenty of hard drive space on the destination drive. Additionally, a re-boot is sometimes needed to release any locked Windows DLLs.

If you have done the above, and the installation still fails, the most likely problem has to do with the way the registry settings for certain environment variables are interacting with the 2.1i installer. Typically, simply resetting these variables will over-write the registry entry that is causing this problem, and allow the installer to succeed.

The variables that have been seen to exhibit the problem are: PATH, TEMP, and TMP.

- **Win9x**: Make sure these variables are listed in your autoexec.bat file.
- **WinNT**: You can check your environment by executing:
  'Start -> Settings -> Control Panel -> System -> Environment Tab'

In the System Variable section, there should be a PATH variable listed. In the User Variable section, there should be both TEMP and TMP variables. Re-updating each of these variables will correct the setting in the registry.

If there is no PATH variable listed in the User section, then create one. To do this:

1. Click on the Variable line and type in PATH.
2. Click on the value, and type in %PATH%.

By doing the above, the registry entries should get corrected, allowing the installation to succeed. For further information please reference:

- http://support.xilinx.com/techdocs/7074.htm
- http://support.xilinx.com/techdocs/7362.htm

CORE Generator

Are there any cores to speed up the implementation of Virtex designs?

The following cores are either included in the Xilinx 2.1i software release, or can be downloaded from the Xilinx CORE Generator Cores and IP Updates page: (http://www.xilinx.com/ipcenter/coregen/updates.htm#updatesCurrent)

The following cores are included in the 2.1i Release CD:

- Dynamic Constant Coefficient Multiplier.
- Divider.
- Block Memory modules (single and dual port).

The following cores can be downloaded from the Xilinx CORE Generator Cores and IP Updates page:

- Gate functions (AND, NAND, OR, NOR, XOR, XNOR, INVERTER).
- Multiplexer functions (bit, bus, slice BUFE/BUFT).
- Register functions (flip-flop and latch based).
- Parallel Multiplier (pipelined and combinatorial).
- Sine/Cosine Lookup TAble.
- Distributed Memories (single and dual port RAM and ROM).
- Adder/Subtractor.
- Accumulator.
- Comparator.
- Binary Counter.
- Decoder.
- FD-Based Shift Register.
- RAM-based Shift Register.
- Two's Complement.
- Numerically Controlled Oscillator (Single and Dual Channel)
- Distributed Arithmetic FIR Filter.
- Asynchronous FIFO.
- FFT and Inverse FFT (16-, 64-, 256-, and 1024-point).

Note: All Xilinx CORE Generator LogiCORE modules that support the Virtex architecture also support Virtex-E and Spartan-II architectures.

Synthesis

How can I instantiate a CLKDLL using Exemplar Spectrum or Synplicity?

Currently, CLKDLL has to be instantiated or manually inserted in Exemplar and Synplicity.

- A sample design and procedure for CLKDLL insertion in Exemplar Spectrum is documented in the following solution: http://www.xilinx.com/techdocs/7737.htm
- A sample design for CLKDLL instantiation in Synplicity is documented in the following solution: http://www.xilinx.com/techdocs/8144.htm

How can I infer a BlockRAM in Exemplar or Synplicity?

Both Exemplar Spectrum and Synplicity now support Virtex BlockRAM (a fully synchronized RAM) inference.

- Xilinx Solution 7929 (http://www.xilinx.com/techdocs/7929.htm) provides VHDL/Verilog example for Exemplar Spectrum.
- Xilinx Solution 2508 (http://www.xilinx.com/techdocs/2508.htm) provides VHDL/Verilog example for Synplicity.

Note: The BlockRAM inference example provided in XCELL 32 for Leonardo Spectrum was incorrect.

How can I infer a ROM in Synplicity?

One of the new features in Synplify 5.3 is ROM inference. Earlier versions of the Synplify compilers were able to infer ROM tables. Synplify 5.3 now maps these inferred ROMs to Xilinx ROM primitives (ROM16X1 and ROM32X1) with the use of an attribute called syn_romstyle.

Xilinx Solution 8183 shows how to infer these ROMs for the 4K and Virtex families in VHDL/Verilog: http://www.xilinx.com/techdocs/8183.htm.

Simulation

How do I use glbl.v module in the Verilog simulation?

In the 2.1i Alliance Series, the general procedure for specifying global signals for the Verilog simulation flow involves defining the global signals with the **$XILINX/verilog/src/glbl.v** module. This module allows a global signal to be modeled as a wire in a global module.

The glbl.v module connects the global signals to the design, which is why it is necessary to compile this module with the other design files and load it along with the toplevel.v file or the testbench.v file for simulation.

Configuration & JTAG/ Boundary Scan

What are the supported Xilinx cable, software, and device combinations?

The following combinations are supported, as described in http://support.xilinx.com/techdocs/8097.htm:

1. MultiLINX cable with Hardware Debugger v2.1i (or later):

- Supports slave serial configuration of XC3000A, Spartan/XL, XC4000E/EX/XL/XLA/XV, and Virtex/E devices.
- SelectMAP configuration on Virtex/E devices.
- Readback verify supported for XC4000E/EX/XL/XLA/XV, XC9500/XL/XV, Spartan/XL, and Virtex/E devices.

2. MultiLINX with JTAG Programmer v2.1i sp3 (or later):

- Supports JTAG configuration of XC1804, XC4000E/EX/XL/XLA/XV, XC9500/XL/XV, Spartan/XL, and Virtex/E devices.
- Supports Readback-Verify of the XC9500/XL/XV devices.

3. Parallel Cable III with Hardware Debugger v2.1i (or later):

- Supports slave serial configuration of XC3000A, XC4000E/EX/XL/XLA/XV, Spartan/XL, and Virtex/E devices.

4. Parallel Cable III with JTAG Programmer v2.1i sp3 (or later):

- Supports JTAG configuration of XC1804, XC4000E/EX/XL/XLA/XV, XC9500/XL/XV, Spartan/XL, Virtex/E devices.
- Supports Readback-Verify of the XC9500/XL/XV devices.

5. XChecker with Hardware Debugger v2.1i (or later):

- Supports slave serial configuration of XC3000A, XC4000E/EX/XL/XLA/XV, Spartan/XL, and Virtex/E devices.
- Supports Readback-Verify and Readback-Capture of XC4000E/EX/XL/XLA/XV, and Spartan/XL devices with a configuration bit stream of 250,000 bits or less.

6. XChecker with JTAG Programmer v2.1i sp3 (or later):

- Supports JTAG configuration of XC1804, XC4000E/EX/XL/XLA/XV, XC9500/XL/XV, Spartan/XL, Virtex/E devices.
- Supports Readback-Verify of the XC9500/XL/XV devices.

Q: Where can I find information on performing JTAG configuration on a Virtex device?

See Application Note 139 (Xapp139) Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan at: http://www.xilinx.com/xapp/xapp139.pdf.

Q: What cable should be used with the Coolrunner ISP programmer?

The Xilinx Parallel III Cable should be used. Please reference: http://support.xilinx.com/techdocs/7588.htm.

Q: Which CoolRunner devices support ISP or Boundary Scan Operations?

The Coolrunner ISP and Boundary Scan support is listed in the following reference: http://support.xilinx.com/techdocs/8173.htm

support.xilinx.com

Q: What recent improvements have been made to the support.xilinx.com search engine?

A number of improvements have been made to our Web search engine:

- The first improvement was to update the underlying search algorithm. Previously we were AND-ing search terms together, which returned very precise results but often made it difficult for users to find what they were looking for. We decided to implement a more Internet friendly algorithm by using an 'ACCRUE' operation. This allows user queries to be scored, returning documents matching the highest number of keywords at the top of the list. Documents containing only one or two keywords would be returned at the bottom.
- The second improvement was to collect our older answer records into a separate archive. When new Xilinx users search our database, they no longer have to worry about sorting through older answer records to find the most current information. However, you will still have access to this older information.
- Finally, we've included the ability to search our software manuals from the same interface. It is now possible to search the Answers Database and online software documentation at the same time. Σ