Designing with FPGA Platforms

The Chief Technology Officer at Synopsys discusses the need for platform-based design in the era of system-on-a-chip FPGAs.

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As FPGAs move into million-gate densities, a world of new possibilities and potential applications is opening up for programmable logic devices. And along with these new opportunities comes many new challenges. The pairing of a low-cost, high performance PowerPC processor (and other hard cores), along with the soft cores and programmable logic circuitry in Xilinx Virtex-II™ FPGAs means that you will now be confronting challenges similar to what ASIC designers encountered when they made the transition to system-on-a-chip (SoC) ASICs.

Everyone who participates in the multimillion-gate segment of the FPGA market is wrestling with the same issues: increased complexity, escalating development costs, evolving standards, too few design engineers, increasingly compressed design cycles, and so on. In addition, as complexity increases, the time it takes you to get a product to market becomes dominated more by your design time than by manufacturing considerations, compromising one of the key advantages of FPGAs.

To help address these challenges, there is increasing pressure for designs to share a common architecture or platform, especially those that are targeted to similar applications. A platform is a basic system architecture that is geared towards a specific application, such as cell phone base stations or set-top boxes, among others; it is customized through software and by adding customized logic and IP.

An FPGA platform enables you to differentiate your products by adding customized logic and IP using the tightly integrated FPGA fabric. Platforms are important in the era of multimillion-gate FPGAs because they enable you to focus on adding value through custom IP rather than wasting time and resources by recreating standard components.

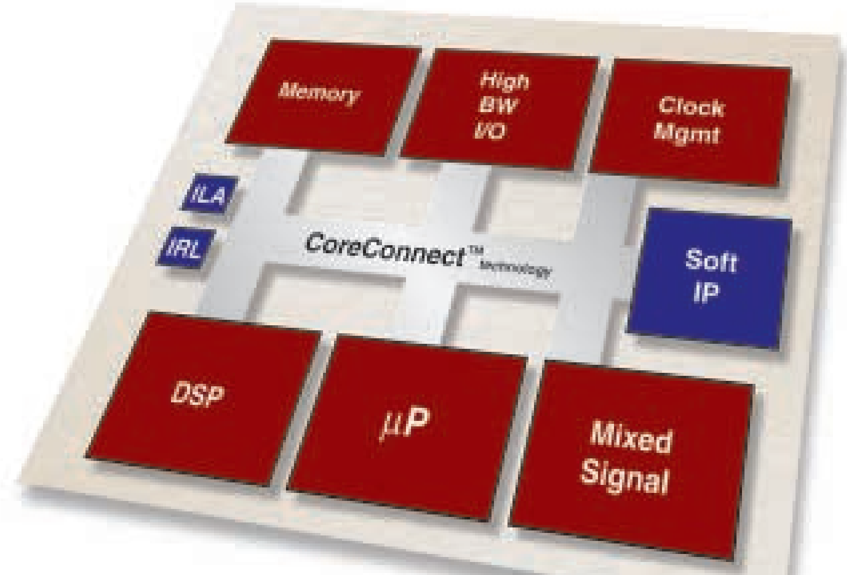

Figure 1 - Platform FPGA:
Xilinx Virtex-II FPGA with embedded PowerPC processor

Platform-Based Design

A central piece of any platform is the embedded processor, such as the IBM PowerPC processor core in the Xilinx Virtex-II platform. A typical platform might also include a bus, DSP, input/output channels, mixed signal functions, memory, and some configurable logic such as shown in Figure 1. FPGA design thus becomes platform design; rather than simply designing with gates, you must now focus on designing entire systems.

For you to effectively exploit a platform by designing at the system level, four primary design considerations must be addressed:

- Hardware design.
- Software design.
- Integration of hardware, software, and IP.
- Verification of the complete system (on a chip).

Synopsys delivers solutions in all four of these areas. The design of hardware has been our traditional domain, and we offer a suite of FPGA synthesis tools for this purpose. FPGA Express™ addresses the push-button, fast turn-around market, while FPGA Compiler II™ addresses more complex designs and compatibility with the ASIC design flow. Looking further into the future, other synthesis technologies such as Synopsys' Physical Synthesis will enable full timing closure for platform FPGAs.

Open SystemC

One of the most difficult aspects of software design involves how to interface software effectively with hardware. Open SystemC, a set of C++ class libraries that enables electronic design at the system level, provides an important tool for designing software and hardware in a common language framework. Based on C and C++ (the languages of choice for most algorithm developers, system architects, and software developers) SystemC also includes all the language elements necessary to effectively address hardware design. In this way, trade-offs between hardware and software can be addressed dynamically, even including reconfiguration in the field.

SystemC helps you create both systems and chips; the suite of tools and methodologies Synopsys has developed around SystemC significantly accelerate the design of elec-

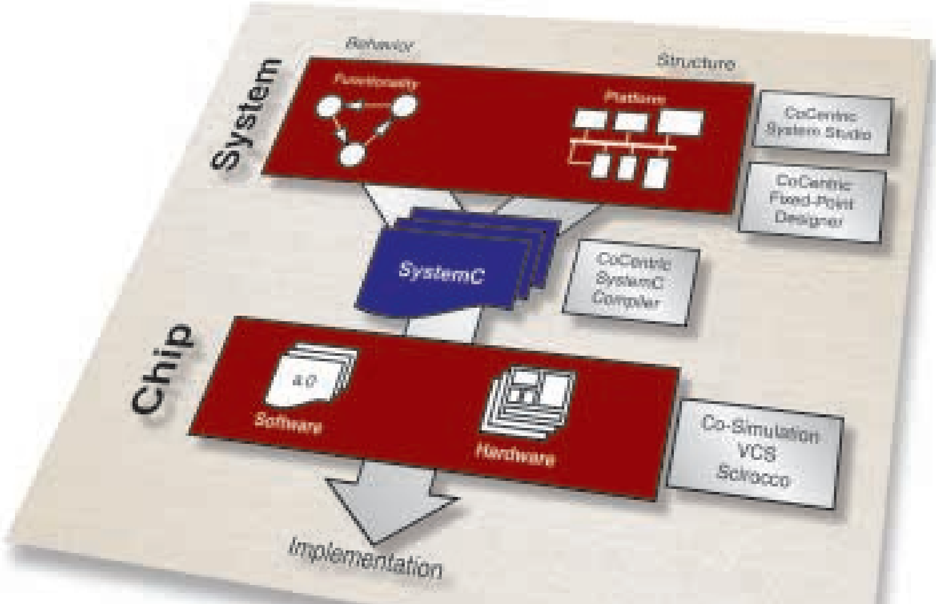

Figure 2 - SystemC tools

tronic systems from concept to implementation (see Figure 2). SystemC follows the community source-licensing model and can be downloaded from the Open SystemC Initiative's website at www.SystemC.org/.

IP Integration

One of the advantages of platform-based design is that it supports the integration of other pieces of proprietary logic and third-party IP. In fact, it is the customized portion of any system-on-a-chip ASIC or platform FPGA that provides the competitive differentiation from one device to the next.

But with the very large number of gates that can now be implemented on a single FPGA, the challenge is to become significantly more productive when creating with these gates. One obvious solution is to leverage existing gates through design reuse. Synopsys has been leading the way in this area and, with its DesignWare® libraries of reusable building blocks and methodology activities, offers several time-saving options for both ASIC and FPGA designers to leverage IP from a variety of sources.

System Verification

The challenge for any system-on-a-chip FPGA is to verify the complete system, including the processor core, and not just the individual blocks that comprise the system. This requires not only a high-speed simulator, but also a complete array of advanced verification tools. In particular, testbench generation, coverage tools, formal verification, a simulation model of the processor and other IP, and static timing analysis tools are essential for platform-based design (see Figure 3).

Static timing analysis illustrates the verification challenges imposed by such a system. Synopsys' PrimeTime® static timing analysis tool can time and analyze a complete chip, offering the multimillion-gate capacity that is required by systems on a chip. It also offers analysis modes that handle the processor core in an effective way.

Conclusion

FPGAs that contain embedded processor cores and application-specific components are creating a need for platform-based design, which requires not only the suite of RTL logic design tools that are already in use today (with the right capacity), but also a comprehensive suite of system-level design tools that will be new to most FPGA designers.

FPGA design has moved beyond the era of simple logic. With the advent of FPGAs that contain an embedded processor core, such as the PowerPC, FPGA designers will soon join their peers in the ASIC world by confronting the challenges of designing entire systems. Synopsys is helping you meet these challenges through the power of its system-level EDA tools optimized for platform-based design.

For more information on all Synopsys products, see www.synopsys.com

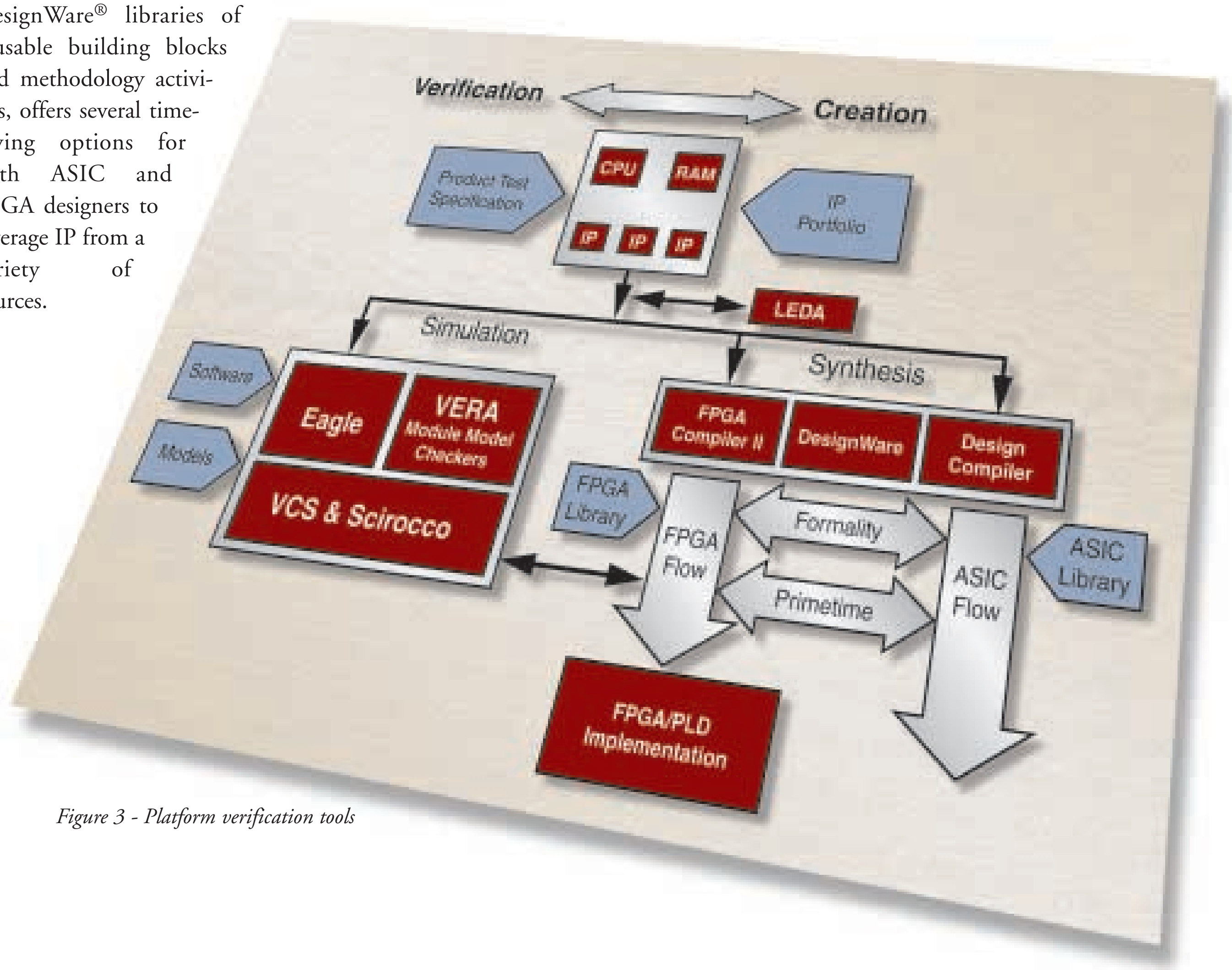

Figure 3 - Platform verification tools