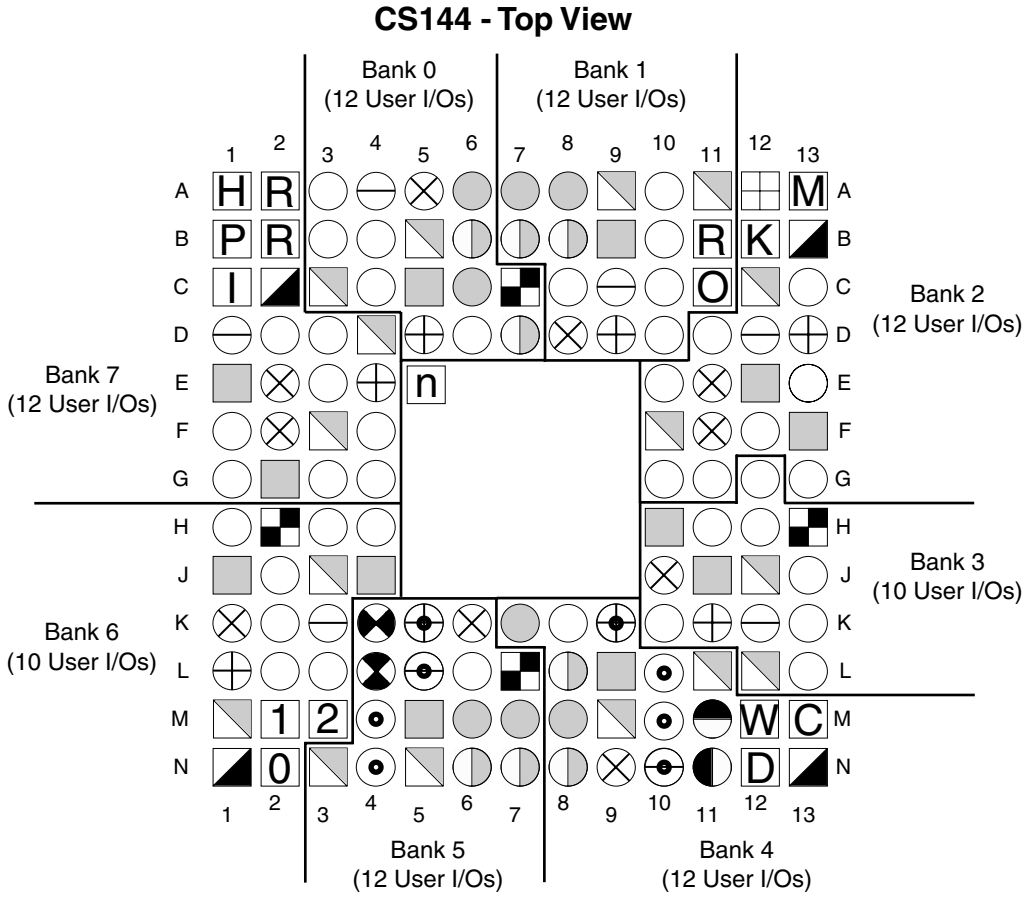
# Pinout Diagrams

This section contains pinout diagrams for the following Virtex-II packages:

# CS144 Chip-Scale BGA Composite Pinout Diagram




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | C CCLK | ⊞ VBATT |
| Dual-Purpose Pins: | P PROG_B | R RSVD |
| ⊙ DIN/D0-D7 | D DONE | ▨ VCCO |
| ⊠ CS_B | 2 1 0 M2, M1, M0 | ◪ VCCAUX |
| ⊠ RDWR_B | H HSWAP_EN | ▪ VCCINT |
| ◓ BUSY/DOUT | K TCK | ▩ GND |
| ◐ INIT_B | I TDI | n NO CONNECT |
| ● GCLKx (P) | O TDO | |
| ◑ GCLKx (S) | M TMS | |
| ⊖ VRP | W PWRDWN_B | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

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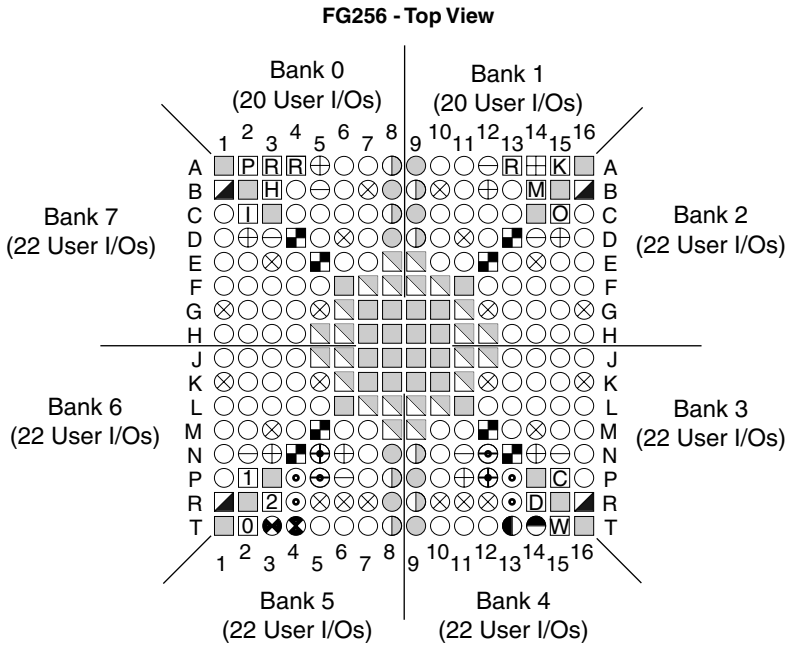
*Figure 4-1:* **CS144 Chip-Scale BGA Composite Pinout Diagram**

# FG256 Fine-Pitch BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | | |
| Dual-Purpose Pins: | | P | PROG_B | | |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊠ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⧖ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◪ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▪ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊙ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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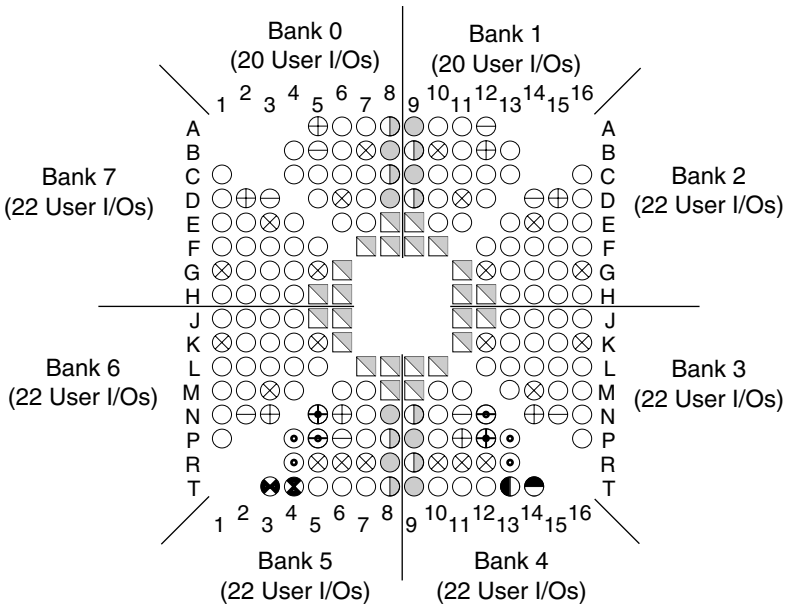
*Figure 4-2:* **FG256 Fine-Pitch BGA Composite Pinout Diagram**

# FG256 Bank Information

**FG256 - Top View**




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| ⊙ DIN/D0-D7 | | |
| ⊗ CS_B | | |
| ⊗ RDWR_B | | ▨ VCCO |
| ◓ BUSY/DOUT | | |
| ◐ INIT_B | | |
| ● GCLKx (P) | | |
| ◑ GCLKx (S) | | |
| ⊖ VRP | | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

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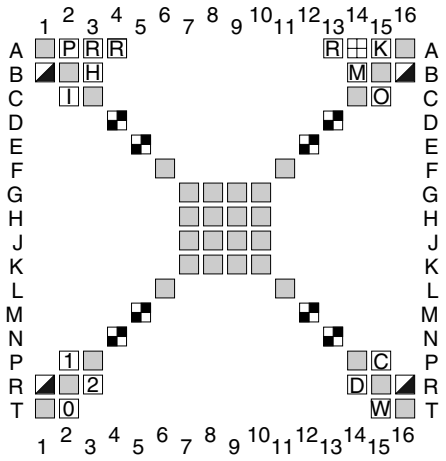
*Figure 4-3:* **FG256 Bank Information**

# FG256 Dedicated Pins

**FG256 - Top View**




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | |
| | P PROG_B | |
| | D DONE | ⊞ VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | ◪ VCCAUX |
| | I TDI | ◪ VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

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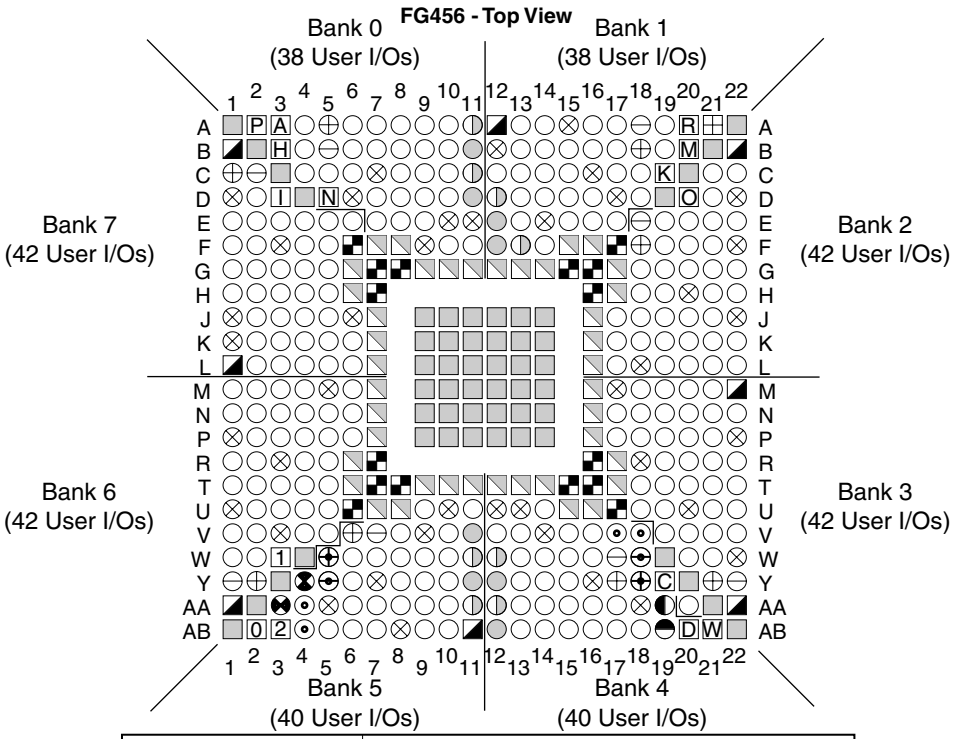
*Figure 4-4:* **FG256 Dedicated Pins**

# FG456 Fine-Pitch BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊗ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊗ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◢ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▚ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊖ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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*Figure 4-5:* **FG456 Fine-Pitch BGA Composite Pinout Diagram**

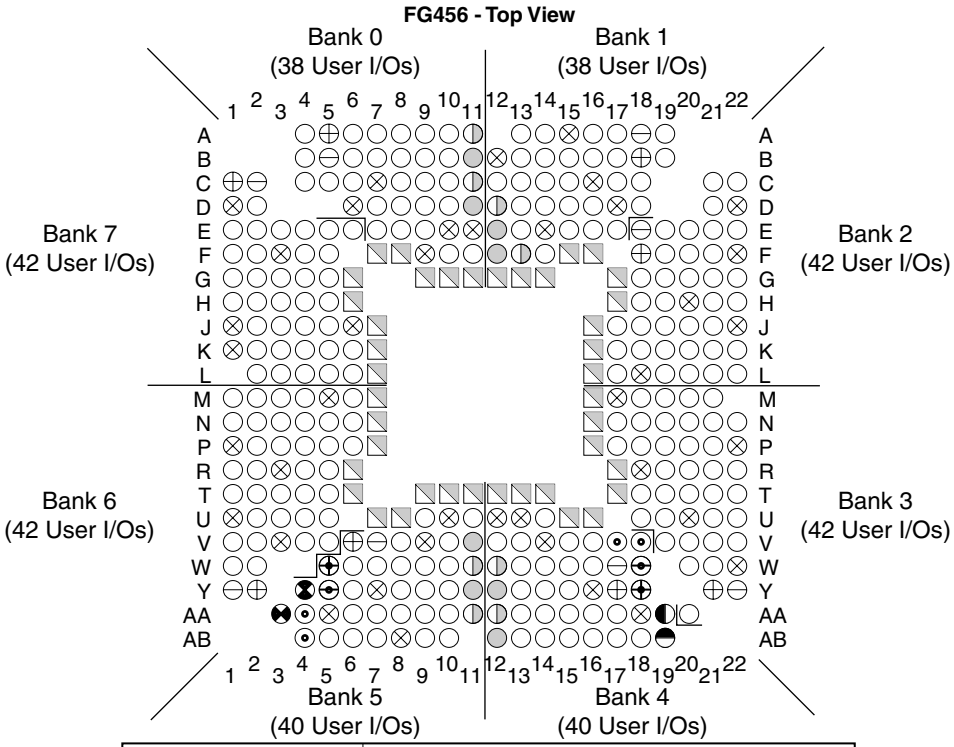
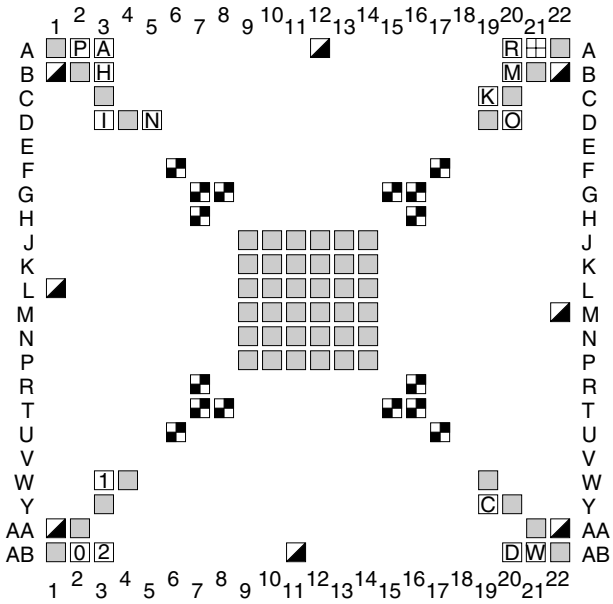



*Figure 4-6:* **FG456 Bank Information**

**FG456 - Top View**




| User I/O Pins | Dedicated Pins | | | |
|---|---|---|---|---|
| | C | CCLK | N | DXN |
| | P | PROG_B | A | DXP |
| | D | DONE | | VBATT |
| | 2 1 0 | M2, M1, M0 | R | RSVD |
| | H | HSWAP_EN | | |
| | K | TCK | | VCCAUX |
| | I | TDI | | VCCINT |
| | O | TDO | | GND |
| | M | TMS | n | NO CONNECT |
| | W | PWRDWN_B | | |

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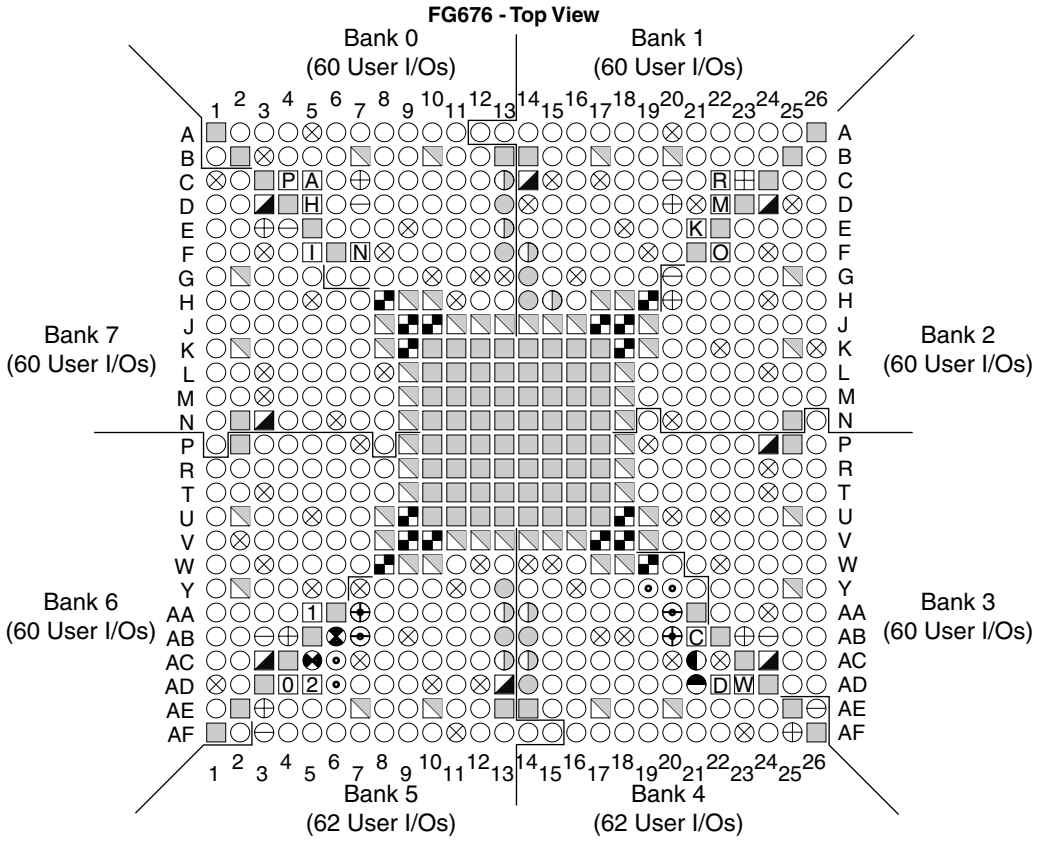
*Figure 4-7:* **FG456 Dedicated Pins**

# FG676 Fine-Pitch BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊗ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊗ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◪ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▩ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊛ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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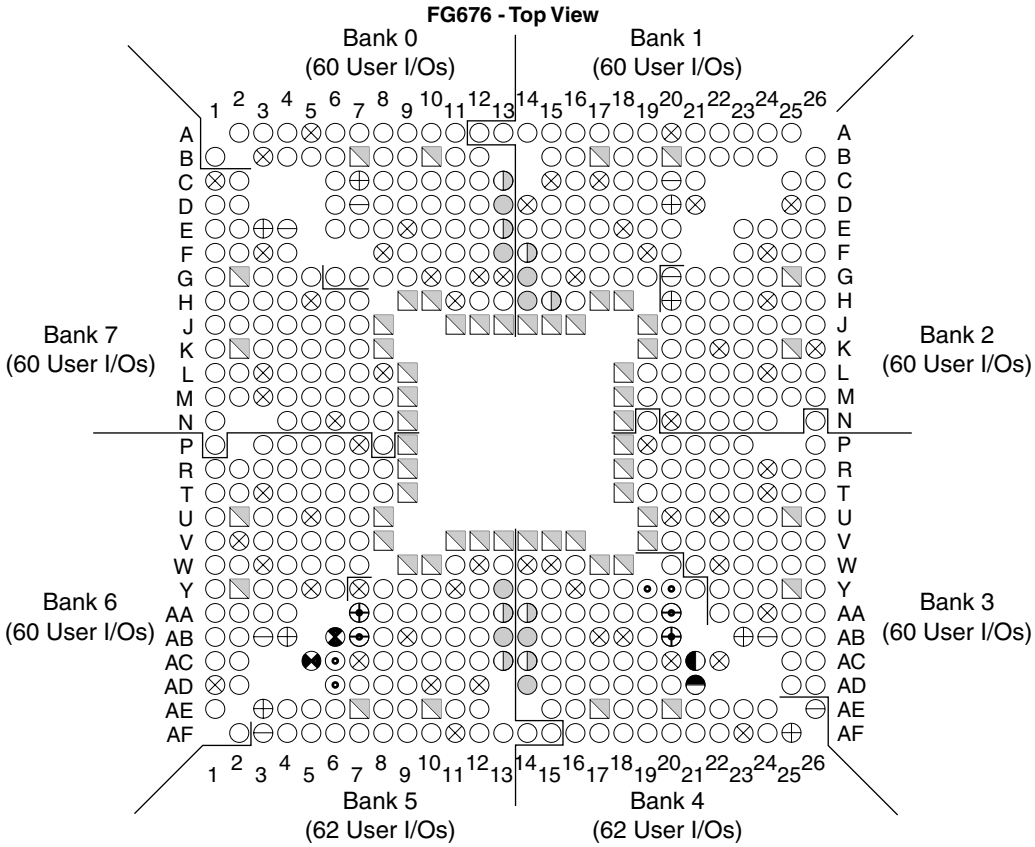
*Figure 4-8:* **FG676 Fine-Pitch BGA Composite Pinout Diagram**

## FG676 Bank Information




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| DIN/D0-D7 | | |
| CS_B | | |
| RDWR_B | | VCCO |
| BUSY/DOUT | | |
| INIT_B | | |
| GCLKx (P) | | |
| GCLKx (S) | | |
| VRP | | |
| VRN | | |
| VREF | | |
| Triple-Purpose Pins: | | |
| D2, D4/ALT_VRP | | |
| D3, D5/ALT_VRN | | |

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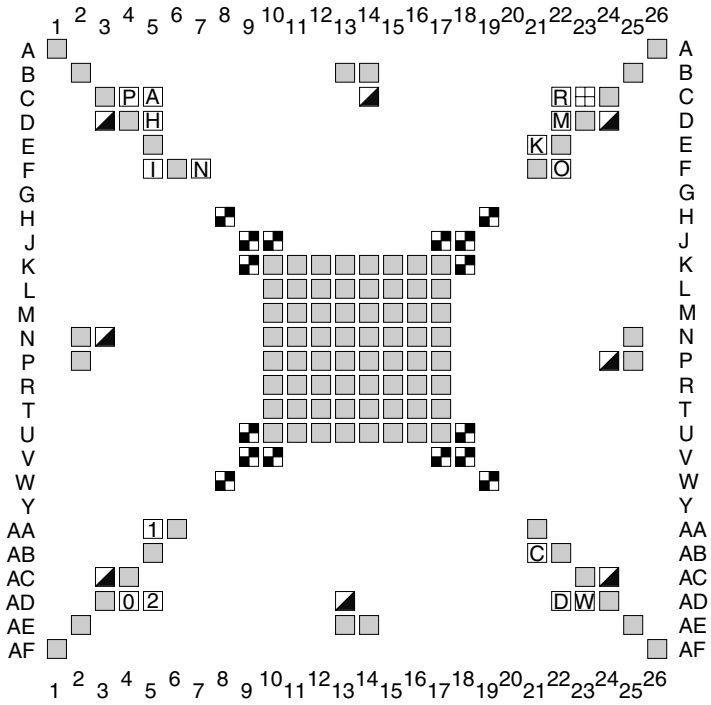
*Figure 4-9:* **FG676 Bank Information**

**FG676 - Top View**




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | N DXN |
| | P PROG_B | A DXP |
| | D DONE | VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | VCCAUX |
| | I TDI | VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

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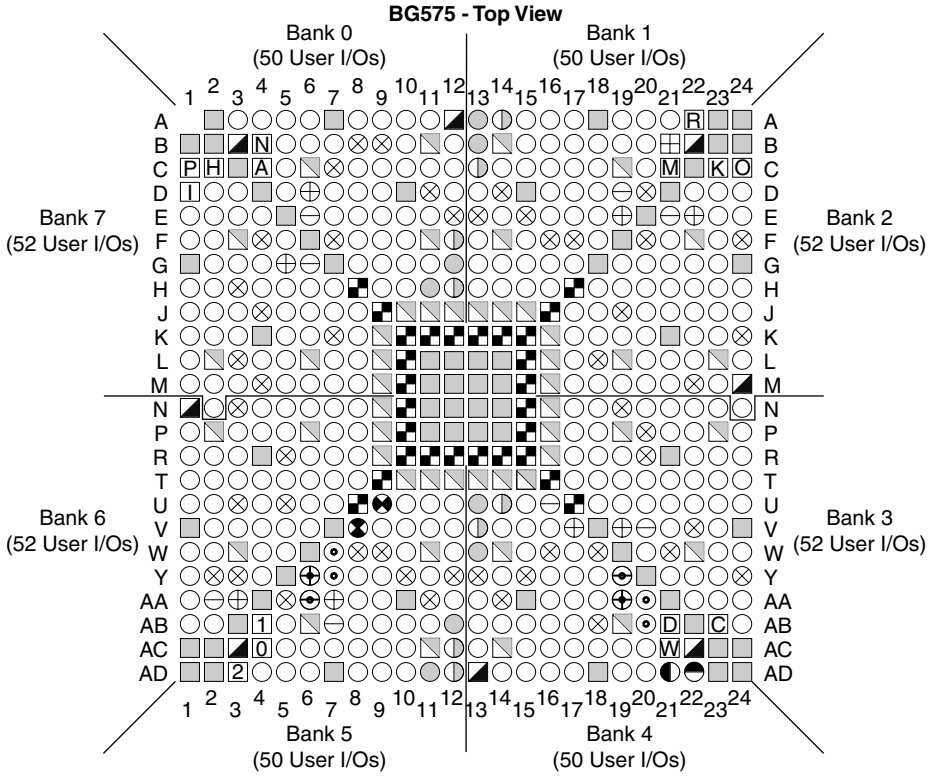
*Figure 4-10:* **FG676 Dedicated Pins**

# BG575 Standard BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊗ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⧓ | RDWR_B | H | HSWAP_EN | ◹ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◢ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▞ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊖ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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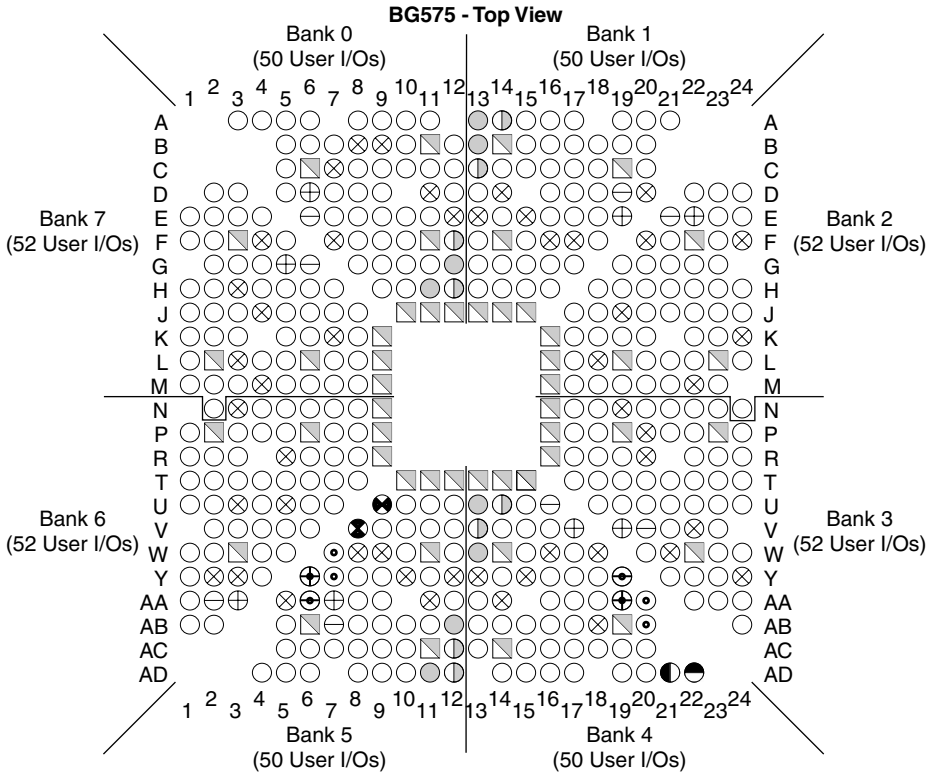
*Figure 4-11:* **BG575 Standard BGA Composite Pinout Diagram**




| User I/O Pins | | Dedicated Pins | |
|---|---|---|---|
| ○ | IO_LXXY_# | | |
| Dual-Purpose Pins: | | | |
| ⊙ | DIN/D0-D7 | | |
| ⊗ | CS_B | | |
| ⊗ | RDWR_B | | ▨ VCCO |
| ◓ | BUSY/DOUT | | |
| ◐ | INIT_B | | |
| ● | GCLKx (P) | | |
| ◑ | GCLKx (S) | | |
| ⊖ | VRP | | |
| ⊕ | VRN | | |
| ⊗ | VREF | | |
| Triple-Purpose Pins: | | | |
| ⊖ | D2, D4/ALT_VRP | | |
| ⊕ | D3, D5/ALT_VRN | | |

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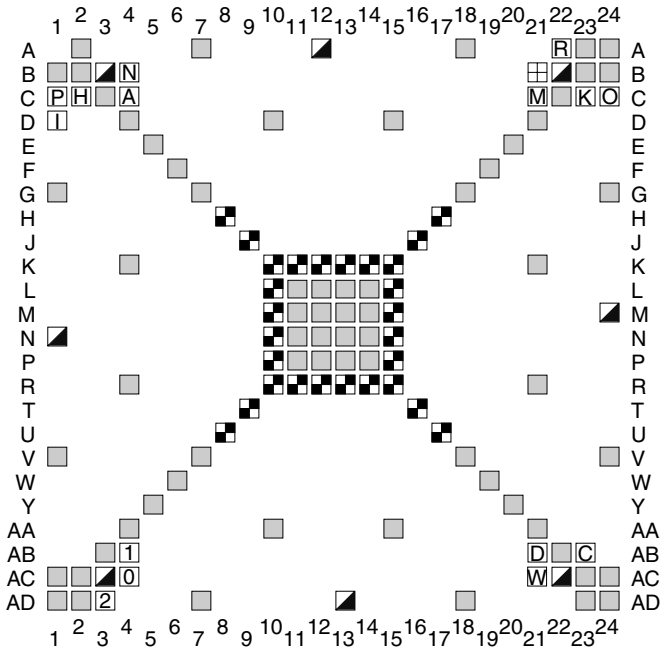
*Figure 4-12:* **BG575 Bank Information**

**BG575 - Top View**




| User I/O Pins | Dedicated Pins | | | |
|---|---|---|---|---|
| | C | CCLK | N | DXN |
| | P | PROG_B | A | DXP |
| | D | DONE | | VBATT |
| | 2 1 0 | M2, M1, M0 | R | RSVD |
| | H | HSWAP_EN | | |
| | K | TCK | | VCCAUX |
| | I | TDI | | VCCINT |
| | O | TDO | | GND |
| | M | TMS | n | NO CONNECT |
| | W | PWRDWN_B | | |

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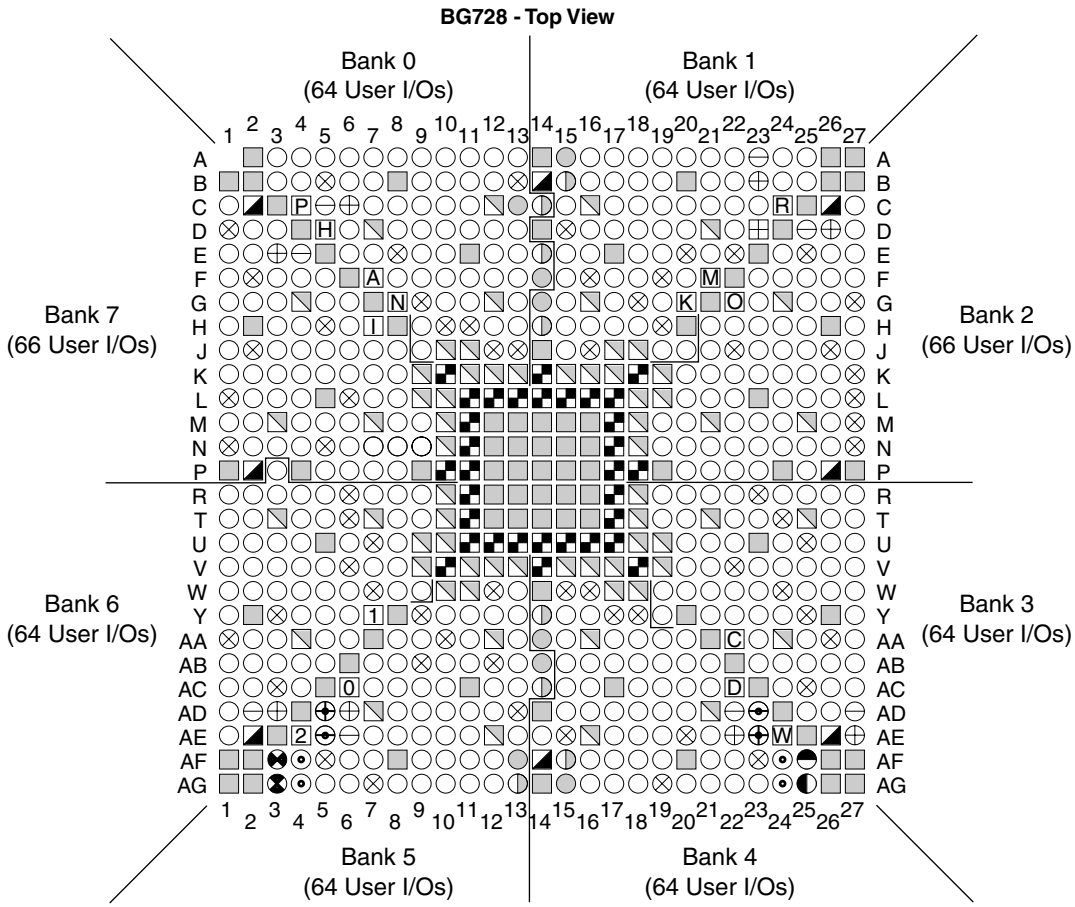
*Figure 4-13:* **BG575 Dedicated Pins**

# BG728 Standard BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊠ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊠ | RDWR_B | H | HSWAP_EN | ▧ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◢ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▩ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊖ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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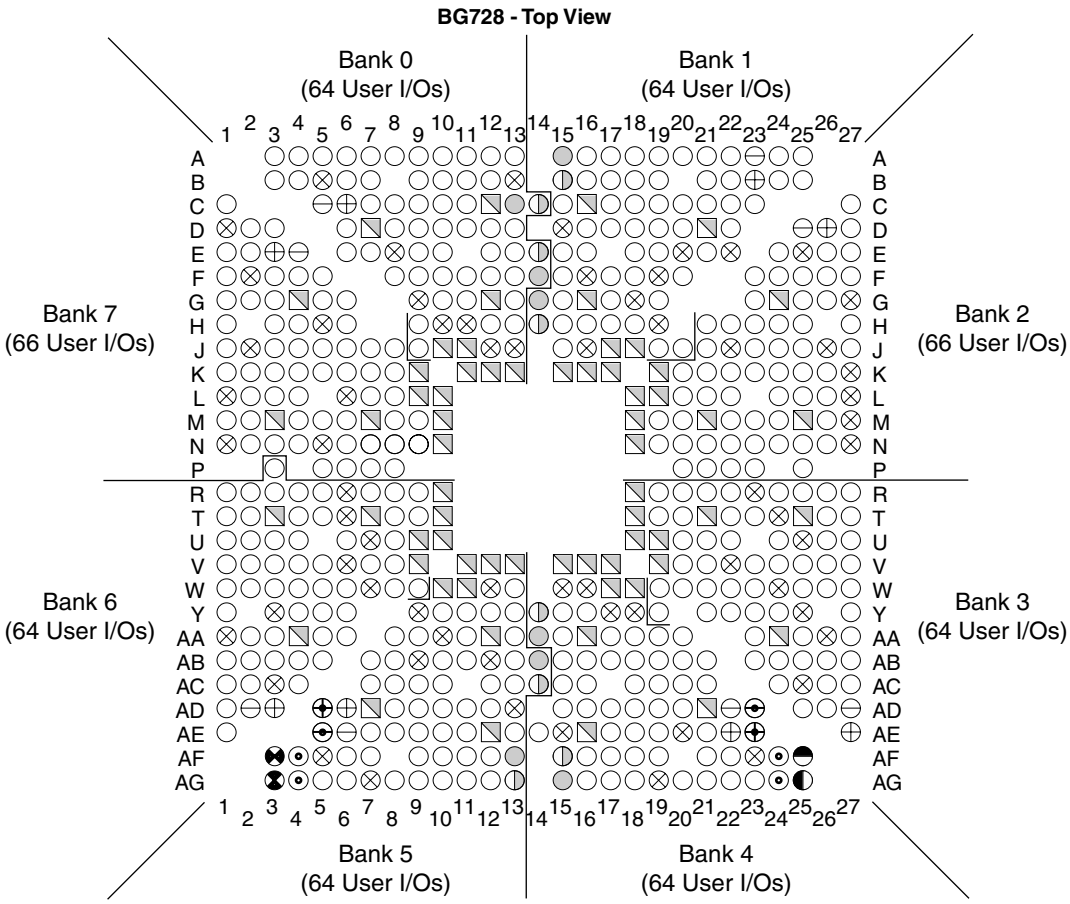
*Figure 4-14:* **BG728 Standard BGA Composite Pinout Diagram**

## BG728 Bank Information




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| ⊙ DIN/D0-D7 | | |
| CS_B | | |
| RDWR_B | | ▨ VCCO |
| BUSY/DOUT | | |
| INIT_B | | |
| GCLKx (P) | | |
| GCLKx (S) | | |
| ⊖ VRP | | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| D2, D4/ALT_VRP | | |
| D3, D5/ALT_VRN | | |

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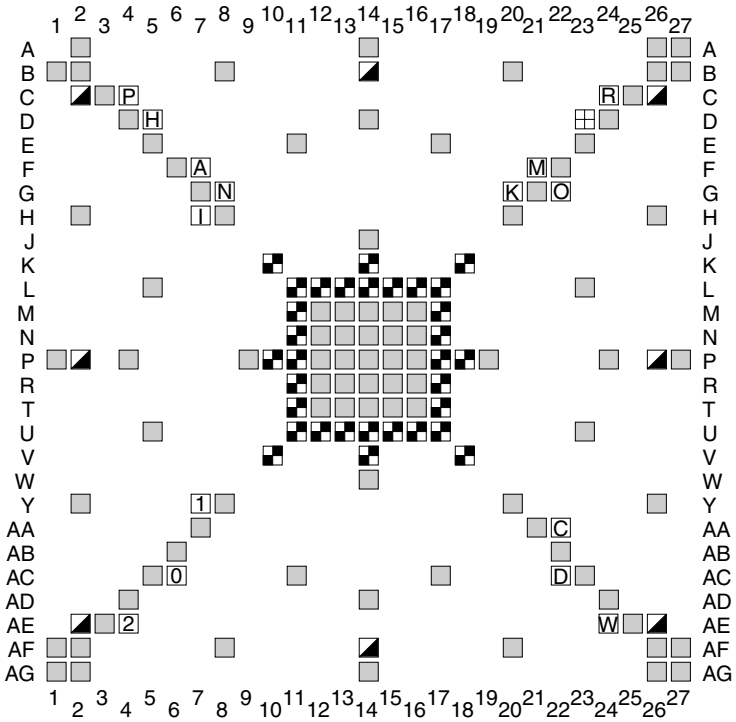
*Figure 4-15:* **BG728 Bank Information**

**BG728 - Top View**




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | N DXN |
| | P PROG_B | A DXP |
| | D DONE | VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | VCCAUX |
| | I TDI | VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

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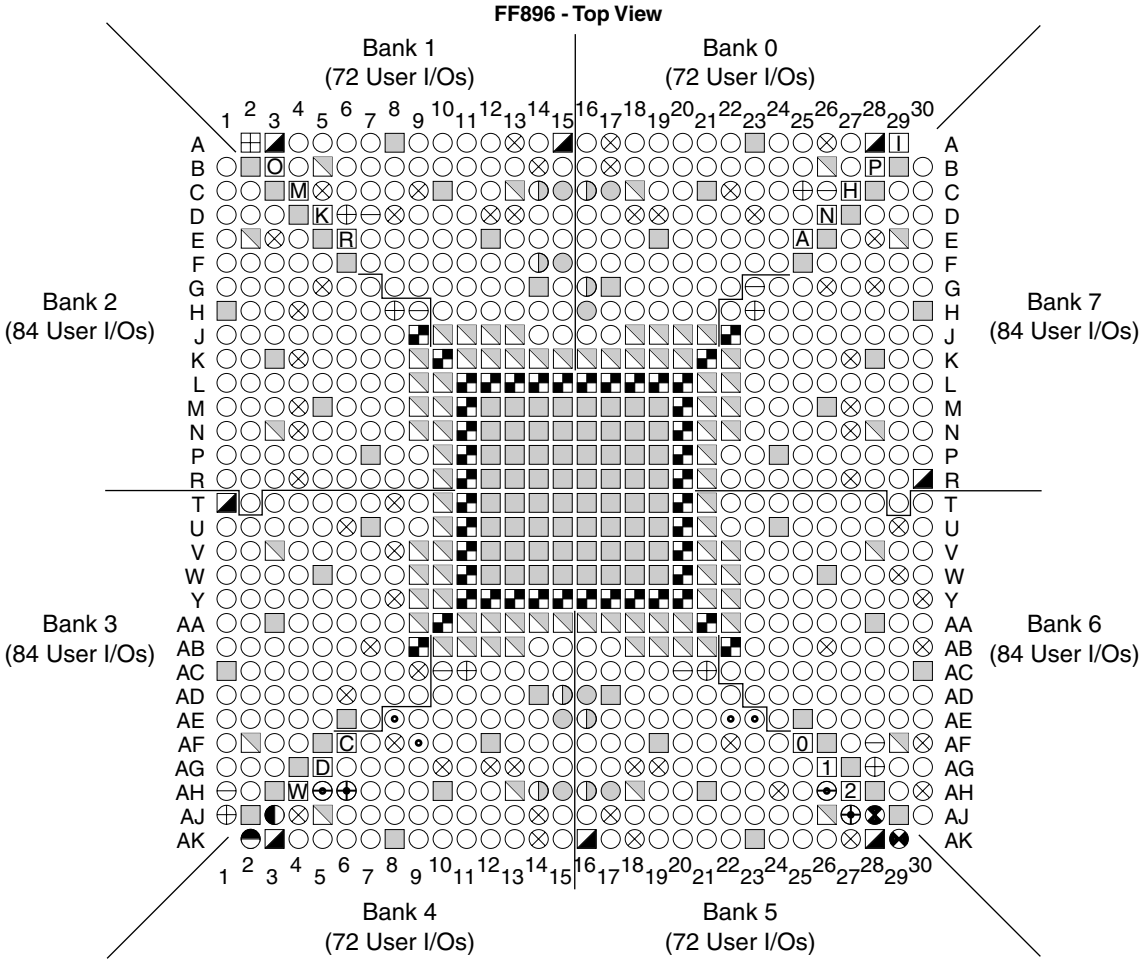
*Figure 4-16:* **BG728 Dedicated Pins**

# FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊠ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊗ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◪ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▩ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊖ | D2,D4/ALT_VRP | | | | |
| ⊕ | D3,D5/ALT_VRN | | | | |

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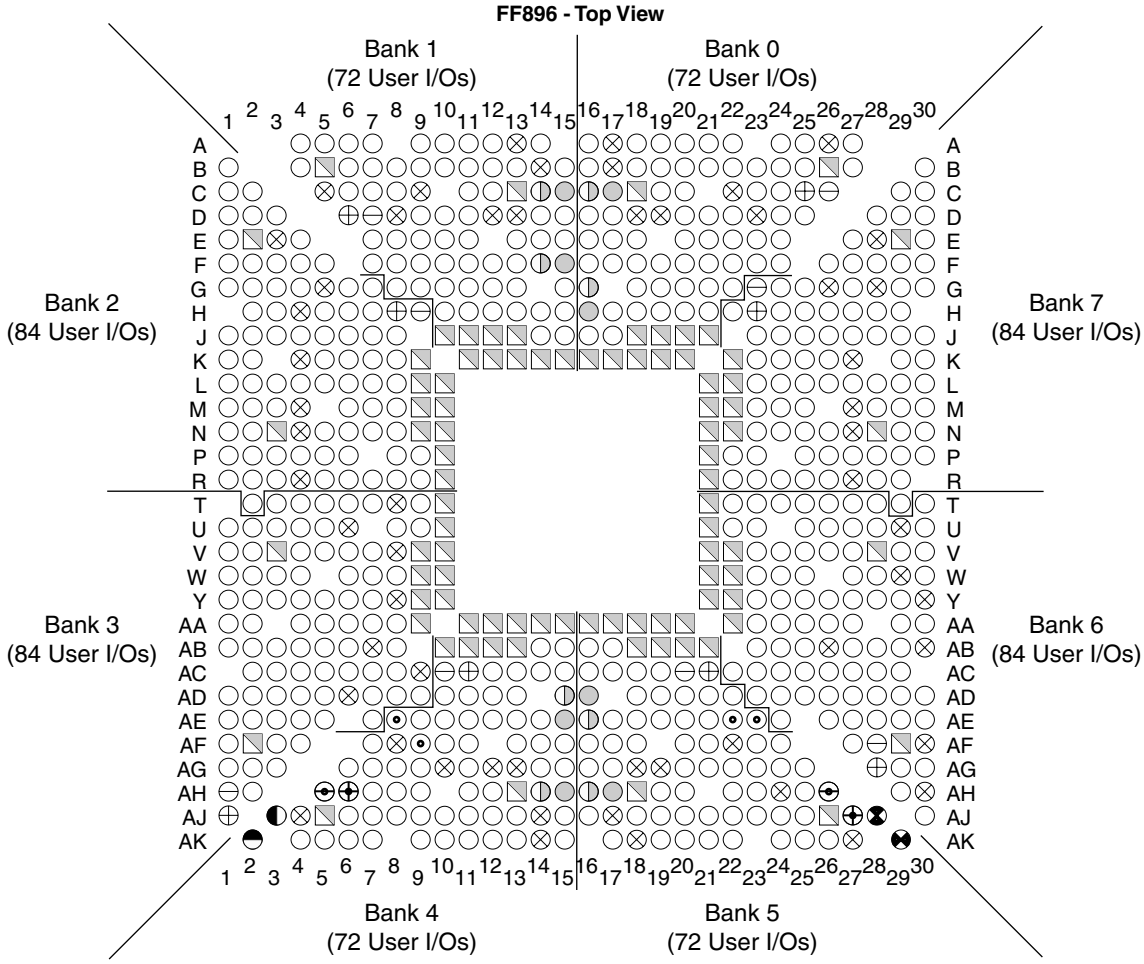
*Figure 4-17:* **FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

## FF896 Bank Information




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| ⊙ DIN/D0-D7 | | |
| ⊗ CS_B | | |
| ⊗ RDWR_B | | ▨ VCCO |
| ◓ BUSY/DOUT | | |
| ◐ INIT_B | | |
| ● GCLKx (P) | | |
| ◑ GCLKx (S) | | |
| ⊖ VRP | | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

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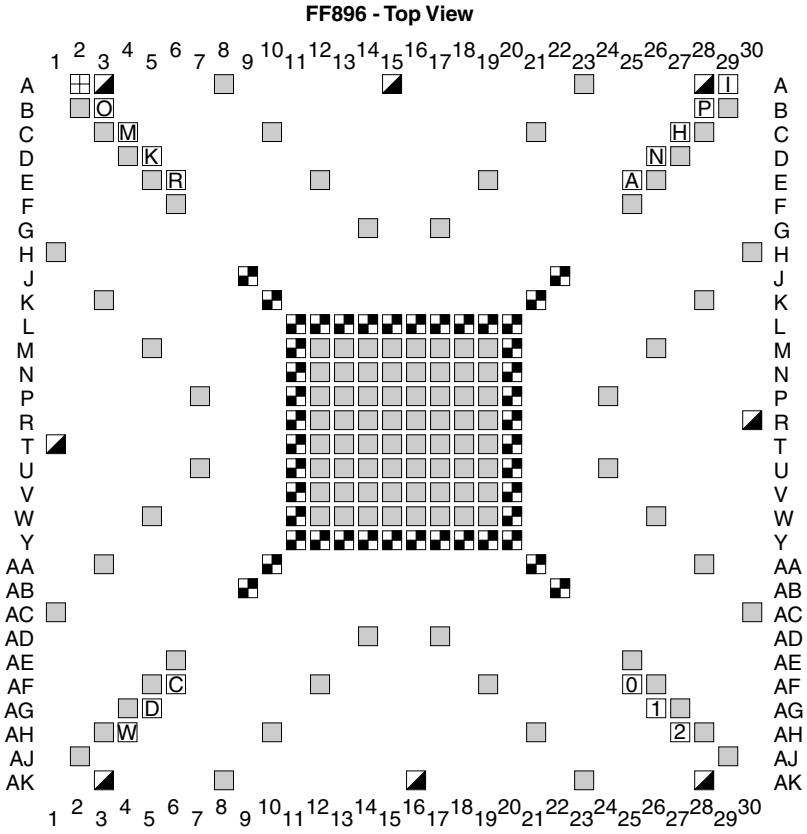
*Figure 4-18:* **FF896 Bank Information**

# FF896 Dedicated Pins




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | N DXN |
| | P PROG_B | A DXP |
| | D DONE | VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | VCCAUX |
| | I TDI | VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

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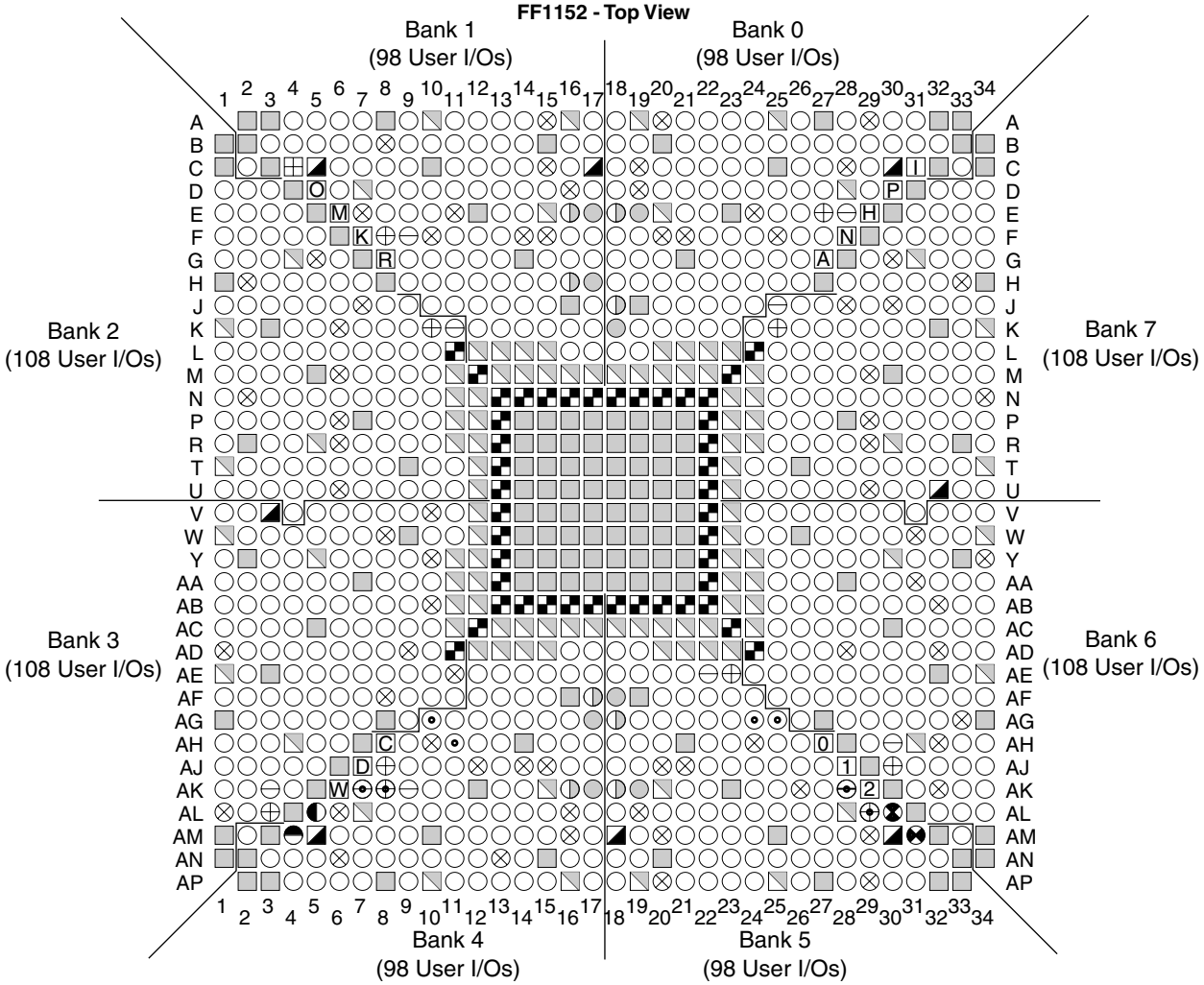
*Figure 4-19:* **FF896 Dedicated Pins**

# FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

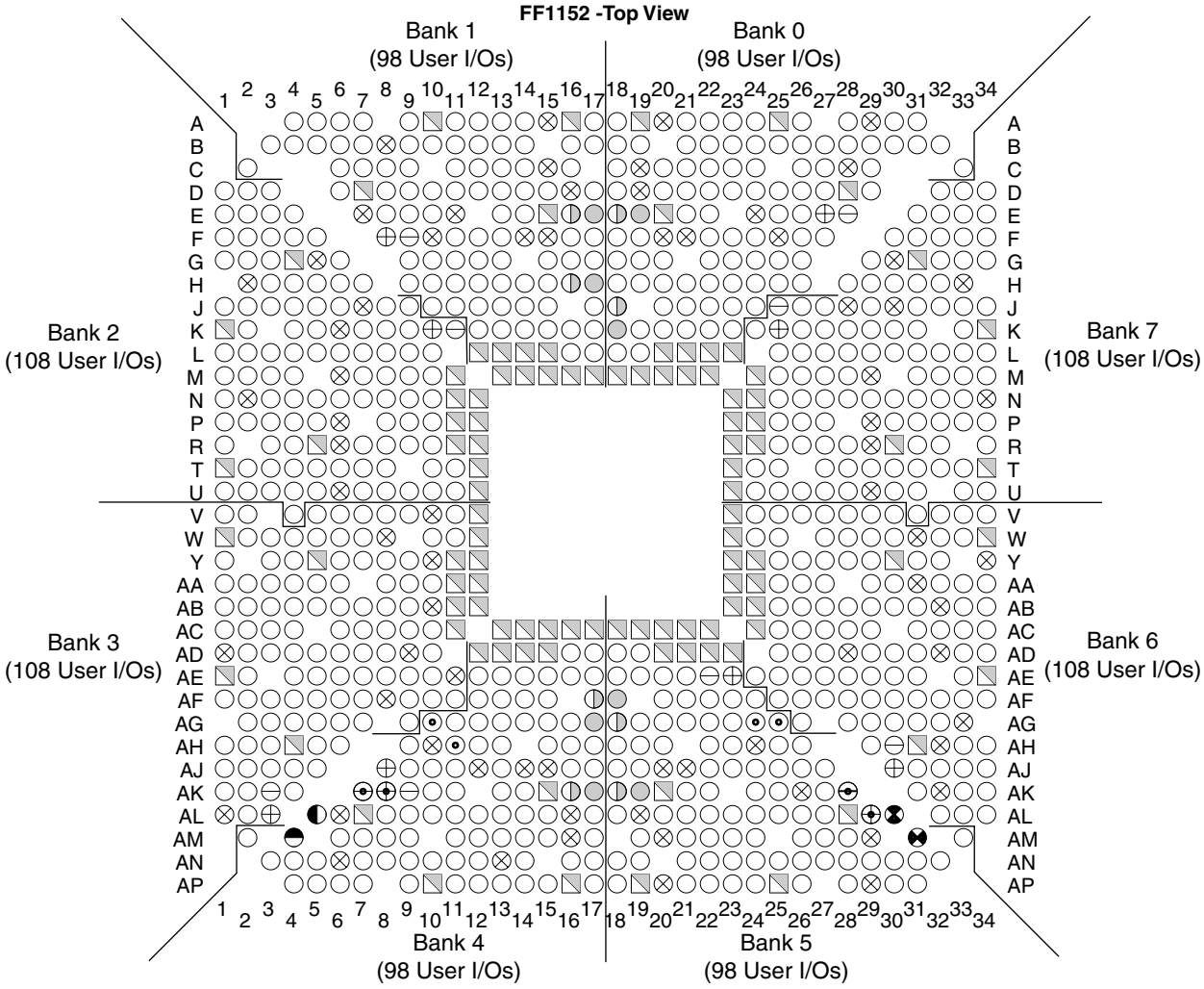



| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | C CCLK | N DXN |
| Dual-Purpose Pins: | P PROG_B | A DXP |
| ⊙ DIN/D0-D7 | D DONE | ⊞ VBATT |
| ⊗ CS_B | 2 1 0 M2, M1, M0 | R RSVD |
| ⊗ RDWR_B | H HSWAP_EN | ▨ VCCO |
| ◓ BUSY/DOUT | K TCK | ◪ VCCAUX |
| ◐ INIT_B | I TDI | ▩ VCCINT |
| ● GCLKx (P) | O TDO | ■ GND |
| ◑ GCLKx (S) | M TMS | n NO CONNECT |
| ⊖ VRP | W PWRDWN_B | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

ug002_c4_53_031501

*Figure 4-20:* **FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

## FF1152 Bank Information

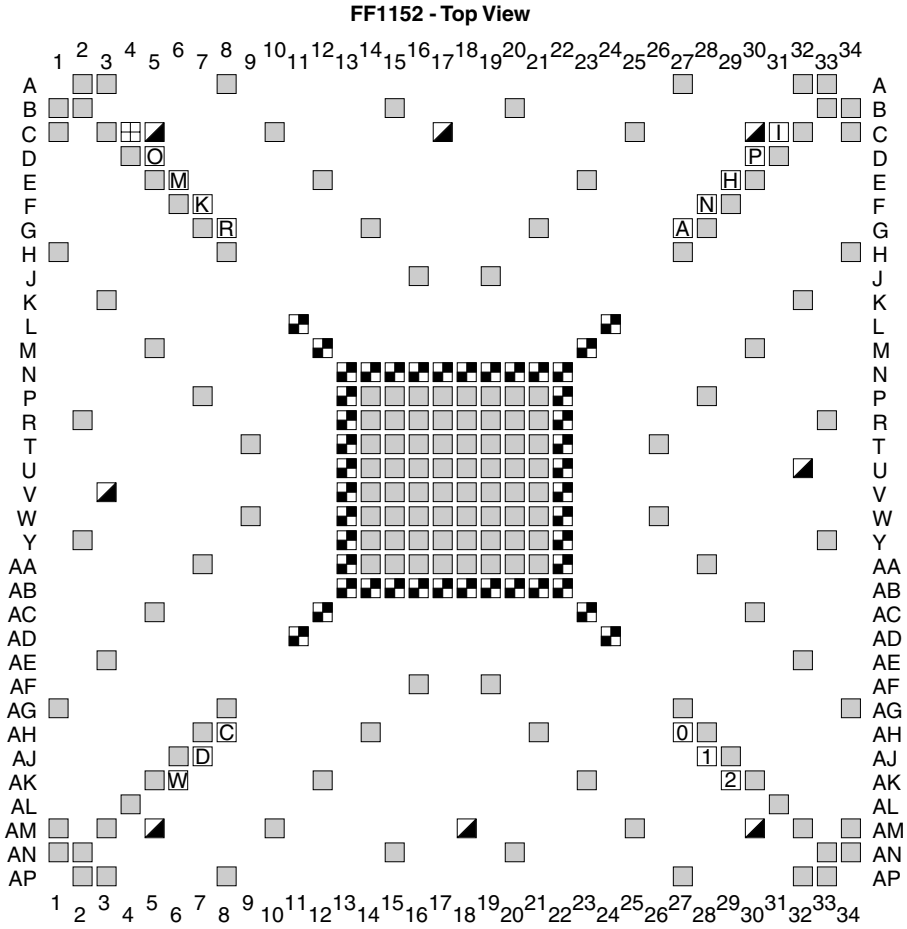



| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| ⊙ DIN/D0-D7 | | |
| ⊗ CS_B | | |
| ⊗ RDWR_B | | ▨ VCCO |
| ◓ BUSY/DOUT | | |
| ◐ INIT_B | | |
| ● GCLKx (P) | | |
| ◑ GCLKx (S) | | |
| ⊖ VRP | | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

ug002_c4_53b_031501

*Figure 4-21:* **FF1152 Bank Information**

# FF1152 Dedicated Pins

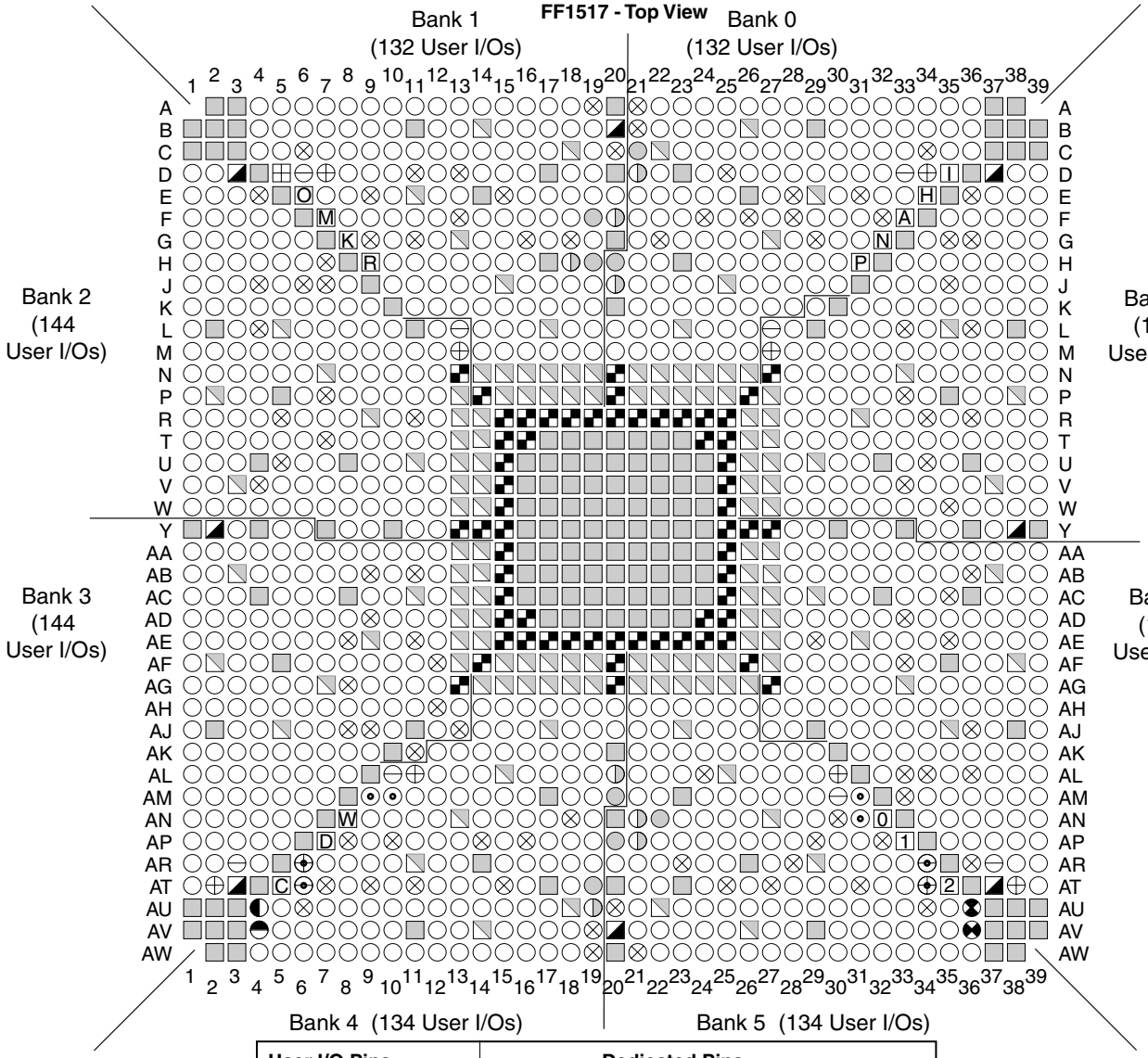



| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | N DXN |
| | P PROG_B | A DXP |
| | D DONE | VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | VCCAUX |
| | I TDI | VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

ug002_c4_53c_120400

*Figure 4-22:* **FF1152 Dedicated Pins**

# FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

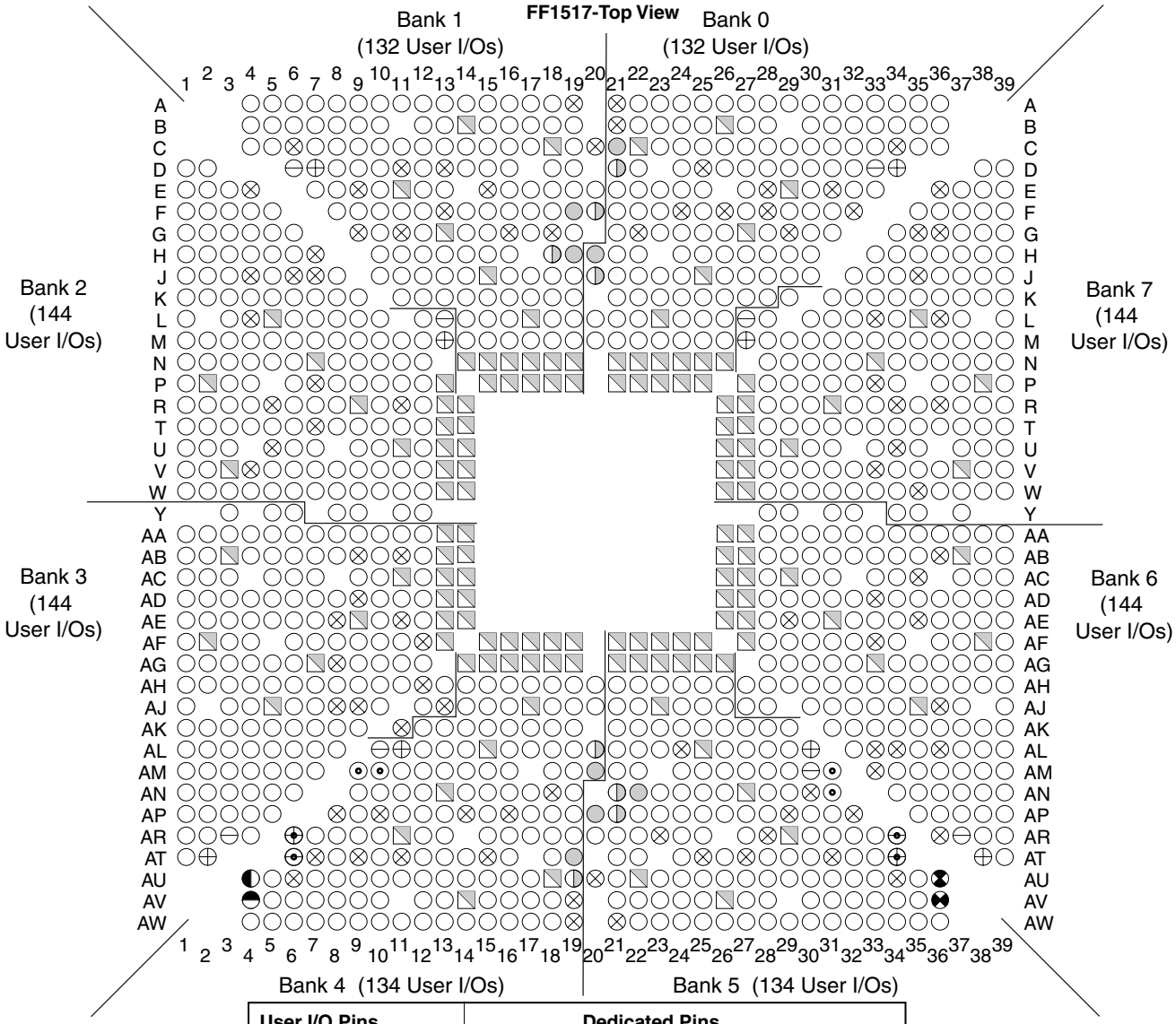



| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊗ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊗ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◪ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▩ | VCCINT |
| ● | GCLKx (P) | O | TDO | ■ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊛ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

ug002_c4_45_031501

*Figure 4-23:* **FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

## FF1517 Bank Information

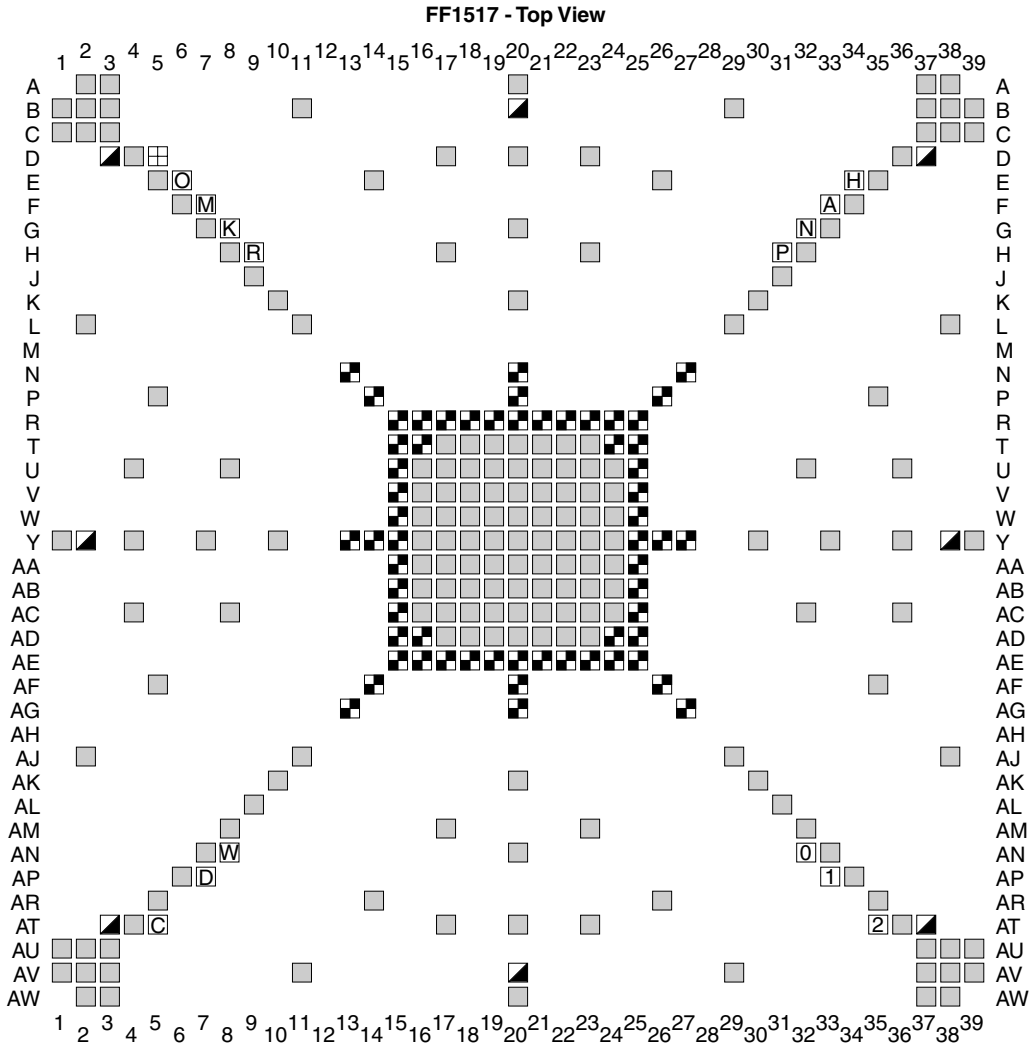



| User I/O Pins | Dedicated Pins | |
|---|---|---|
| IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| DIN/D0-D7 | | |
| CS_B | | |
| RDWR_B | | VCCO |
| BUSY/DOUT | | |
| INIT_B | | |
| GCLKx (P) | | |
| GCLKx (S) | | |
| VRP | | |
| VRN | | |
| VREF | | |
| Triple-Purpose Pins: | | |
| D2, D4/ALT_VRP | | |
| D3, D5/ALT_VRN | | |

ug002_c4_45b_031501

*Figure 4-24:* **FF1517 Bank Information**

# FF1517 Dedicated Pins

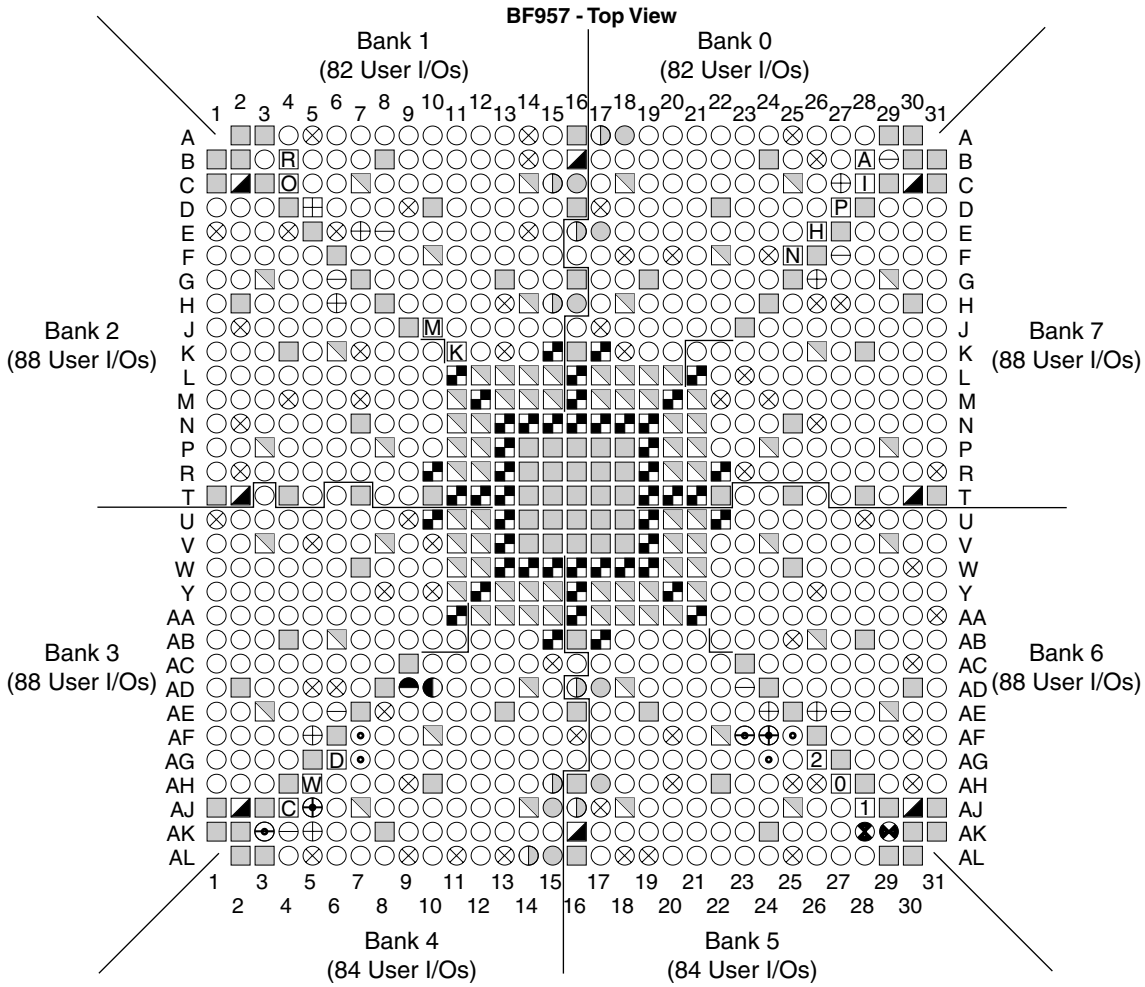



| User I/O Pins | Dedicated Pins | | | |
|---|---|---|---|---|
| | C | CCLK | N | DXN |
| | P | PROG_B | A | DXP |
| | D | DONE | | VBATT |
| | 2 1 0 | M2, M1, M0 | R | RSVD |
| | H | HSWAP_EN | | |
| | K | TCK | | VCCAUX |
| | I | TDI | | VCCINT |
| | O | TDO | | GND |
| | M | TMS | n | NO CONNECT |
| | W | PWRDWN_B | | |

ug002_c4_45c_120400

*Figure 4-25:* **FF1517 Dedicated Pins**

# BF957 Flip-Chip BGA Composite Pinout Diagram




| User I/O Pins | | Dedicated Pins | | | |
|---|---|---|---|---|---|
| ○ | IO_LXXY_# | C | CCLK | N | DXN |
| Dual-Purpose Pins: | | P | PROG_B | A | DXP |
| ⊙ | DIN/D0-D7 | D | DONE | ⊞ | VBATT |
| ⊗ | CS_B | 2 1 0 | M2, M1, M0 | R | RSVD |
| ⊗ | RDWR_B | H | HSWAP_EN | ▨ | VCCO |
| ◓ | BUSY/DOUT | K | TCK | ◪ | VCCAUX |
| ◐ | INIT_B | I | TDI | ▩ | VCCINT |
| ● | GCLKx (P) | O | TDO | ▨ | GND |
| ◑ | GCLKx (S) | M | TMS | n | NO CONNECT |
| ⊖ | VRP | W | PWRDWN_B | | |
| ⊕ | VRN | | | | |
| ⊗ | VREF | | | | |
| Triple-Purpose Pins: | | | | | |
| ⊖ | D2, D4/ALT_VRP | | | | |
| ⊕ | D3, D5/ALT_VRN | | | | |

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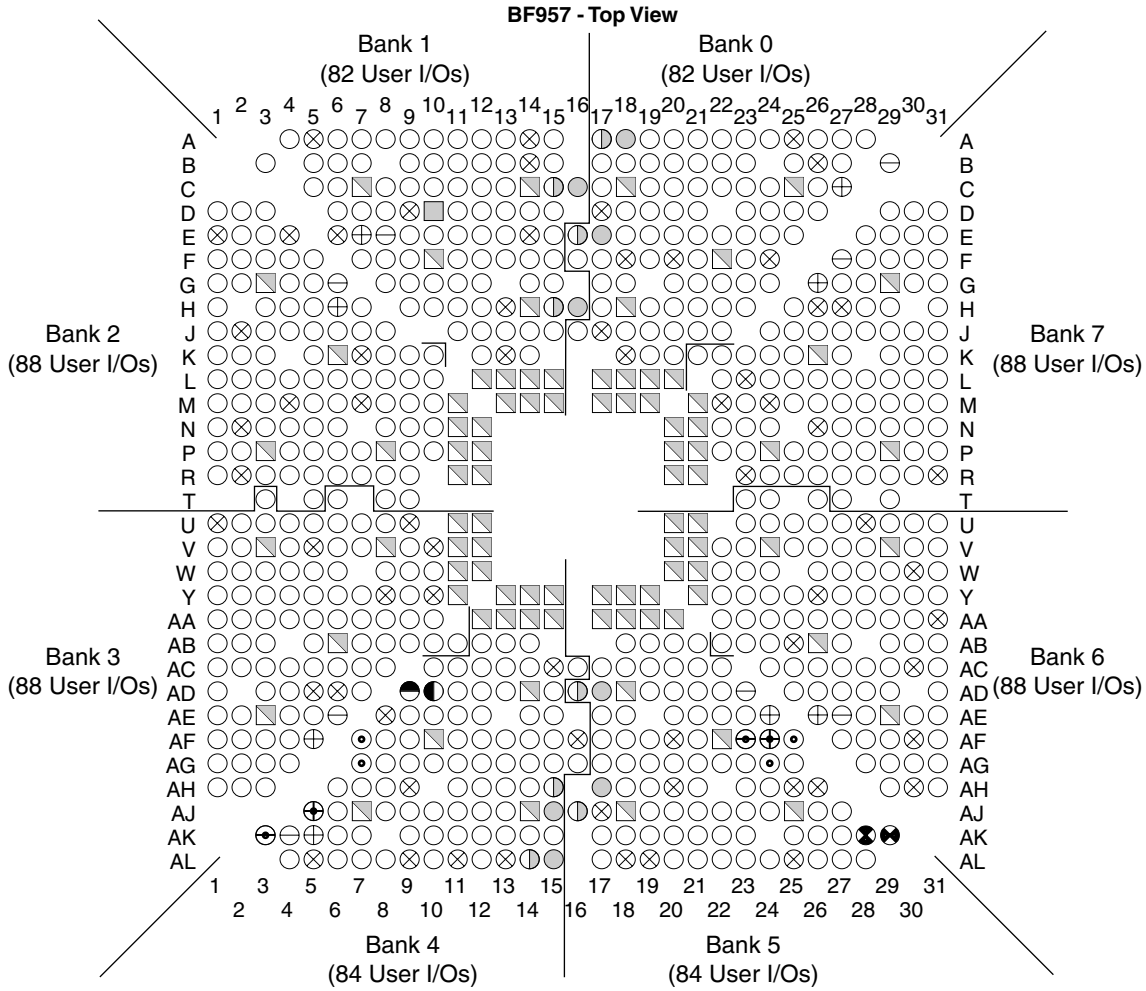
*Figure 4-26:* **BF957 Flip-Chip BGA Composite Pinout Diagram**

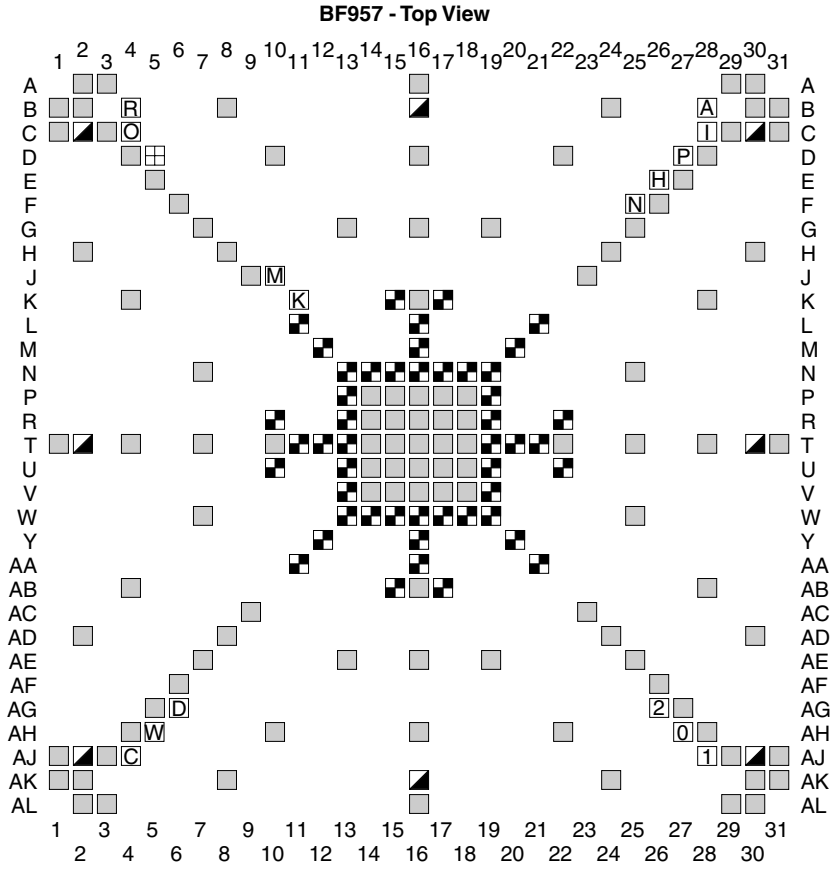
# BF957 Bank Information




| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | | |
| Dual-Purpose Pins: | | |
| ⊙ DIN/D0-D7 | | |
| ⊗ CS_B | | |
| ⧗ RDWR_B | | ▨ VCCO |
| ◓ BUSY/DOUT | | |
| ◐ INIT_B | | |
| ● GCLKx (P) | | |
| ◑ GCLKx (S) | | |
| ⊖ VRP | | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊖ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

ug002_c4_54b_032901

*Figure 4-27:* **BF957 Bank Information**



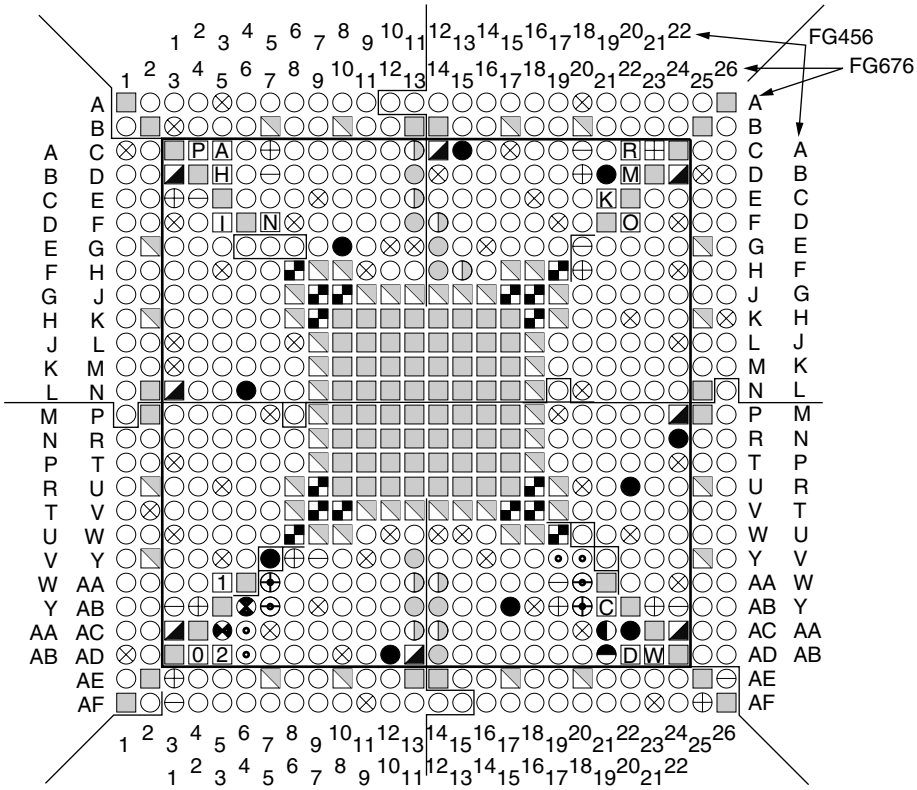

| User I/O Pins | Dedicated Pins | |
|---|---|---|
| | C CCLK | N DXN |
| | P PROG_B | A DXP |
| | D DONE | VBATT |
| | 2 1 0 M2, M1, M0 | R RSVD |
| | H HSWAP_EN | |
| | K TCK | VCCAUX |
| | I TDI | VCCINT |
| | O TDO | GND |
| | M TMS | n NO CONNECT |
| | W PWRDWN_B | |

ug002_c4_54c_120400

*Figure 4-28:* **BF957 Dedicated Pins**

# FG456 - FG676 Pinout Compatibility Diagram

**FG676/FG456 Pinout Compatible Diagram - Top View**




**Note:** FF456 and FG676 are pinout compatible with with the exception of the LVDS pairs. I/O $V_{REF}$ pins in FG676 are user I/O pins in FG456. In addition, some user I/O pins are not in the same bank (see ◯◯ lines). VRP (V7) and VRN (V6) in Bank 5 and VRP (W17) and VRN (Y17) in Bank 4 are only user I/Os in FG676.

| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ◯ IO_LXXY_# | C CCLK | N DXN |
| Dual-Purpose Pins: | P PROG_B | A DXP |
| ⊙ DIN/D0-D7 | D DONE | ⊞ VBATT |
| ⊗ CS_B | 2 1 0 M2, M1, M0 | R RSVD |
| ⊗ RDWR_B | H HSWAP_EN | ▨ VCCO |
| ◓ BUSY/DOUT | K TCK | ◪ VCCAUX |
| ◐ INIT_B | I TDI | ▩ VCCINT |
| ● GCLKx (P) | O TDO | ■ GND |
| ◑ GCLKx (S) | M TMS | n NO CONNECT |
| ⊖ VRP | W PWRDWN_B | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| ● VREF on FG676 User I/O on FG456 | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

**Corresponding Pinouts**

| FG456 | FG676 |
|---|---|
| A1 | C3 |
| . | . |
| . | . |
| . | . |
| . | . |
| . | . |
| AB22 | AD24 |

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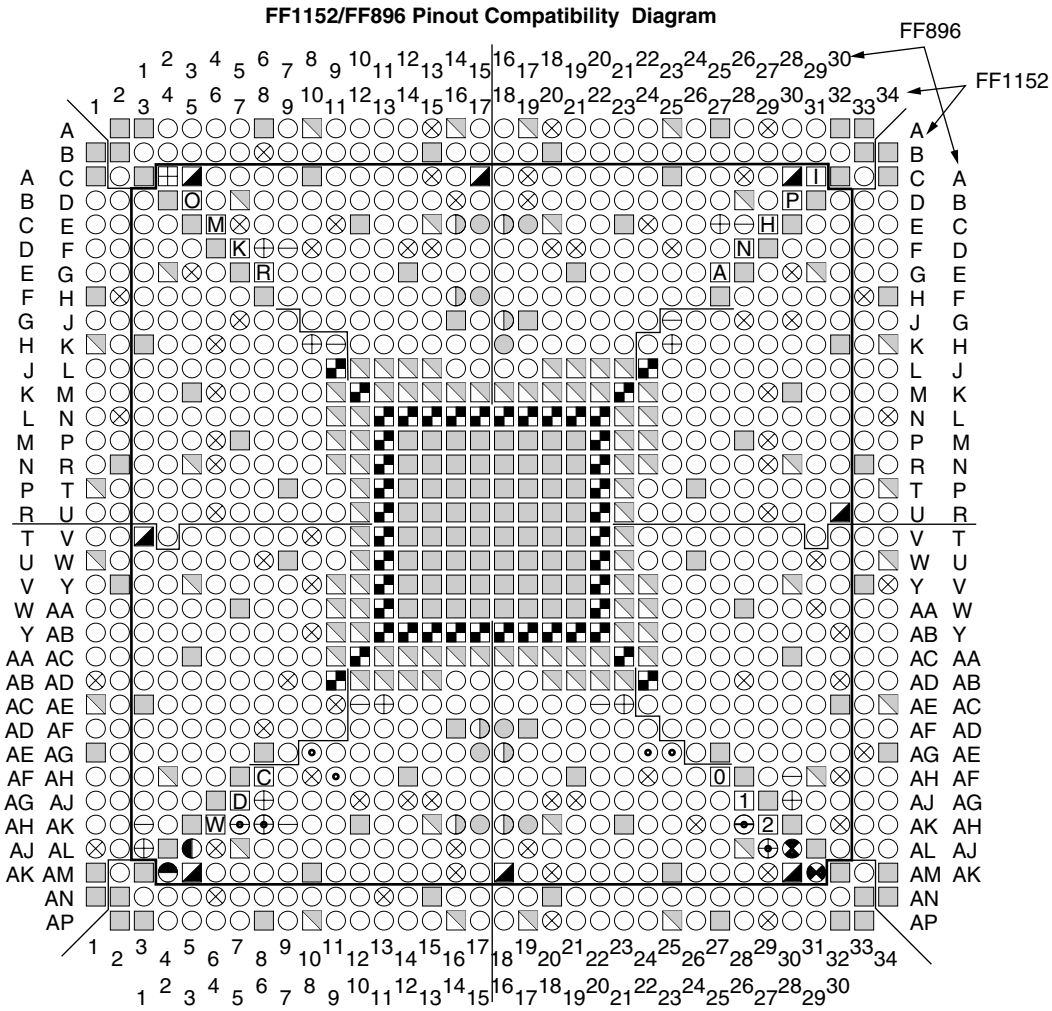
*Figure 4-29:* **FG456 - FG676 Pinout Compatibility Diagram**

# FF896 - FF1152 Pinout Compatibility Diagram




**Note:** FF896 is pinout compatible with the FF1152 except for LVDS pairs. Also, in Bank 4, VRP/VRN pins are not compatible: for FF896, VRP is in AC10 and VRN is in AC11, and for FF1152, VRP is in AK9 and VRN is in AJ8. If DCI is not used in Bank 4, or is used with ALT_VRP or ALT_VRN, then the user I/Os are compatible.

| User I/O Pins | Dedicated Pins | |
|---|---|---|
| ○ IO_LXXY_# | C CCLK | N DXN |
| Dual-Purpose Pins: | P PROG_B | A DXP |
| ⊙ DIN/D0-D7 | D DONE | ⊞ VBATT |
| ⊠ CS_B | 2 1 0 M2, M1, M0 | R RSVD |
| ⊠ RDWR_B | H HSWAP_EN | ▨ VCCO |
| ◓ BUSY/DOUT | K TCK | ◪ VCCAUX |
| ◐ INIT_B | I TDI | ▪ VCCINT |
| ● GCLKx (P) | O TDO | ▩ GND |
| ◑ GCLKx (S) | M TMS | n NO CONNECT |
| ⊖ VRP | W PWRDWN_B | |
| ⊕ VRN | | |
| ⊗ VREF | | |
| Triple-Purpose Pins: | | |
| ⊙ D2, D4/ALT_VRP | | |
| ⊕ D3, D5/ALT_VRN | | |

**Corresponding Pinouts**

| FF896 | FF1152 |
|---|---|
| A2 | C4 |
| . | . |
| . | . |
| . | . |
| . | . |
| . | . |
| AK29 | AM31 |

ug002_c4_55_032901

*Figure 4-30:* **FF896 - FF1152 Pinout Compatibility Diagram**