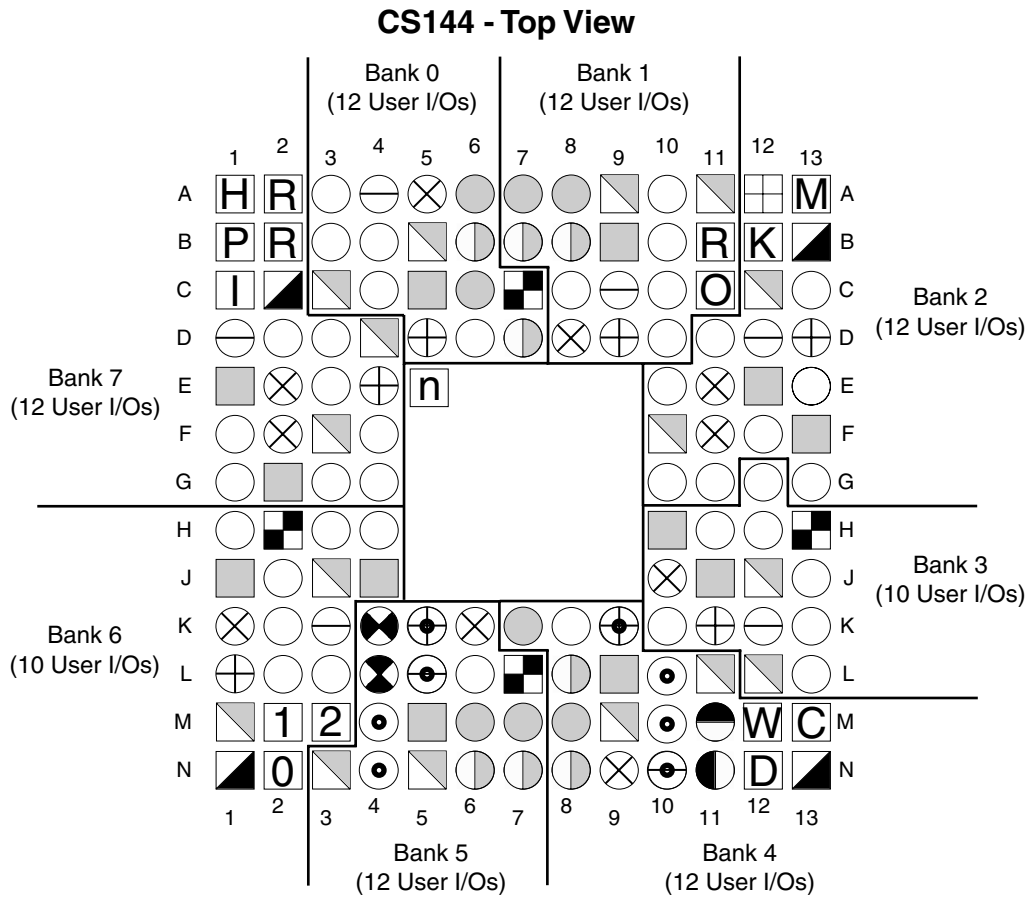


## Pinout Diagrams

This section contains pinout diagrams for the following Virtex-II packages:

- "CS144 Chip-Scale BGA Composite Pinout Diagram" on page 412
- "FG256 Fine-Pitch BGA Composite Pinout Diagram" on page 413
  - FG256 Bank Information
  - FG256 Dedicated Pins
- "FG456 Fine-Pitch BGA Composite Pinout Diagram" on page 417
  - FG456 Bank Information
  - FG456 Dedicated Pins
- "FG676 Fine-Pitch BGA Composite Pinout Diagram" on page 421
  - FG676 Bank Information
  - FG676 Dedicated Pins
- "BG575 Standard BGA Composite Pinout Diagram" on page 425
  - BG575 Bank Information
  - BG575 Dedicated Pins
- "BG728 Standard BGA Composite Pinout Diagram" on page 429
  - BG728 Bank Information
  - BG728 Dedicated Pins
- "FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 433
  - FF896 Bank Information
  - FF896 Dedicated Pins
- "FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 437
  - FF1152 Bank Information
  - FF1152 Dedicated Pins
- "FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 441
  - FF1517 Bank Information
  - FF1517 Dedicated Pins
- "BF957 Flip-Chip BGA Composite Pinout Diagram" on page 445
  - BF957 Bank Information
  - BF957 Dedicated Pins
- "FG456 - FG676 Pinout Compatibility Diagram" on page 448
- "FF896 - FF1152 Pinout Compatibility Diagram" on page 449

# CS144 Chip-Scale BGA Composite Pinout Diagram

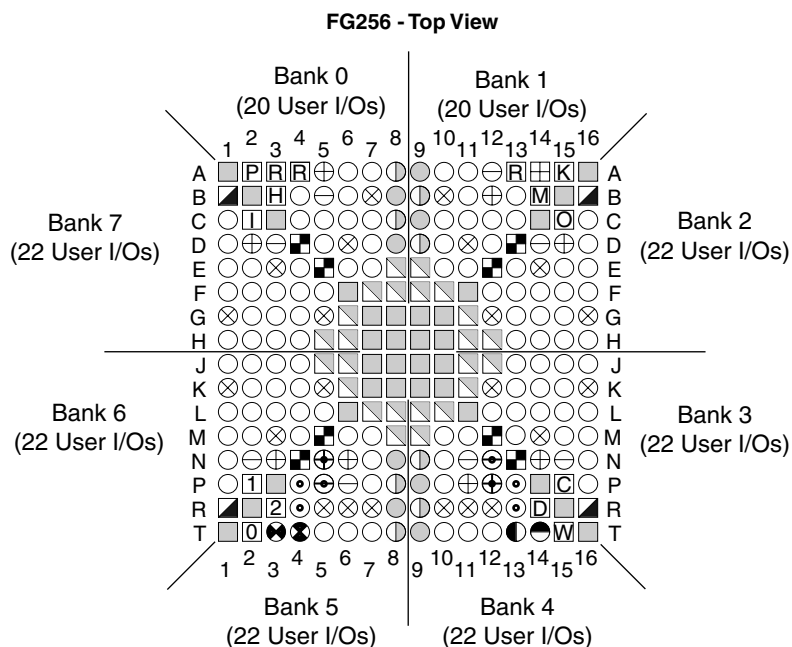


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	⊠ CCLK	⊞ VBATT
<u>Dual-Purpose Pins:</u>	⊡ PROG_B	⊞ RSVD
⊙ DIN/D0-D7	⊞ DONE	⊞ VCCO
⊗ CS_B	⊞ M2, M1, M0	⊞ VCCAUX
⊗ RDWR_B	⊞ HSWAP_EN	⊞ VCCINT
⊙ BUSY/DOUT	⊞ TCK	⊞ GND
⊙ INIT_B	⊞ TDI	⊞ NO CONNECT
⊙ GCLKx (P)	⊞ TDO	
⊙ GCLKx (S)	⊞ TMS	
⊖ VRP	⊞ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-1: CS144 Chip-Scale BGA Composite Pinout Diagram

# FG256 Fine-Pitch BGA Composite Pinout Diagram

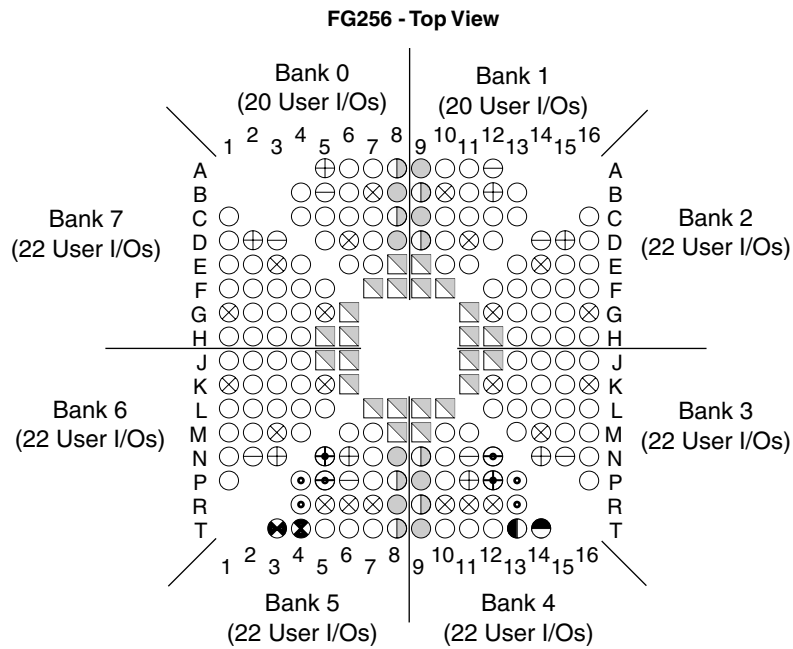


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	□ CCLK	
<u>Dual-Purpose Pins:</u>	□ PROG_B	
⊙ DIN/D0-D7	□ DONE	⊕ VBATT
⊗ CS_B	⊠ M2, M1, M0	⊠ RSVD
⊗ RDWR_B	⊠ HSWAP_EN	⊠ VCCO
⊖ BUSY/DOUT	⊠ TCK	⊠ VCCAUX
⊖ INIT_B	⊠ TDI	⊠ VCCINT
⊖ GCLKx (P)	⊠ TDO	⊠ GND
⊖ GCLKx (S)	⊠ TMS	⊠ NO CONNECT
⊖ VRP	⊠ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-2: FG256 Fine-Pitch BGA Composite Pinout Diagram

## FG256 Bank Information



User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
⊖ BUSY/DOUT		
◐ INIT_B		
◑ GCLKx (P)		
◑ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

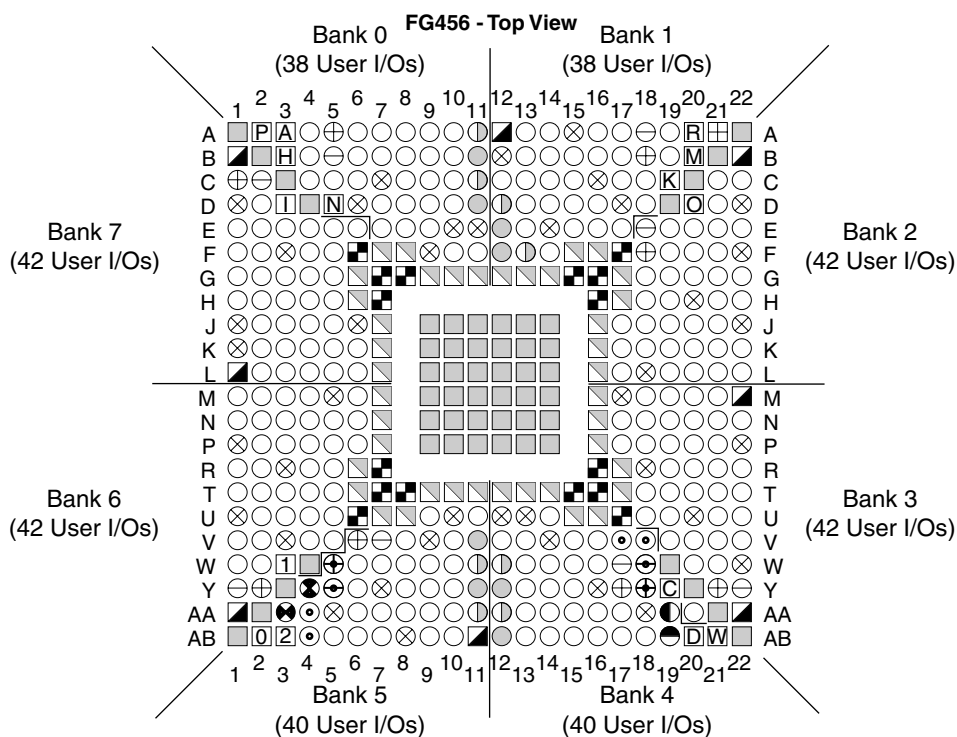
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Figure 4-3: FG256 Bank Information





# FG456 Fine-Pitch BGA Composite Pinout Diagram

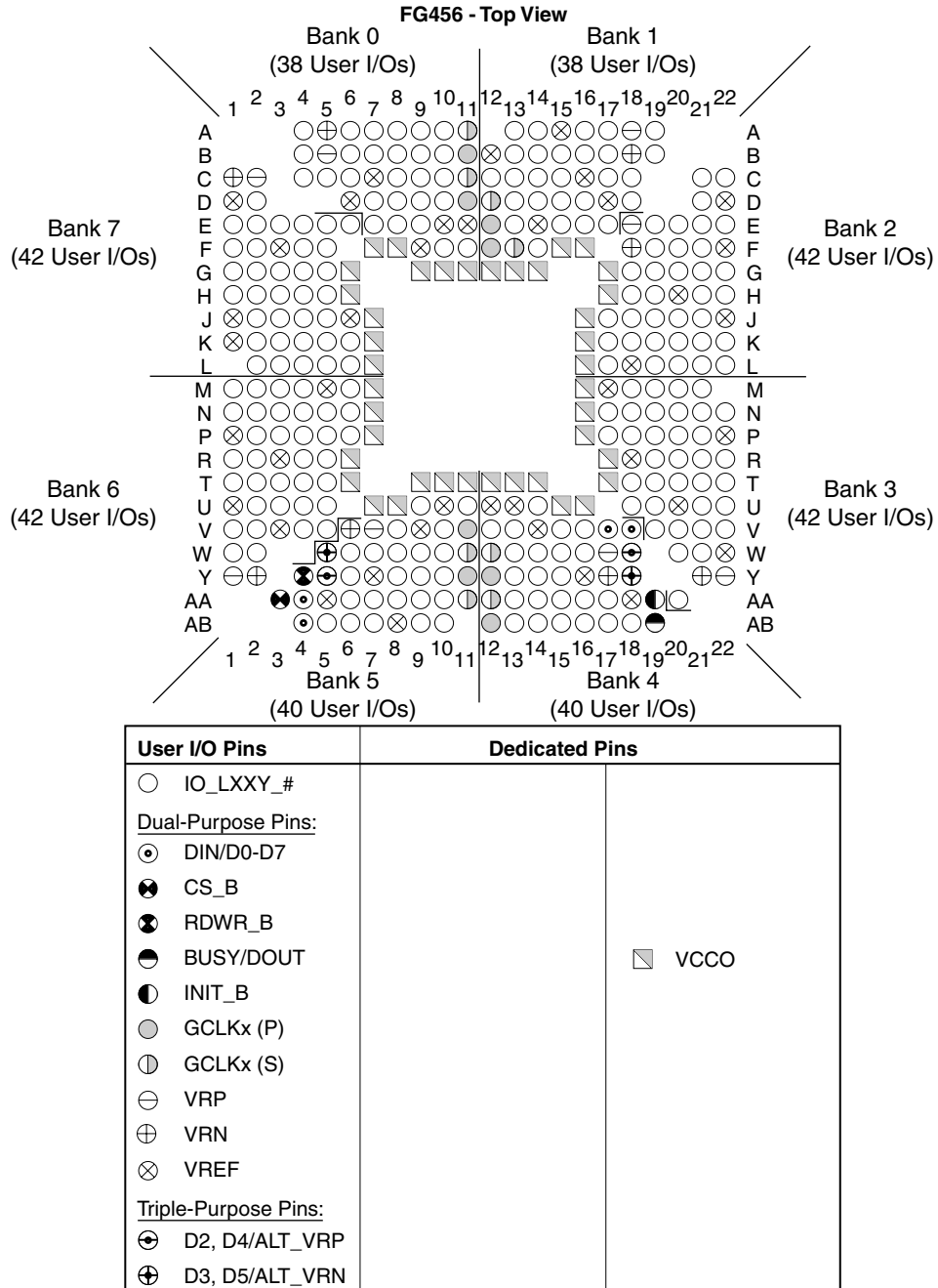


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊙ DIN/D0-D7	Ⓛ DONE	Ⓢ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓝ VCCO
⊙ BUSY/DOUT	Ⓚ TCK	Ⓜ VCCAUX
⊙ INIT_B	Ⓜ TDI	Ⓜ VCCINT
⊙ GCLKx (P)	Ⓞ TDO	Ⓜ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓝ NO CONNECT
⊖ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-5: FG456 Fine-Pitch BGA Composite Pinout Diagram

## FG456 Bank Information



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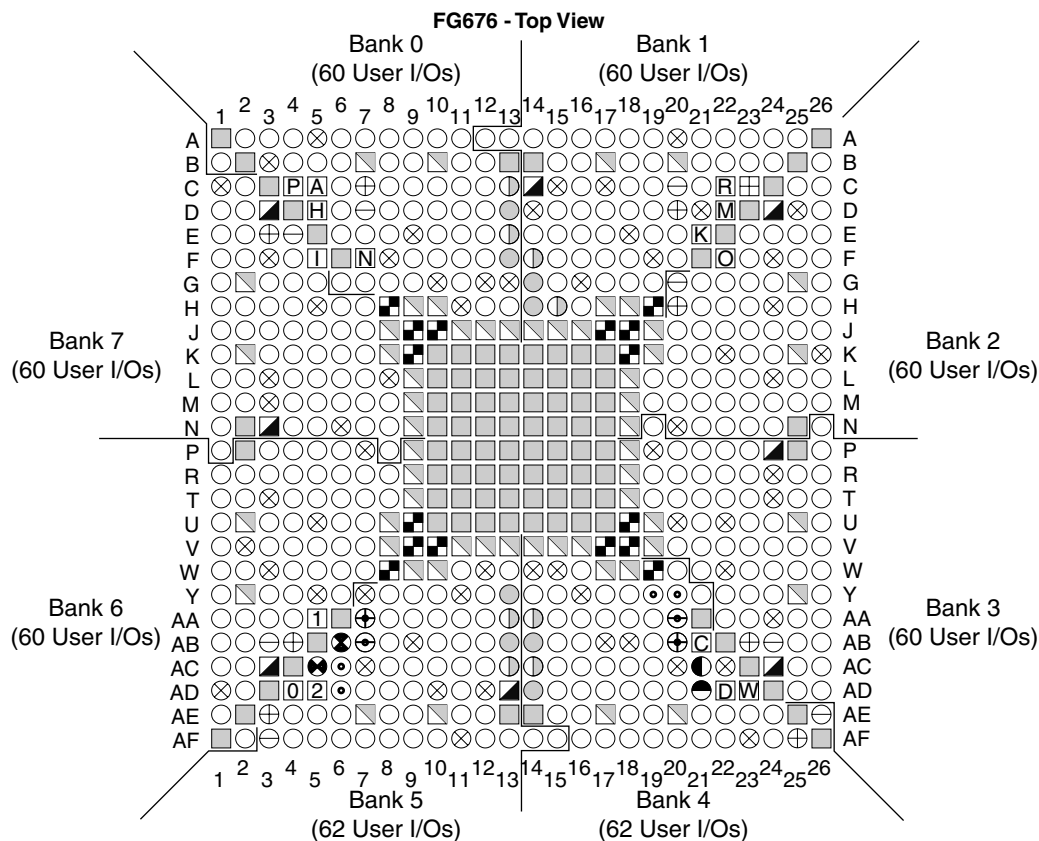
Figure 4-6: FG456 Bank Information







# FG676 Fine-Pitch BGA Composite Pinout Diagram



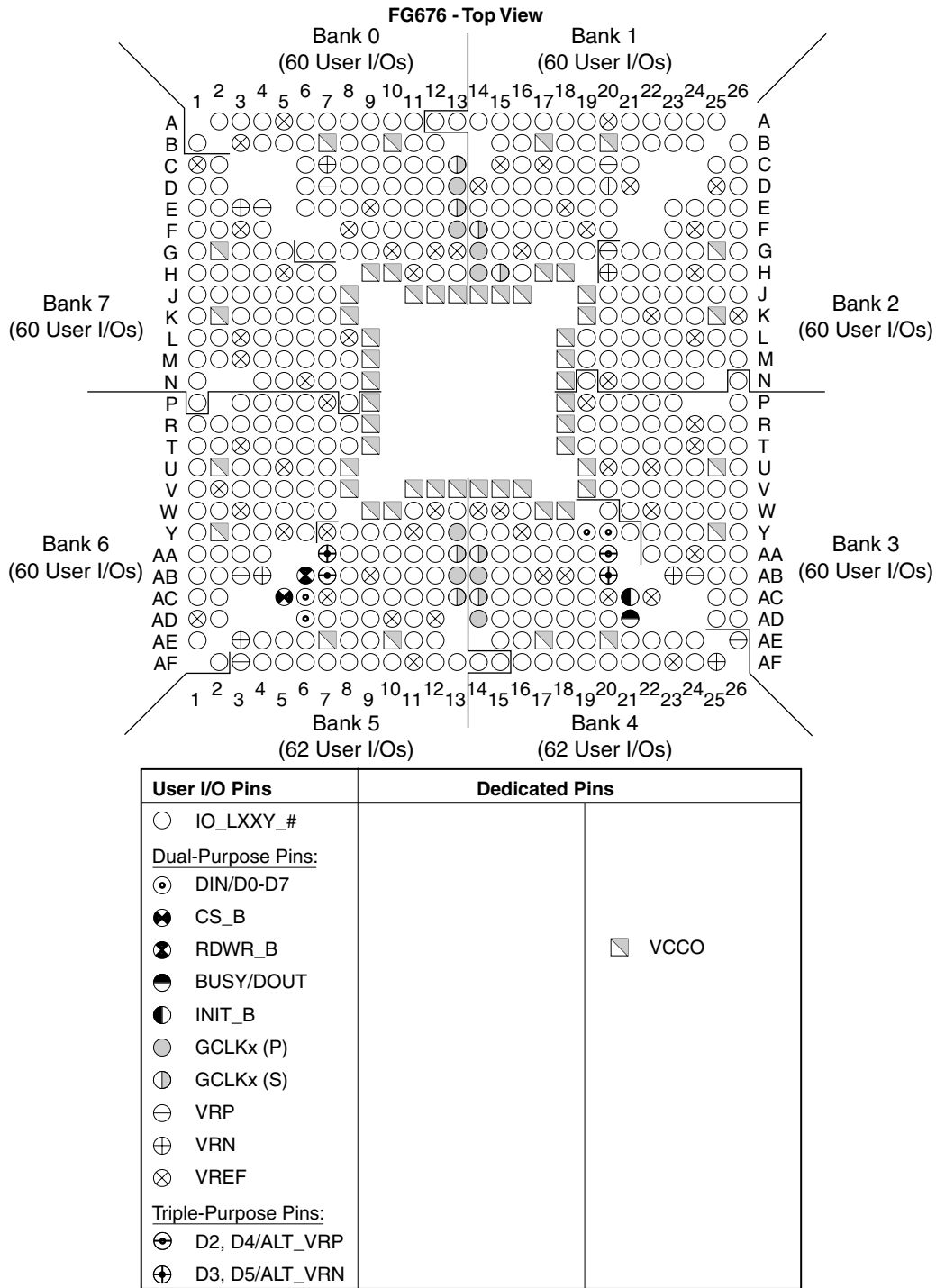
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊙ DIN/D0-D7	Ⓛ DONE	Ⓜ VBATT
⊗ CS_B	Ⓛ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓛ VCCO
⊗ BUSY/DOUT	Ⓜ TCK	Ⓛ VCCAUX
⊗ INIT_B	Ⓛ TDI	Ⓛ VCCINT
⊗ GCLKx (P)	Ⓛ TDO	Ⓛ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓛ NO CONNECT
⊗ VRP	Ⓜ PWRDWN_B	
⊗ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊗ D2, D4/ALT_VRP		
⊗ D3, D5/ALT_VRN		

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Figure 4-8: FG676 Fine-Pitch BGA Composite Pinout Diagram

## FG676 Bank Information

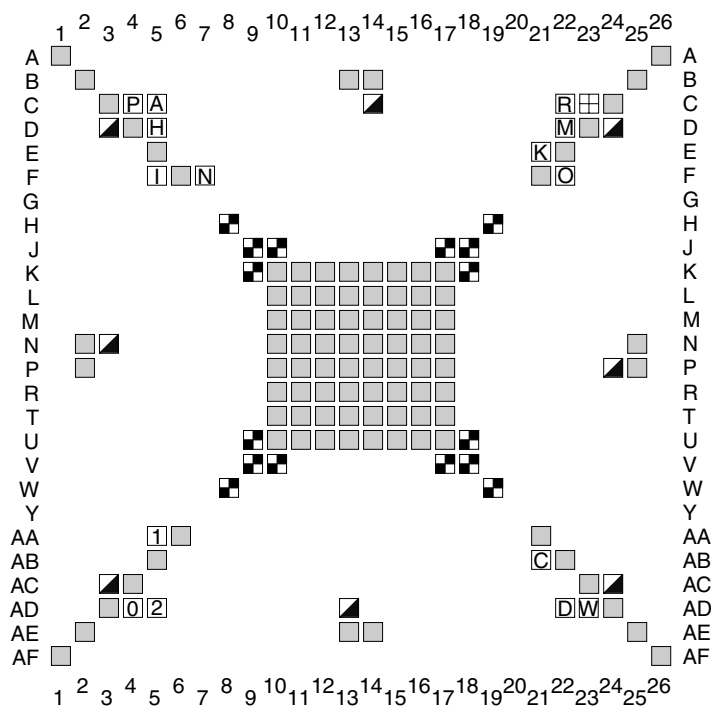


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Figure 4-9: FG676 Bank Information

# FG676 Dedicated Pins

FG676 - Top View



4

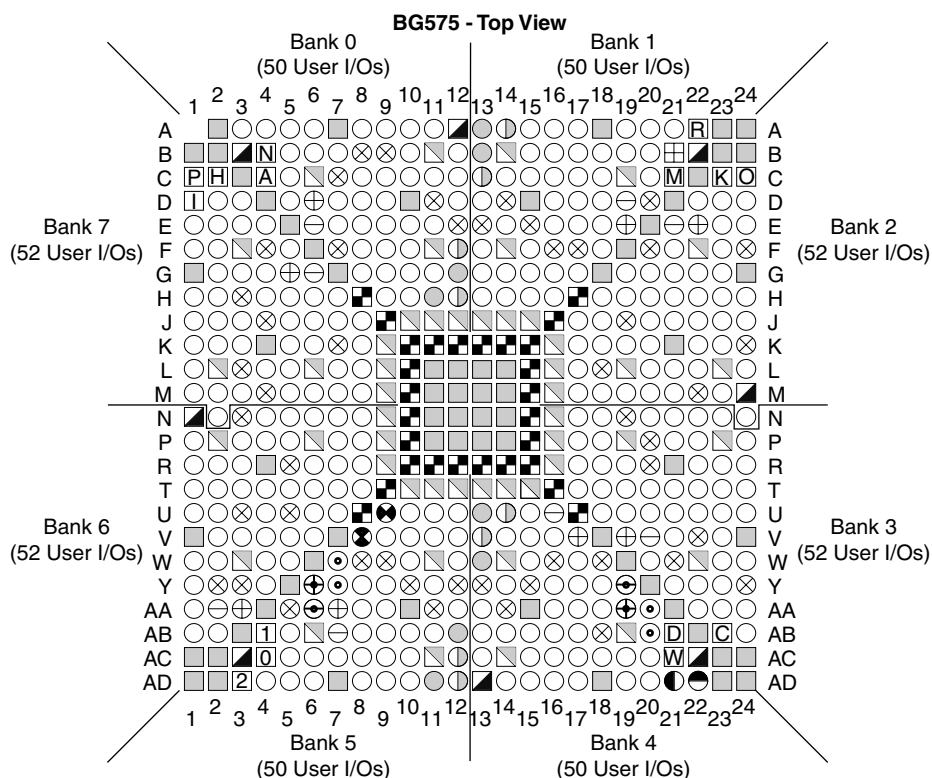
User I/O Pins	Dedicated Pins			
	C	CCLK	N	DXN
	P	PROG_B	A	DXP
	D	DONE	+	VBATT
	2 1 0	M2, M1, M0	R	RSVD
	H	HSWAP_EN	▲	VCCAUX
	K	TCK	■	VCCINT
	I	TDI	□	GND
	O	TDO	◻	NO CONNECT
	M	TMS		
	W	PWRDWN_B		

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Figure 4-10: FG676 Dedicated Pins



# BG575 Standard BGA Composite Pinout Diagram

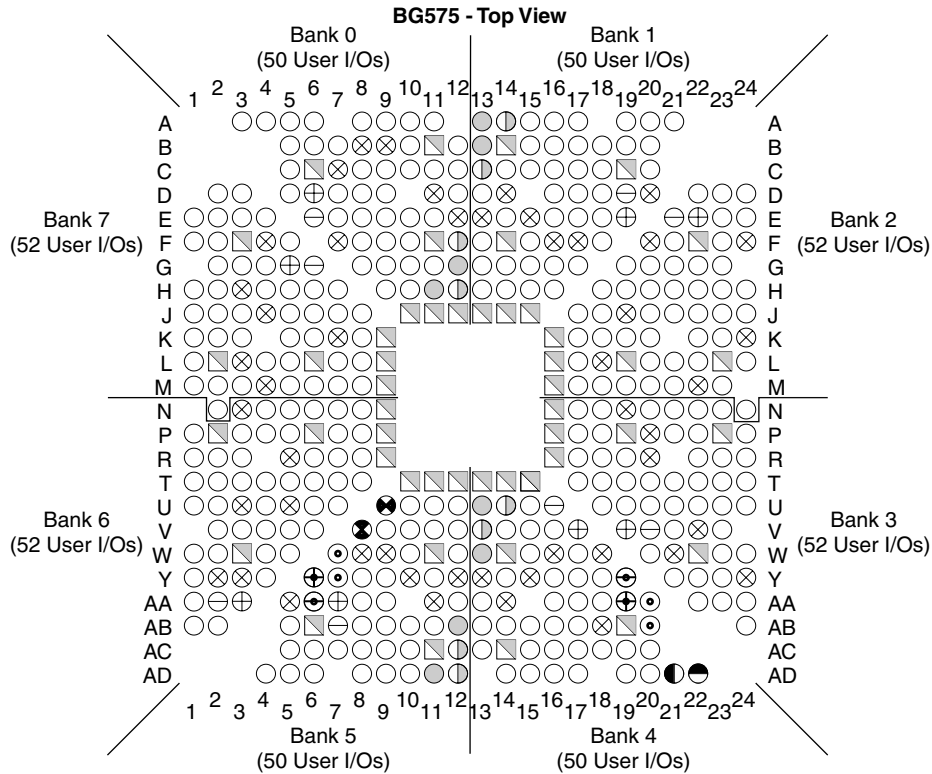


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	ⓐ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	ⓑ PROG_B	Ⓞ DXP
⊕ DIN/D0-D7	ⓓ DONE	Ⓢ VBATT
⊗ CS_B	Ⓜ2 Ⓜ1 Ⓜ0 M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	Ⓥ VCCO
⊗ BUSY/DOUT	Ⓚ TCK	Ⓦ VCCAUX
⊗ INIT_B	Ⓛ TDI	Ⓧ VCCINT
⊗ GCLKx (P)	Ⓞ TDO	Ⓧ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓨ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-11: BG575 Standard BGA Composite Pinout Diagram

## BG575 Bank Information



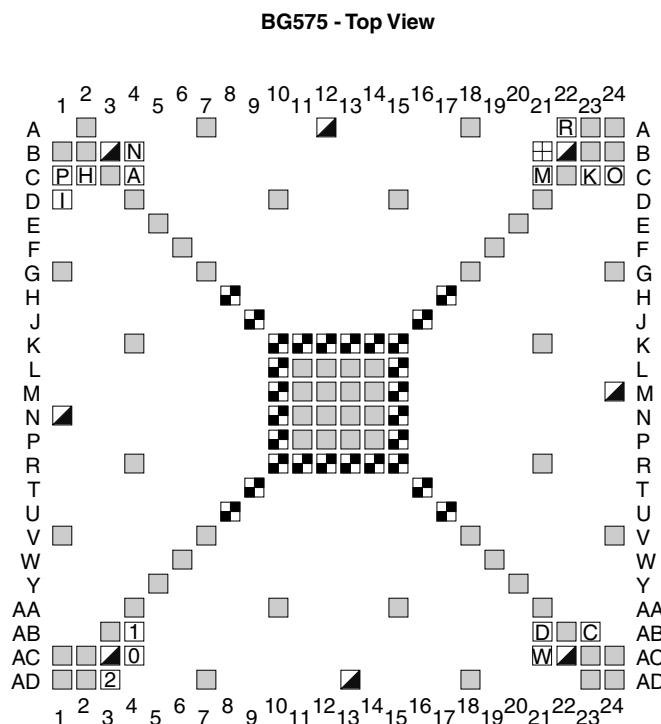
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-12: BG575 Bank Information



## BG575 Dedicated Pins



4

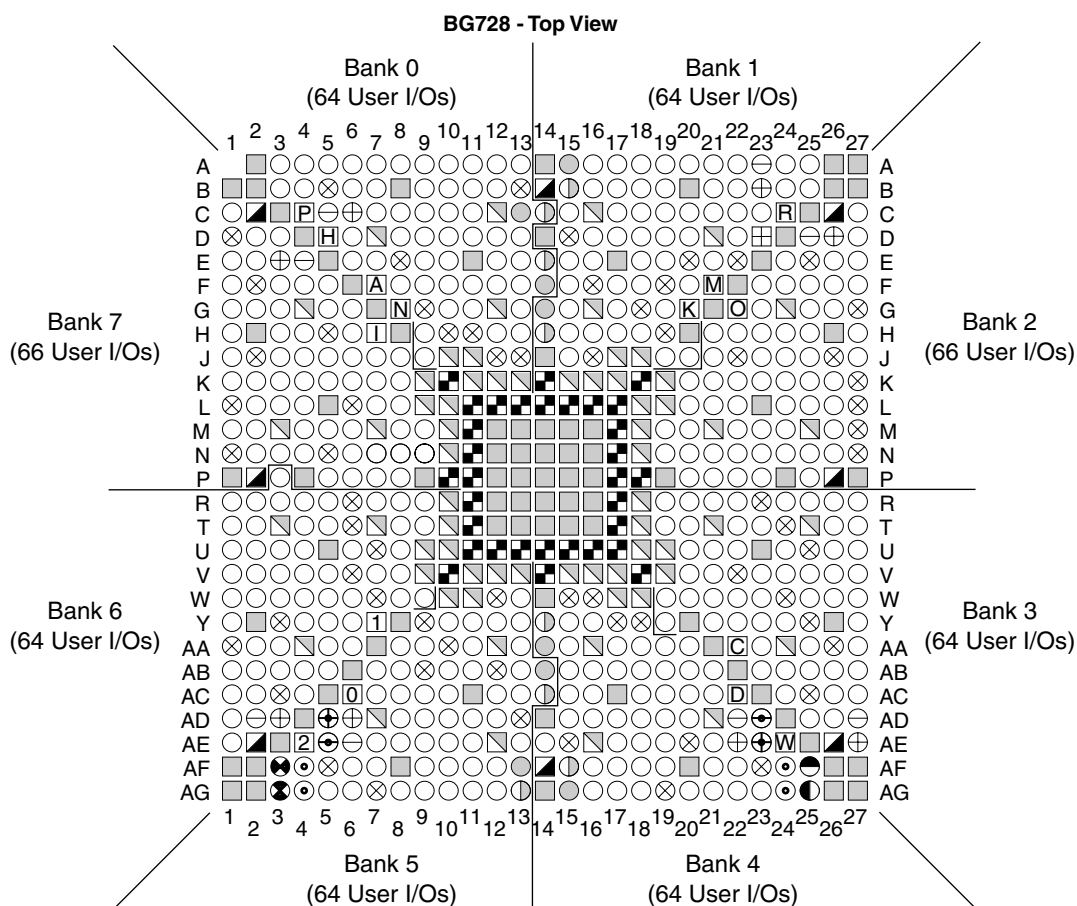
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">C</span> CCLK</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">P</span> PROG_B</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">D</span> DONE</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">2</span><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">1</span><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">0</span> M2, M1, M0</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">H</span> HSWAP_EN</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">K</span> TCK</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">I</span> TDI</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">O</span> TDO</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">M</span> TMS</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">W</span> PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">N</span> DXN</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">A</span> DXP</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">+</span> VBATT</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">R</span> RSVD</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">■</span> VCCAUX</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">■</span> VCCINT</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">□</span> GND</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">n</span> NO CONNECT</li> </ul>

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Figure 4-13: BG575 Dedicated Pins



# BG728 Standard BGA Composite Pinout Diagram



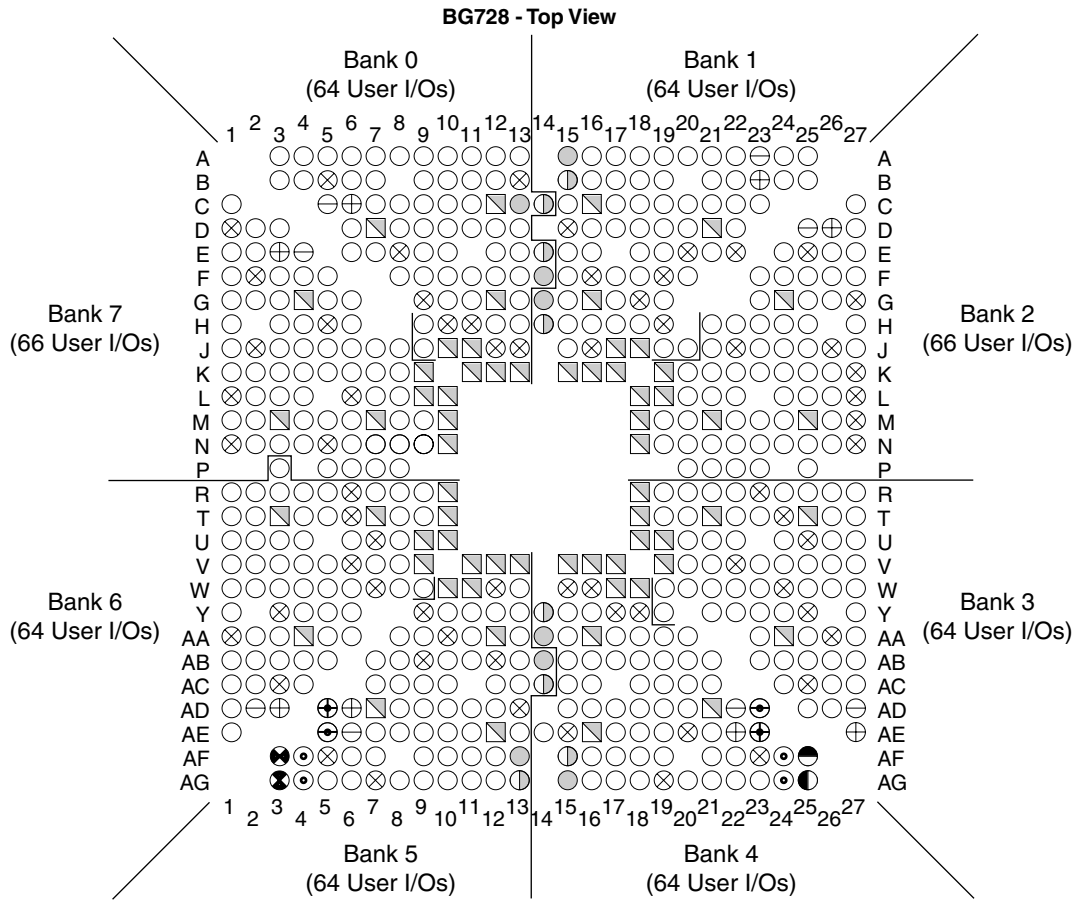
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	ⓐ DXP
⊙ DIN/D0-D7	ⓓ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	Ⓢ VCCO
⊗ BUSY/DOUT	Ⓚ TCK	Ⓛ VCCAUX
⊗ INIT_B	Ⓦ TDI	Ⓜ VCCINT
⊗ GCLKx (P)	Ⓞ TDO	Ⓛ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓝ NO CONNECT
⊗ VRP	Ⓦ PWRDWN_B	
⊗ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊗ D2, D4/ALT_VRP		
⊗ D3, D5/ALT_VRN		

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Figure 4-14: BG728 Standard BGA Composite Pinout Diagram

## BG728 Bank Information

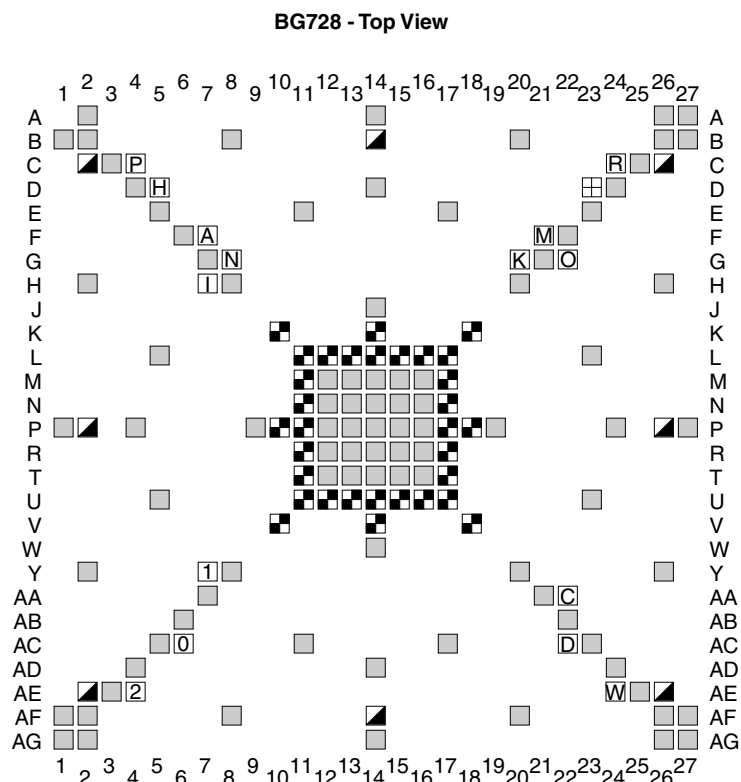


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<b>Dual-Purpose Pins:</b>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		◻ VCCO
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<b>Triple-Purpose Pins:</b>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-15: BG728 Bank Information

## BG728 Dedicated Pins



4

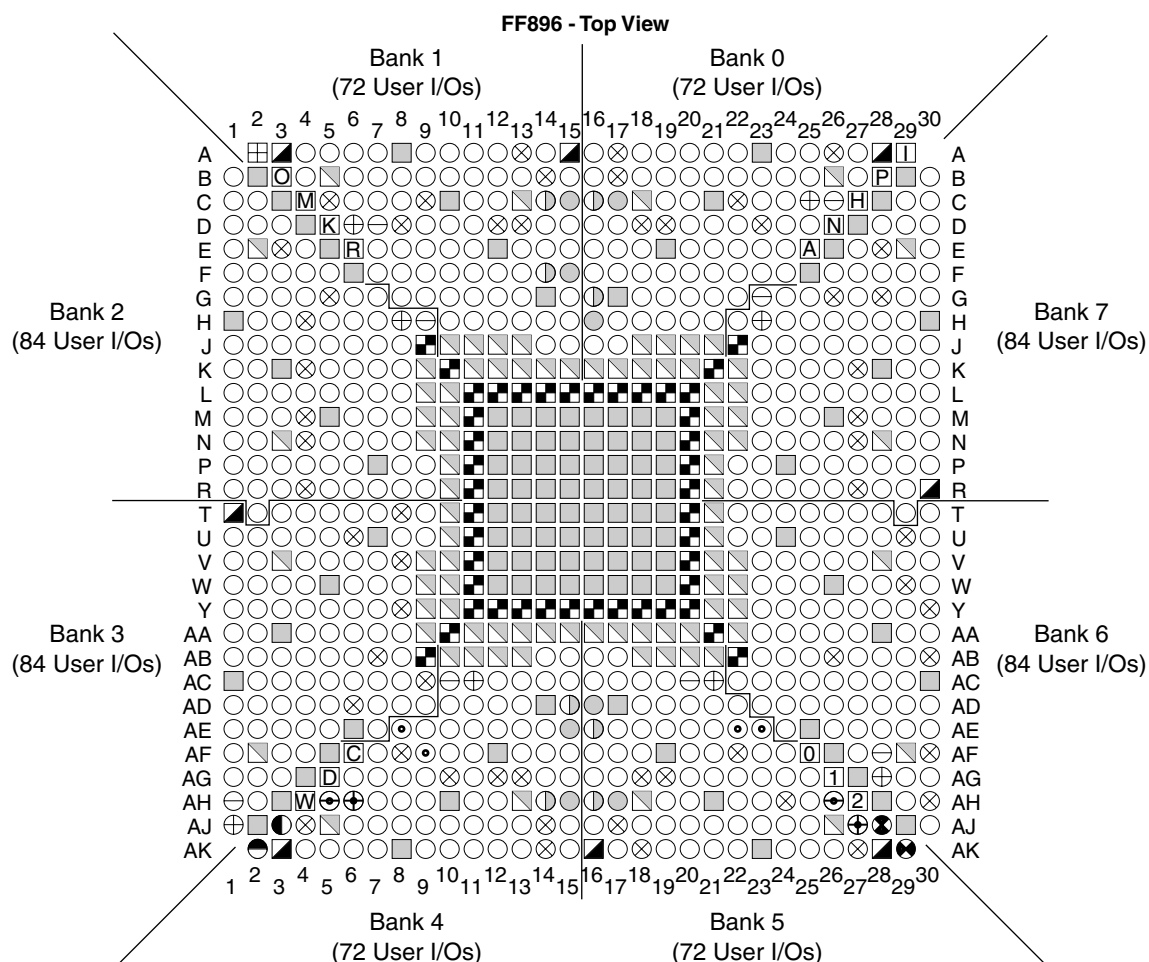
User I/O Pins	Dedicated Pins	
	<p>ⓐ CCLK</p> <p>Ⓟ PROG_B</p> <p>ⓓ DONE</p> <p>②①①① M2, M1, M0</p> <p>ⓗ HSWAP_EN</p> <p>Ⓚ TCK</p> <p>Ⓦ TDI</p> <p>Ⓞ TDO</p> <p>Ⓜ TMS</p> <p>Ⓦ PWRDWN_B</p>	<p>Ⓝ DXN</p> <p>Ⓐ DXP</p> <p>⊕ VBATT</p> <p>Ⓡ RSVD</p> <p>▴ VCCAUX</p> <p>▣ VCCINT</p> <p>■ GND</p> <p>Ⓝ NO CONNECT</p>

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Figure 4-16: BG728 Dedicated Pins



# FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram



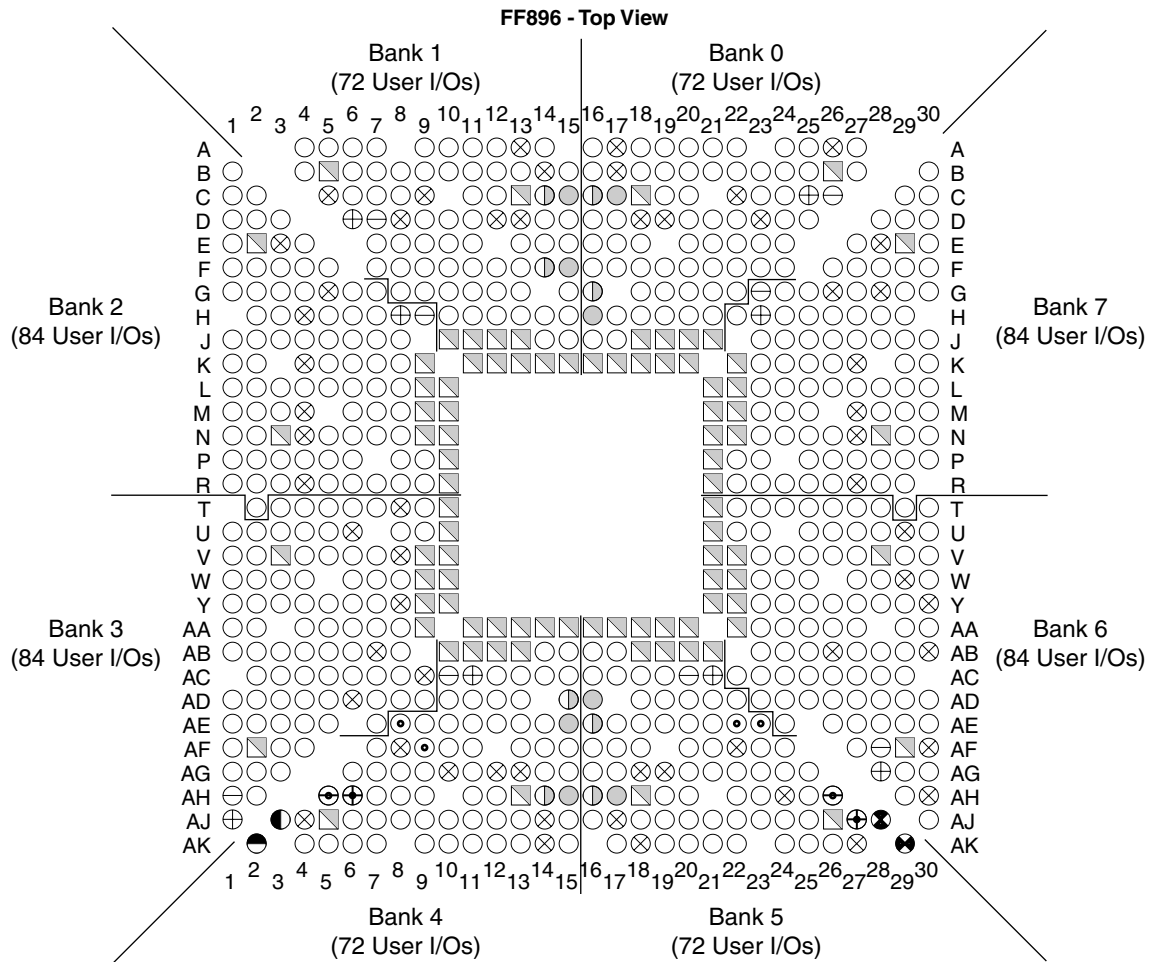
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓒ CCLK	⒩ DXN
<u>Dual-Purpose Pins:</u>	⒫ PROG_B	Ⓐ DXP
⊙ DIN/D0-D7	Ⓓ DONE	⊞ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓝ VCCO
● BUSY/DOUT	Ⓚ TCK	Ⓛ VCCAUX
● INIT_B	Ⓜ TDI	Ⓜ VCCINT
● GCLKx (P)	Ⓜ TDO	Ⓜ GND
Ⓜ GCLKx (S)	Ⓜ TMS	Ⓜ NO CONNECT
⊖ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2,D4/ALT_VRP		
⊕ D3,D5/ALT_VRN		

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Figure 4-17: FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

## FF896 Bank Information



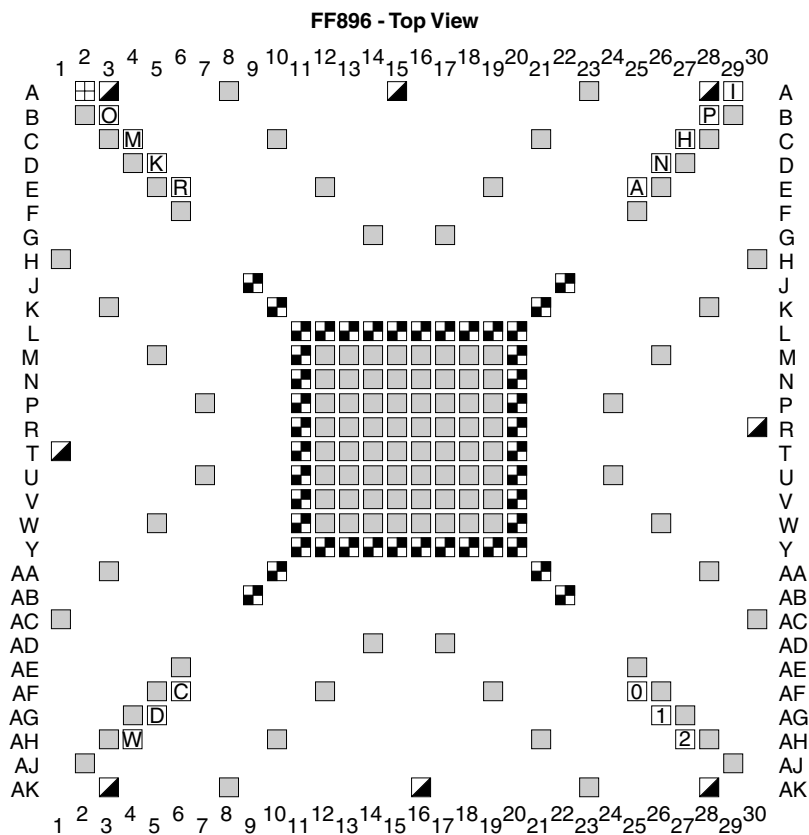
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<b>Dual-Purpose Pins:</b>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
● INIT_B		
○ GCLKx (P)		
○ GCLKx (S)		
⊖ VREF		
⊕ VRN		
⊗ VREF		
<b>Triple-Purpose Pins:</b>		
⊖ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-18: FF896 Bank Information



## FF896 Dedicated Pins



4

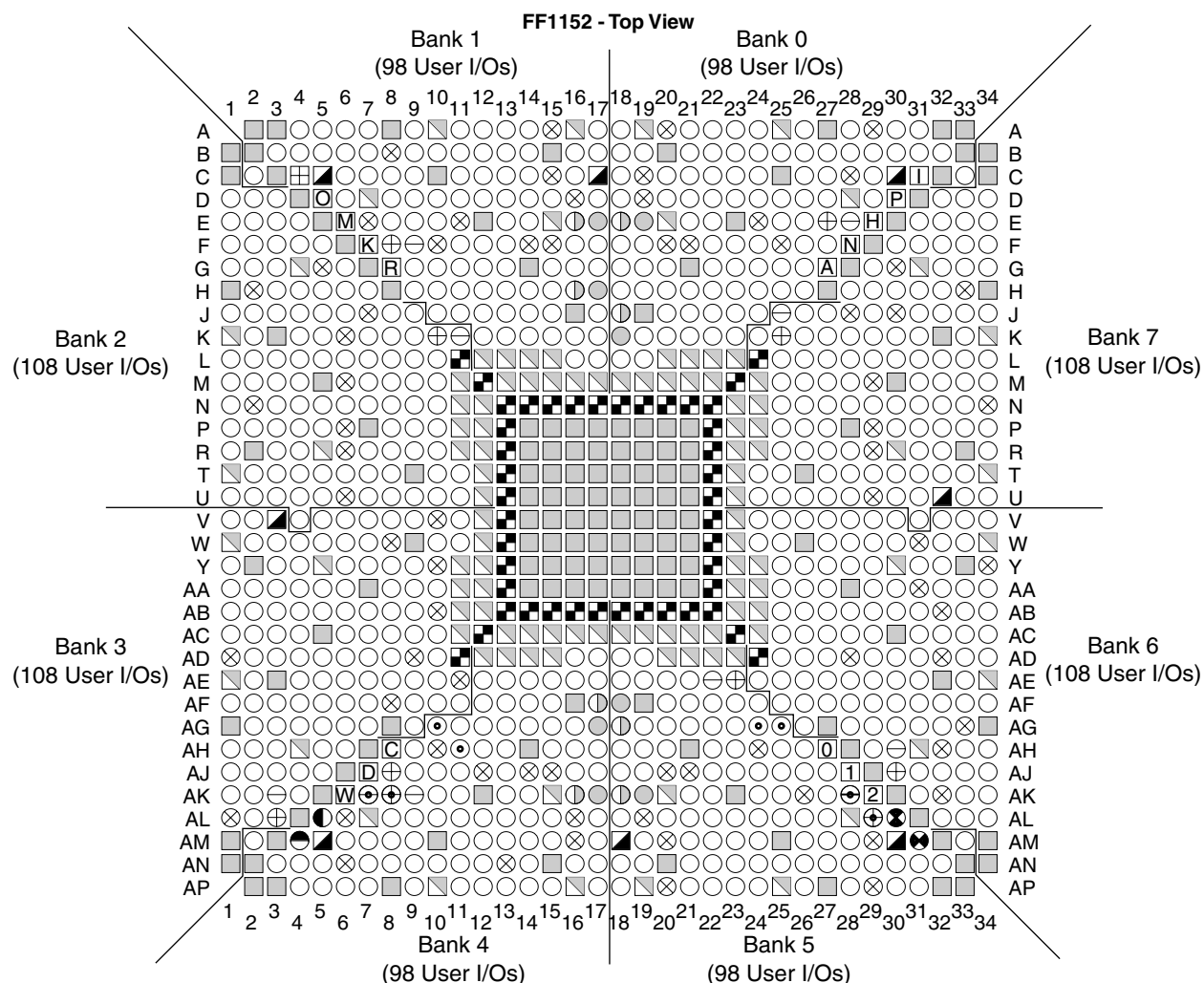
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">C</span> CCLK</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">P</span> PROG_B</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">D</span> DONE</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">2</span><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">1</span><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">0</span> M2, M1, M0</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">H</span> HSWAP_EN</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">K</span> TCK</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">I</span> TDI</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">O</span> TDO</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">M</span> TMS</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">W</span> PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">N</span> DXN</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">A</span> DXP</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">+</span> VBATT</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">R</span> RSVD</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">■</span> VCCAUX</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">■</span> VCCINT</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">■</span> GND</li> <li><span style="border: 1px solid black; border-radius: 50%; padding: 2px;">n</span> NO CONNECT</li> </ul>

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Figure 4-19: FF896 Dedicated Pins



# FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram



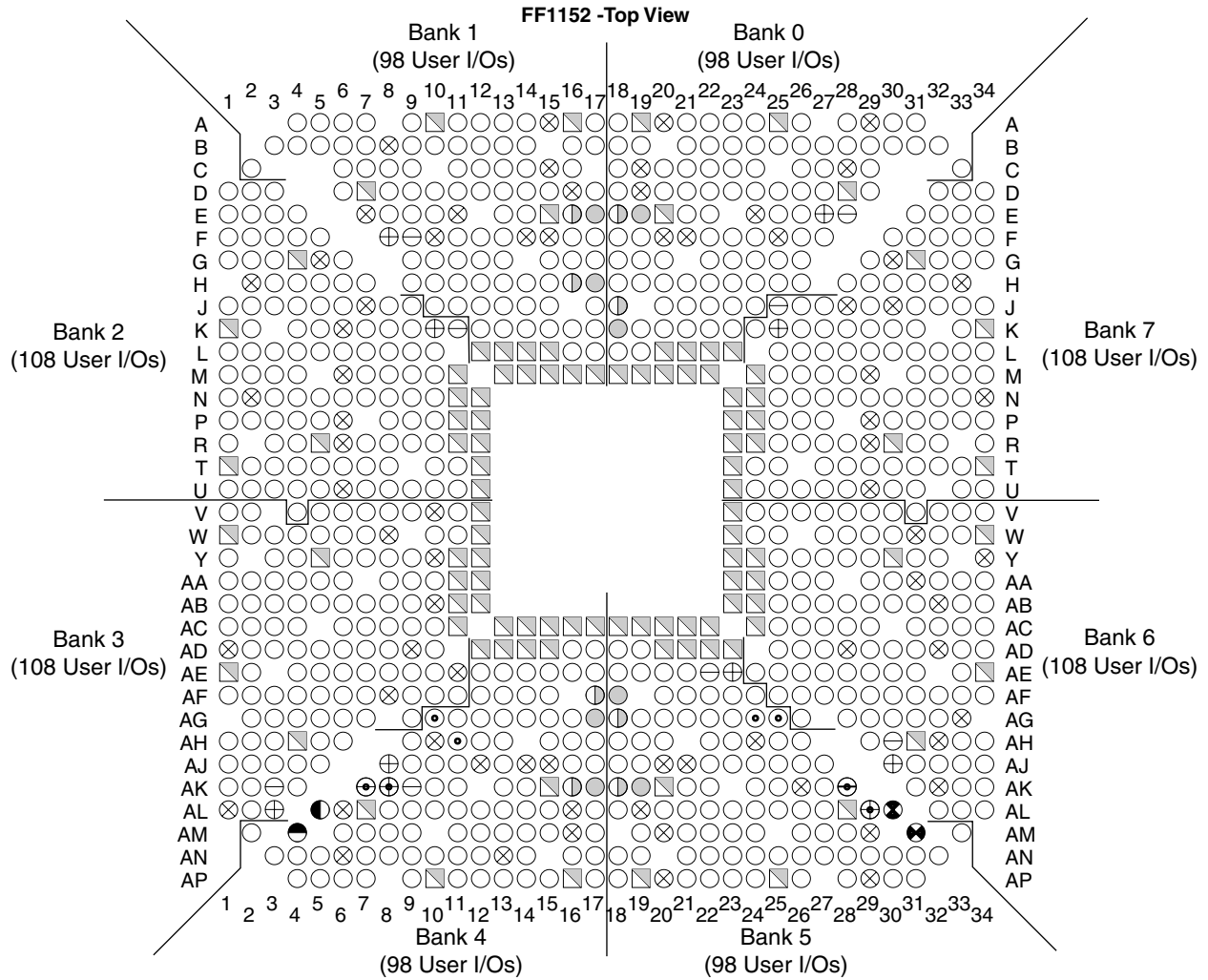
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊙ DIN/D0-D7	Ⓣ DONE	⊞ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓢ VCCO
⊙ BUSY/DOUT	Ⓚ TCK	Ⓢ VCCAUX
⊙ INIT_B	Ⓜ TDI	Ⓢ VCCINT
⊙ GCLKx (P)	Ⓜ TDO	Ⓢ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓢ NO CONNECT
⊖ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-20: FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

## FF1152 Bank Information

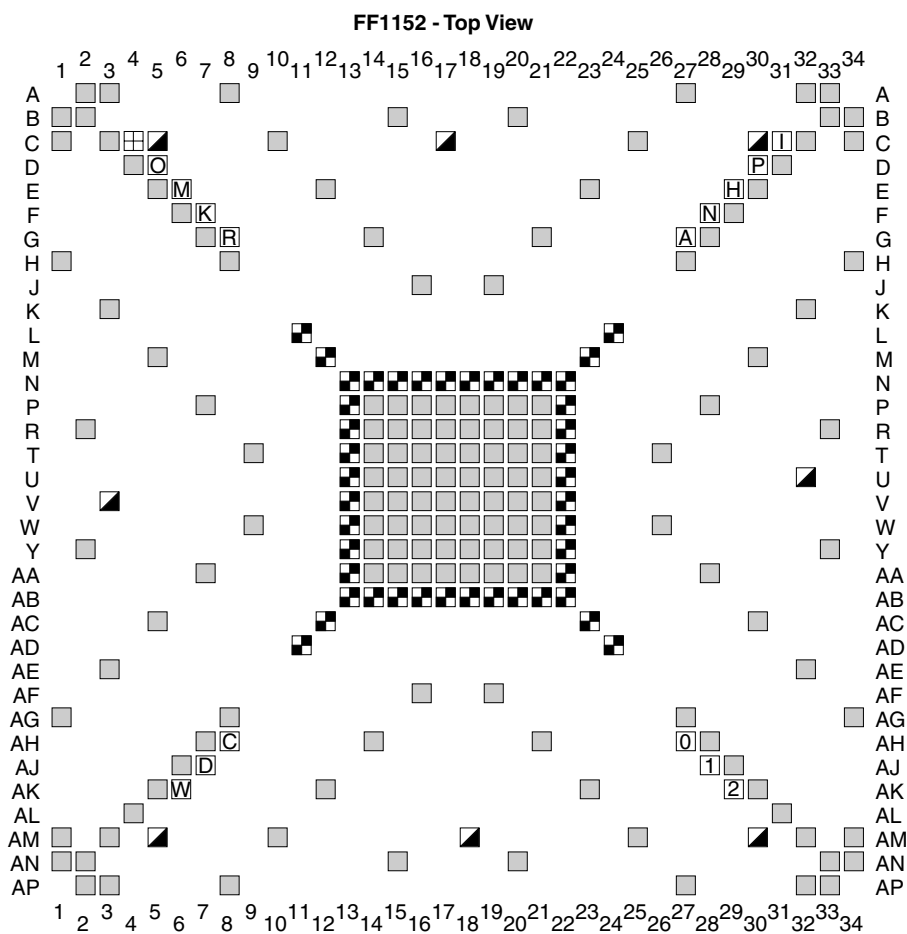


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▧ VCCO
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-21: FF1152 Bank Information

## FF1152 Dedicated Pins



4

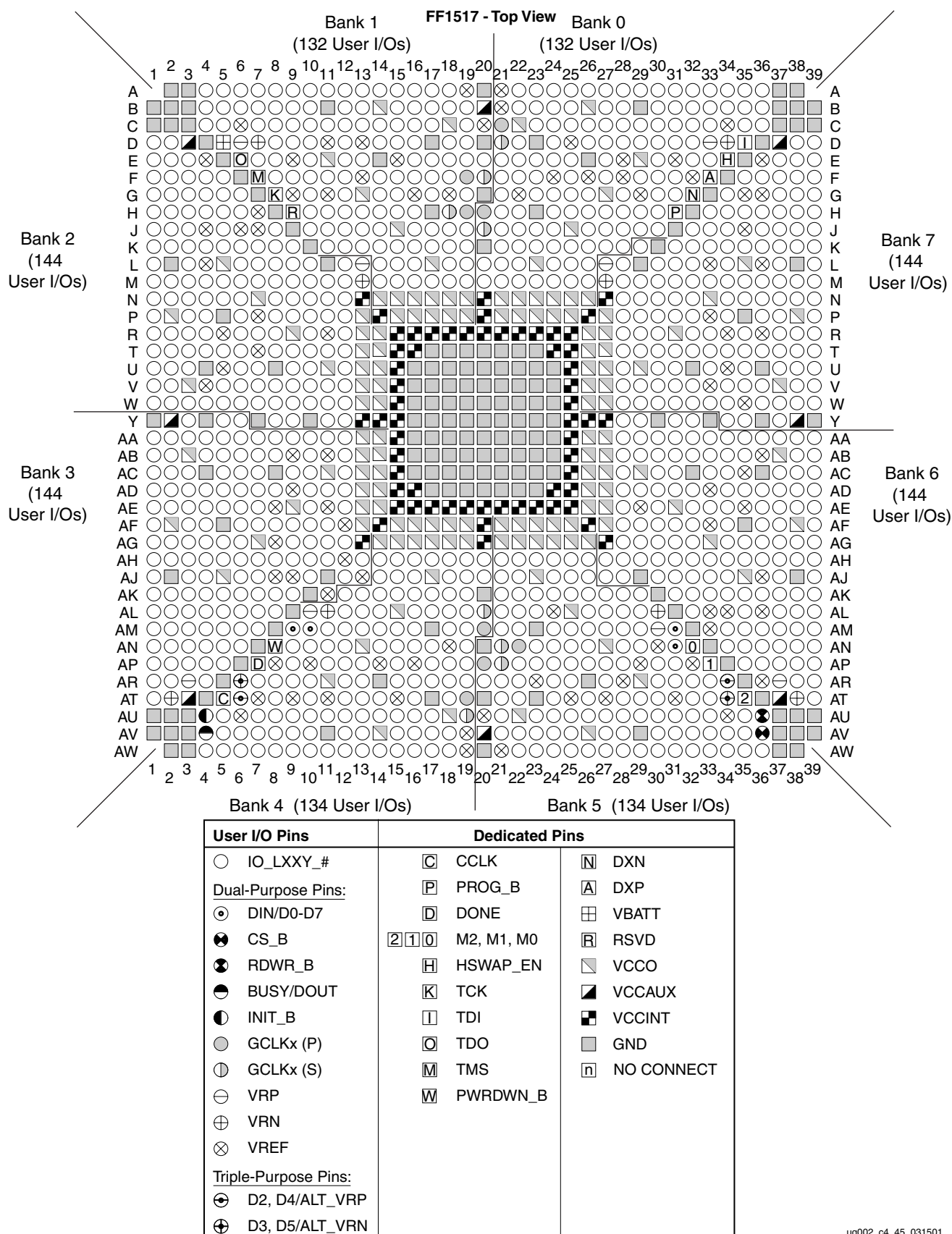
User I/O Pins	Dedicated Pins	
	Ⓢ CCLK	Ⓝ DXN
	Ⓟ PROG_B	Ⓐ DXP
	Ⓣ DONE	⊕ VBATT
	②①① M2, M1, M0	Ⓡ RSVD
	ⓗ HSWAP_EN	▣ VCCAUX
	Ⓚ TCK	▣ VCCINT
	Ⓦ TDI	■ GND
	Ⓞ TDO	□ NO CONNECT
	Ⓜ TMS	
	Ⓜ PWRDWN_B	

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Figure 4-22: FF1152 Dedicated Pins



# FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

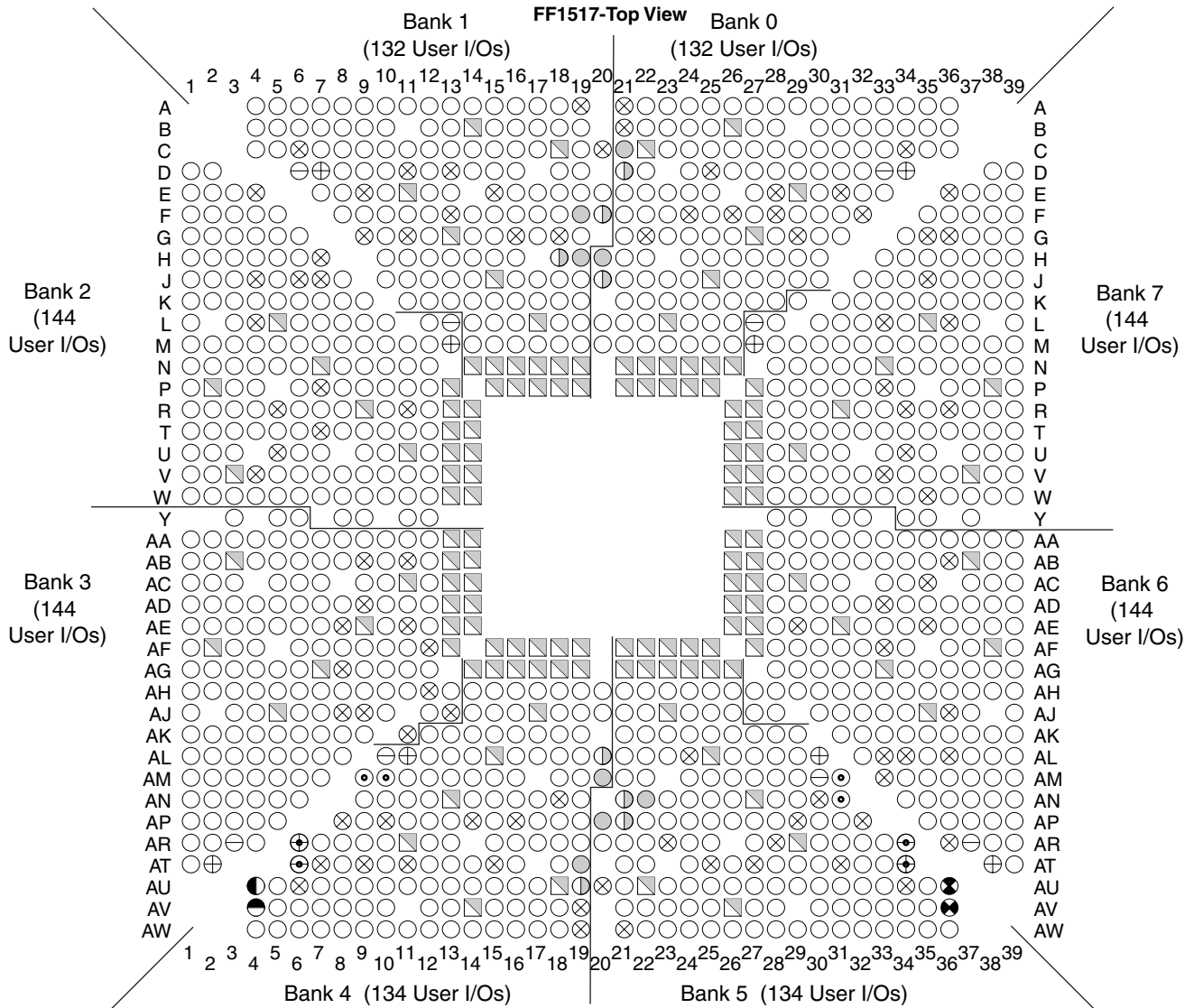


4

Figure 4-23: FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

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## FF1517 Bank Information



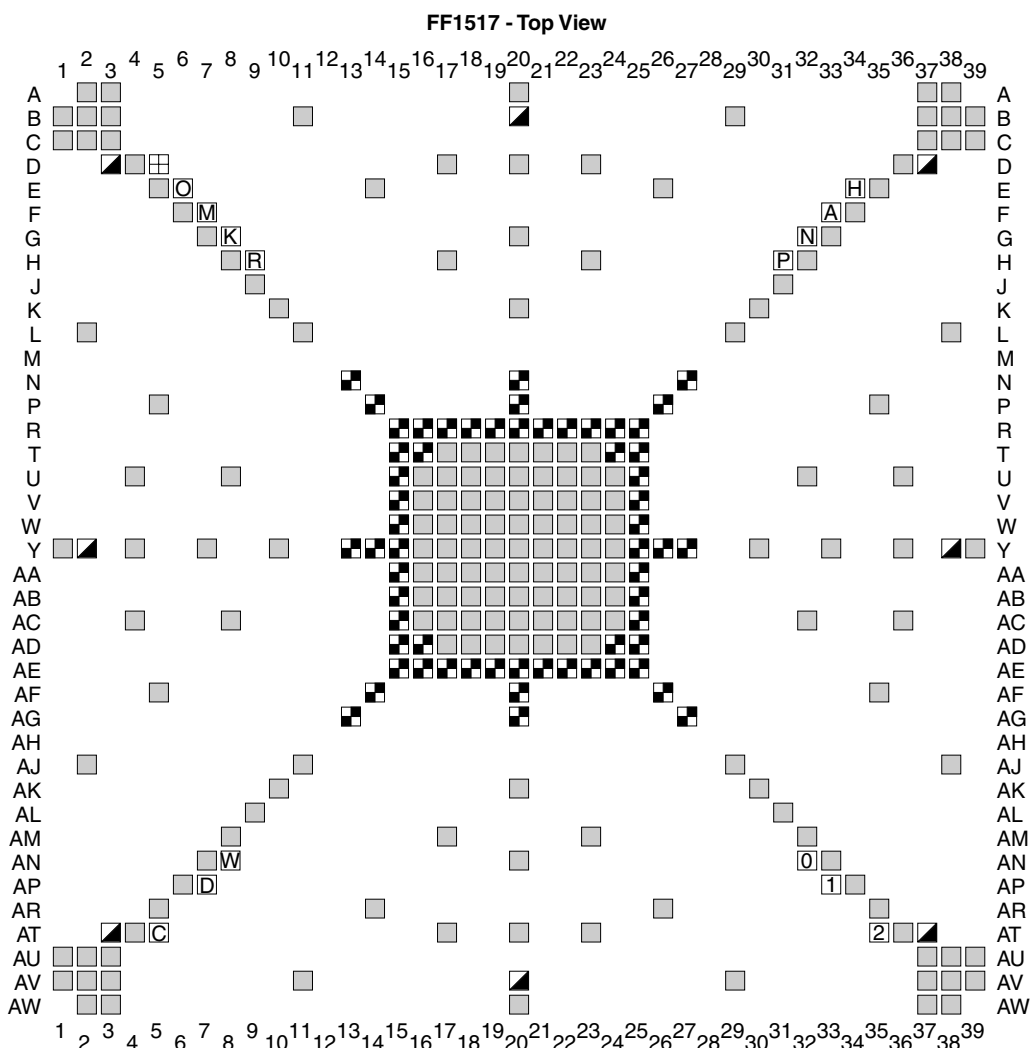
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<b>Dual-Purpose Pins:</b>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
⊖ BUSY/DOUT		
⊖ INIT_B		
⊙ GCLKx (P)		
⊙ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<b>Triple-Purpose Pins:</b>		
⊖ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-24: FF1517 Bank Information



## FF1517 Dedicated Pins



4

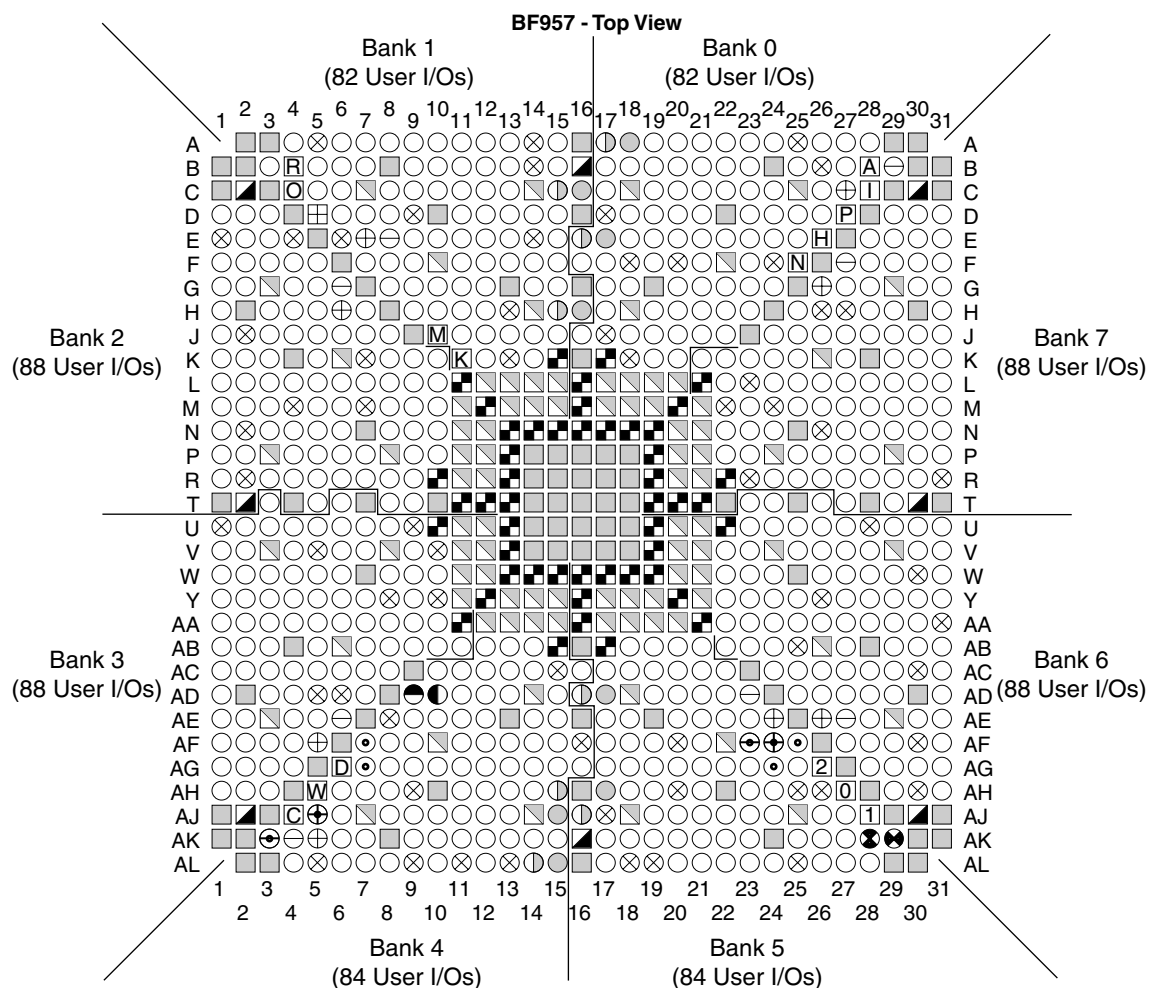
User I/O Pins	Dedicated Pins	
	ⓐ CCLK	Ⓝ DXN
	Ⓟ PROG_B	Ⓐ DXP
	ⓓ DONE	⊕ VBATT
	Ⓜ M2, M1, M0	Ⓡ RSVD
	ⓗ HSWAP_EN	⬛ VCCAUX
	Ⓚ TCK	⬜ VCCINT
	Ⓛ TDI	⬚ GND
	ⓐ TDO	Ⓝ NO CONNECT
	Ⓜ TMS	
	Ⓦ PWRDWN_B	

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Figure 4-25: FF1517 Dedicated Pins



# BF957 Flip-Chip BGA Composite Pinout Diagram



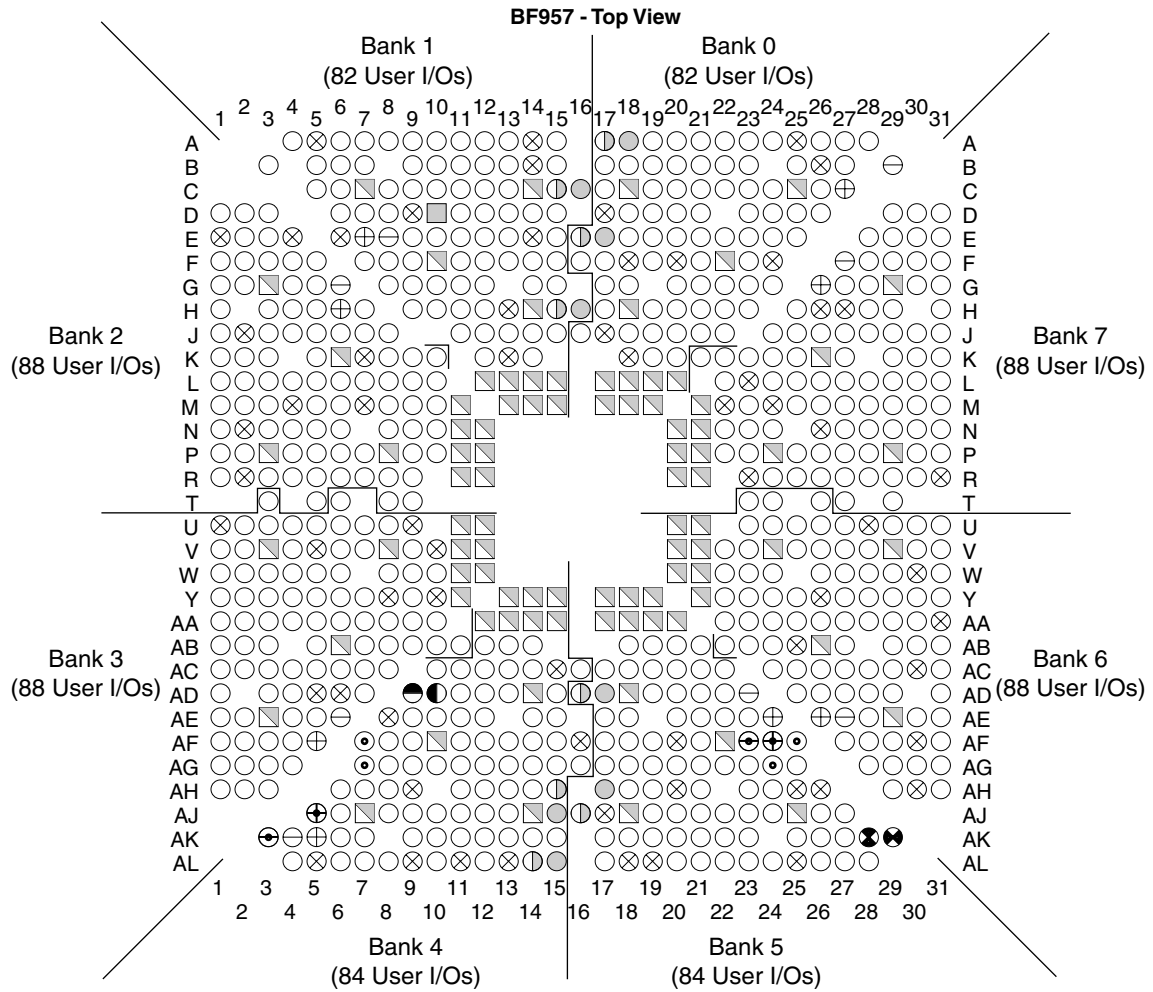
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊕ DIN/D0-D7	Ⓛ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓜ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓜ VCCO
⊖ BUSY/DOUT	Ⓜ TCK	Ⓜ VCCAUX
⊖ INIT_B	Ⓜ TDI	Ⓜ VCCINT
⊖ GCLKx (P)	Ⓜ TDO	Ⓜ GND
⊖ GCLKx (S)	Ⓜ TMS	Ⓜ NO CONNECT
⊖ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-26: BF957 Flip-Chip BGA Composite Pinout Diagram

## BF957 Bank Information

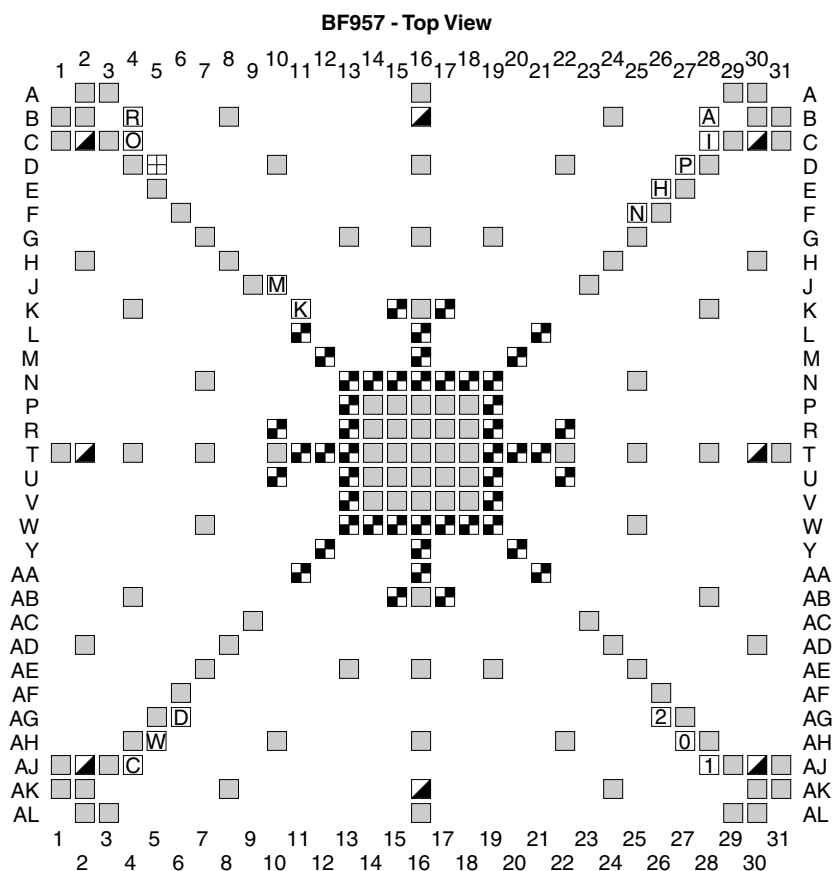


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
◐ INIT_B		
○ GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊖ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

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Figure 4-27: BF957 Bank Information

BF957 Dedicated Pins



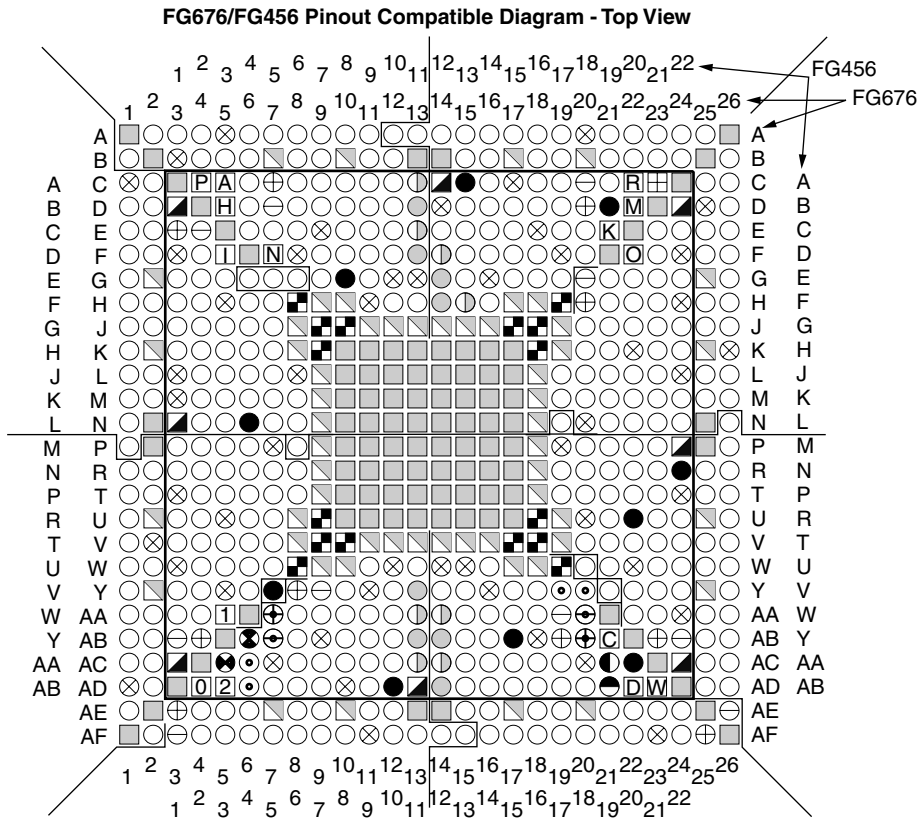
4

User I/O Pins	Dedicated Pins			
	C	CCLK	N	DXN
	P	PROG_B	A	DXP
	D	DONE	+	VBATT
	2 1 0	M2, M1, M0	R	RSVD
	H	HSWAP_EN	▀	VCCAUX
	K	TCK	■	VCCINT
	I	TDI	□	GND
	O	TDO	n	NO CONNECT
	M	TMS		
	W	PWRDWN_B		

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Figure 4-28: BF957 Dedicated Pins

# FG456 - FG676 Pinout Compatibility Diagram



**Note:** FG456 and FG676 are pinout compatible with the exception of the LVDS pairs. I/O VREF pins in FG676 are user I/O pins in FG456. In addition, some user I/O pins are not in the same bank (see lines). VRP (V7) and VRN (V6) in Bank 5 and VRP (W17) and VRN (Y17) in Bank 4 are only user I/Os in FG676.

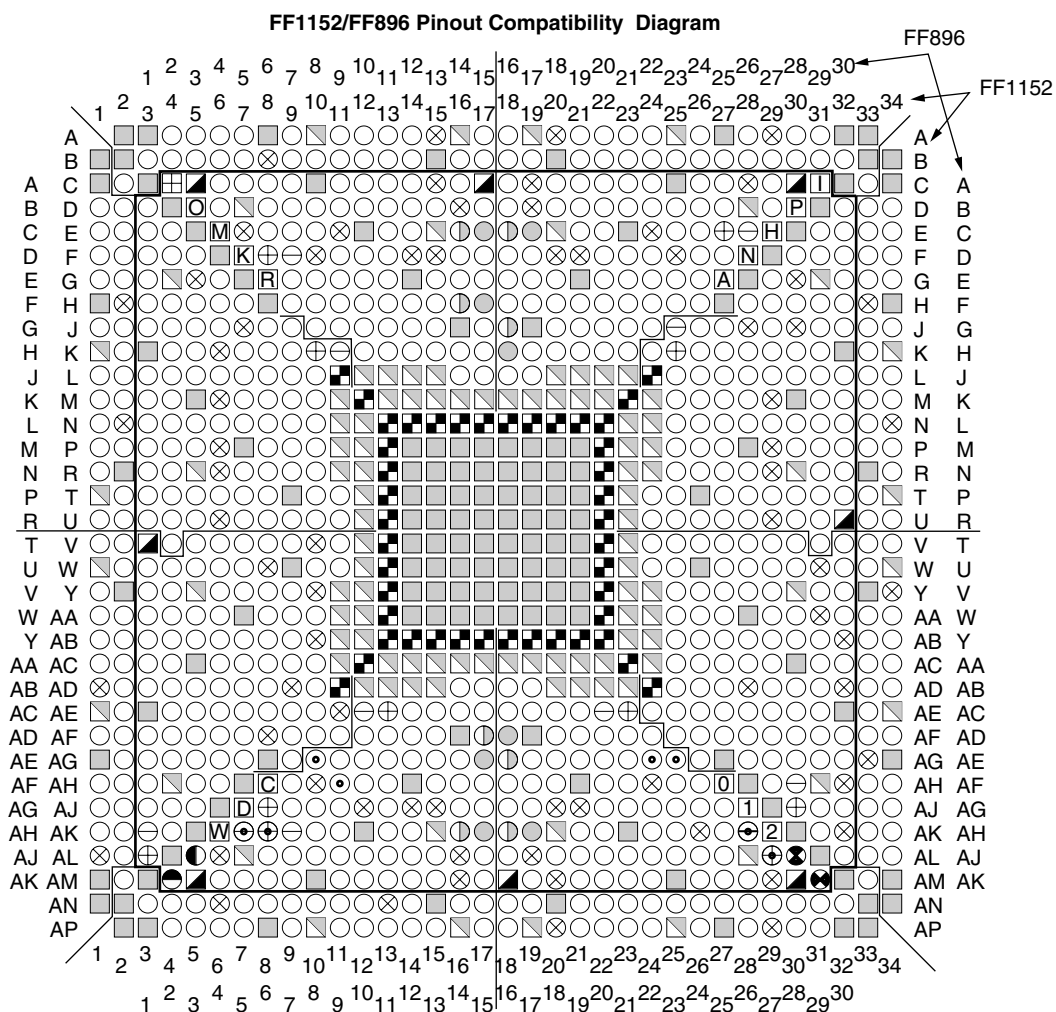
User I/O Pins	Dedicated Pins	
IO_LXXY_#	CCLK	DXN
<b>Dual-Purpose Pins:</b>	PROG_B	DXP
DIN/D0-D7	DONE	VBATT
CS_B	M2, M1, M0	RSVD
RDWR_B	HSWAP_EN	VCCO
BUSY/DOUT	TCK	VCCAUX
INIT_B	TDI	VCCINT
GCLKx (P)	TDO	GND
GCLKx (S)	TMS	NO CONNECT
VRP	PWRDWN_B	
VRN		
VREF		
VREF on FG676 User I/O on FG456		
<b>Triple-Purpose Pins:</b>		
D2, D4/ALT_VRP		
D3, D5/ALT_VRN		

Corresponding Pinouts	
FG456	FG676
A1	C3
.	.
.	.
.	.
.	.
AB22	AD24

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Figure 4-29: FG456 - FG676 Pinout Compatibility Diagram

# FF896 - FF1152 Pinout Compatibility Diagram



4

**Note:** FF896 is pinout compatible with the FF1152 except for LVDS pairs. Also, in Bank 4, VRP/VRN pins are not compatible: for FF896, VRP is in AC10 and VRN is in AC11, and for FF1152, VRP is in AK9 and VRN is in AJ8. If DCI is not used in Bank 4, or is used with ALT\_VRP or ALT\_VRN, then the user I/Os are compatible.

User I/O Pins	Dedicated Pins	
○ IO_LXYY_#	ⓐ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	ⓐ DXP
⊙ DIN/D0-D7	ⓓ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	Ⓢ VCCO
⊙ BUSY/DOUT	Ⓚ TCK	Ⓢ VCCAUX
⊙ INIT_B	Ⓦ TDI	Ⓢ VCCINT
⊙ GCLKx (P)	Ⓞ TDO	Ⓢ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓢ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

### Corresponding Pinouts

FF896	FF1152
A2	C4
.	.
.	.
.	.
.	.
AK29	AM31

ug002\_c4\_55\_032901

Figure 4-30: FF896 - FF1152 Pinout Compatibility Diagram