About This Handbook

This document describes the function and operation of Virtex-II devices and also includes information on FPGA configuration techniques and PCB design considerations. For Virtex-II device specifications, refer to the Virtex-II **Data Sheet** in Part I of this handbook.

For details on the following topics, see the Virtex-II *Platform FPGA User Guide* in Part II of this handbook:

- Chapter 1: Timing Models
- Chapter 2: Design Considerations
- Chapter 3: Configuration
- Chapter 4: PCB Design Considerations
- Appendix A: Application Notes
- Appendix B: BitGen and PROMGen Switches and Options
- Appendix C: XC18V00 Series PROMs
- Appendix D: Glossary

Additional Resources

The following table lists URLs for resources available on the web. For additional information, go to **http://www.xilinx.com**.

Resource	Description/URL
Handbook	This site contains the latest *Virtex-II User Guide* and *Virtex-II Data Sheet*: **http://www.xilinx.com/products/virtex/handbook/**
Application Notes	This site contains device-specific design techniques and approaches: **http://www.xilinx.com/apps/appsweb.htm**
Data Book	*The Programmable Logic Data Book* describes device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging: **http://www.xilinx.com/partinfo/databook.htm**
Xcell Journals	This site contains quarterly journals for Xilinx programmable logic users: **http://www.xilinx.com/xcell/xcell.htm**
Tech Tips	See this site for the latest news, design tips, and patch information on the Xilinx design environment: **http://www.xilinx.com/support/techsup/journals/index.htm**
Answers Database	This database provides a current listing of solution records for Xilinx software tools. Search this database using the search function at: **http://www.xilinx.com/support/searchtd.htm**

Typographical Conventions

The following typographical conventions are used in this manual:

- Red text indicates a cross-reference to information within this document. Click red text to open the specified cross-reference.
- **Blue-underlined text** indicates a link to a Web page. Click blue-underlined text to browse the specified Web site.
- `Courier font` indicates prompts or program outputs displayed by the system.

  `speed grade: 5`
- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  Courier bold also indicates menu commands: **`File`** → **`Open`**
- *Italic font* denotes the following items:
  - Variables that are substituted with user-defined values

    `edif2ngd` *`design_name`*
  - References to other documents.

    See the *Libraries Guide* for more information.
  - Emphasis in text

    If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  `edif2ngd` [*option_name*] *design_name*
- Braces "{ }" enclose a list of items from which you must choose one or more, and a vertical bar " | " separates items in a list of choices:

  `lowpwr =`{**`on`** | **`off`**}
- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
IOB #2: Name = CLKIN'
.
.
.
```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2 . . . locn;*