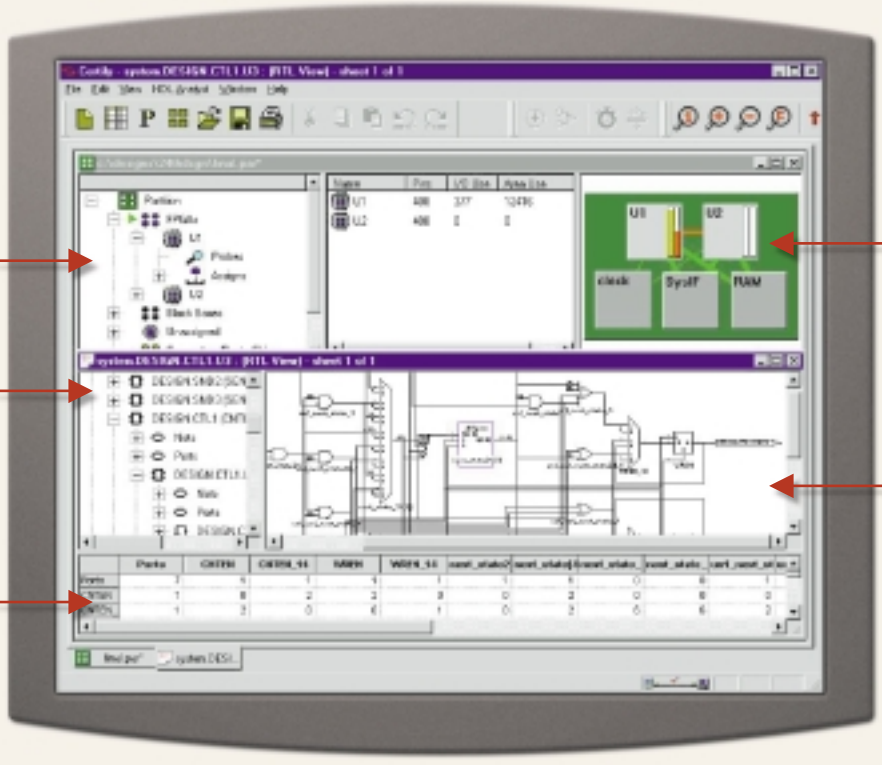
Certify™

ASIC Hardware Prototypes Directly from RTL Code



Info View: instant access to all prototype-level design information

HDL Analyst® RTL Browser: transverse levels of hierarchy rapidly to decide where the ASIC logic belongs in the prototype board

Connectivity Matrix: gain quick and clean understanding of connectivity between functional blocks

Partition View: drag-and-drop logic from your ASIC to make partitioning decisions

HDL Analyst RTL Viewer: transform RTL code into a schematic to view all levels of the design

It makes perfect sense. Early and rapid prototyping can accelerate the first-pass success of complex ASICs. Unfortunately, traditional ASIC prototyping techniques have proven to be difficult, cumbersome and time consuming. Certify has changed all that. It's a tool as robust as it is easy to use. In fact, Certify features one of the most intuitive, information-focused, and user-friendly interfaces of any ASIC design tool. At the same time, it's a sophisticated tool developed to quickly and consistently deliver ASIC designers the highest Quality of Results (QoR).

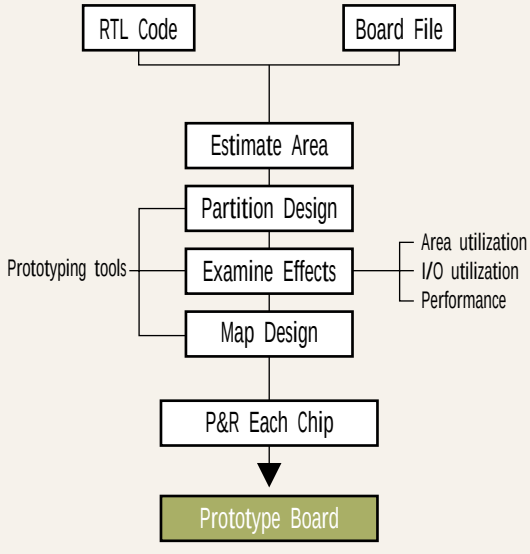
Getting to know Certify

- First and only synthesis product targeting ASIC prototyping and verification using multiple FPGAs
- Combines RTL multi-chip partitioning with best-in-class FPGA synthesis
- Makes ASIC prototyping significantly easier
- Shortens prototype development time
- Improves prototype performance
- Enables faster time to market
- Typical prototype speed between 10-60 MHz

Certify Features	Benefits
Best-in-Class FPGA Synthesis	Optimal speed and efficiency of prototype.
Partition-Driven Synthesis	Manages time budgets across FPGAs.
RTL Partitioning	Partition RTL code, not gate-level netlist, for full verification prior to synthesis.
Prototyping Tools to Guide User	Shortens time to prototype.
Fast, Accurate Feedback on I/O and Area Utilization	Reduces iterations between partitioning and layout.
Multi-Million Gate Capacity	No need to break up design into many small blocks.
Manages Logic Replication	Optimal ASIC prototype without changing ASIC source code.
Manages Probe Point Creation	High observability for debugging without changing source.
Optimized for Iterative Design	Reduces time to fix errors.
Understands Characteristics of Prototype Board	Optimal speed and efficiency of prototype.
Supports Popular FPGA Vendors	Flexibility in implementation choice.
Impact Analysis	Instantly evaluate partitioning decisions.

Rapid RTL prototyping with multiple FPGAs

Certify dramatically increases the productivity of designers building ASIC prototypes using FPGAs. Certify provides optimization capabilities designed to get the maximum efficiency and speed from the prototype. Automatic timing analysis across multiple FPGAs is built into Certify, enabling simultaneous partitioning and optimization of a design spanning multiple FPGAs. Only Certify has the capacity to take a million-plus gate ASIC RTL and synthesize it directly into multiple FPGAs, without requiring changes to the RTL source code, and without requiring the user to break up the design into many small blocks just for synthesis.



Combining synthesis and partitioning

In the traditional flow for building prototypes using multiple FPGAs, synthesis and partitioning are separate steps in the flow. Synthesis is performed without understanding the partition. This leads to sub-optimal optimization decisions. Also, partitioning into multiple FPGAs is done without any feedback from the synthesis engine about the impact of partitioning decisions on the speed and routability of the prototype. As a result, designers must make several time-consuming iterations between synthesis and partitioning to arrive at a solution. In addition, it's extremely difficult to achieve a legal partition running at near real-time speeds.

Certify combines synthesis and partitioning into one tool, eliminating the need for iterations, thus reducing the time required to build a prototype. Automatic timing analysis across multiple FPGAs enables a prototype to be built that runs at near real-time speeds. Certify shortens prototype development time, improves prototype performance, and enables faster time to market.

Certify Prototyping Tools	
• Automatic pin assignment	• Feedthrough optimization
• Certify Pin Multiplier	• Constant propagation
• Fan-in driven MUX decomposition	• Bit slicing of large primitives
• Logic replication	• Zippering

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