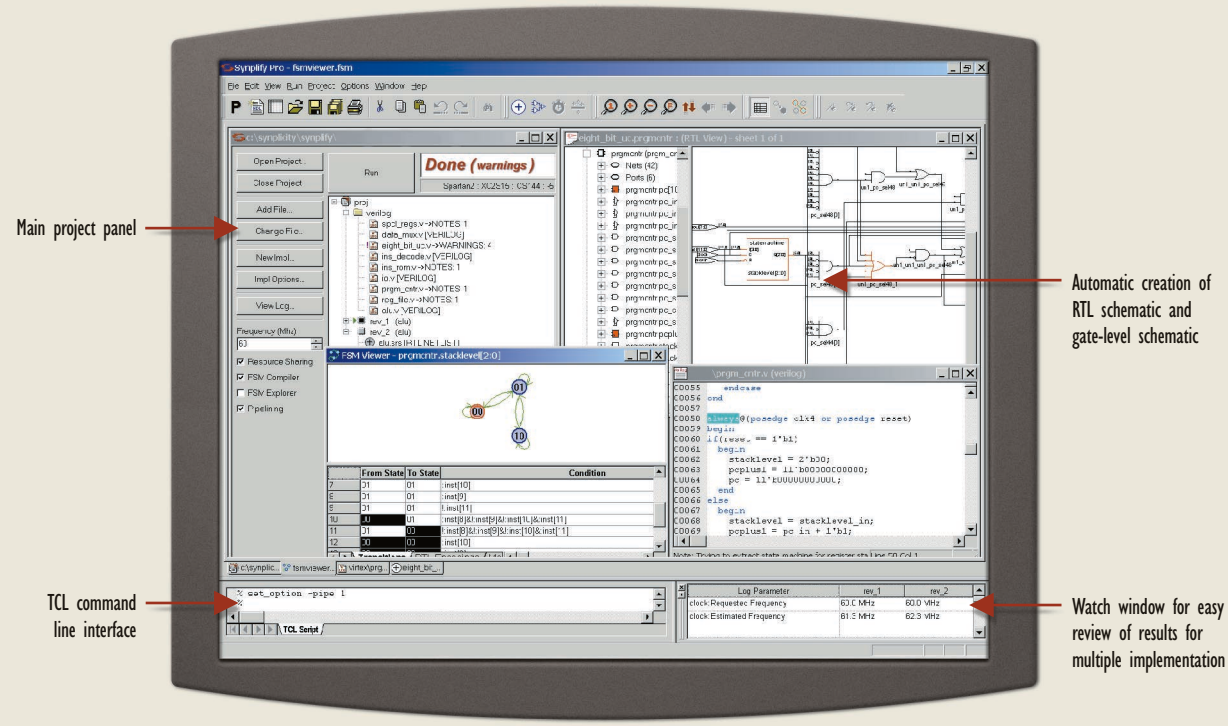
Synplify Pro™

Advanced FPGA-Synthesis Solution for Multi-Million Gate Programmable Logic Designs



High-end FPGAs and FPGA synthesis

As system complexities advance, the complexity of programmable logic is following suit. High-density field programmable gate arrays (FPGAs) now contain millions of gates and operate at speeds in excess of 100 MHz. At this level of complexity, schedules, budgets and FPGA design tools all begin to feel the burden. Enter the Synplify Pro solution that starts with all the features that made the Synplify® product the industry's most popular and robust synthesis tool, and moves beyond by providing additional capabilities. By using the Synplify Pro solution, you can push the performance of multi-million gate designs while remaining comfortably on or ahead of schedule.

The Synplify Pro software addresses the unique requirements of multi-million gate programmable IC projects. Where advanced project management features are required, such as controlling various implementations of a design, the Synplify Pro tool accommodates incremental design techniques, the integration of intellectual property (IP) and design re-use.

New features in the Synplify Pro solution:

- A powerful new graphical user interface displays multiple implementations including a project browser, a new command line interface with an expanded TCL command set, a log watch window that displays the results of synthesis for multiple implementations simultaneously, plus batch mode operation. In addition to all of the features of the Synplify FPGA synthesis solution, the Synplify Pro product adds:
- FSM Explorer with state diagram viewer and cross-probing
- Register balancing for pipelined multipliers and ROMs
- Probe point extraction for test and debugging
- Cross-probing to the HDL Analyst® RTL analysis and debugging environment from 3rd party text files such as timing reports
- Complex project management capabilities for managing multiple implementations

Features	Benefits
Proprietary B.E.S.T.™ Algorithms	Produces globally optimized designs in a fraction of the time required by traditional synthesis tools.
Integrated Module Generation and Mapping	Higher performing, area-efficient implementations of arithmetic/datapath functions.
Lightning-Fast Compile Times	Synthesizes even the largest design in minutes.
SCOPE® Multi-Level Design Constraints	Provides designer with complete control over the synthesis process.
Comprehensive Language Support	Verilog: IEEE 1364-1995 compliant. VHDL: IEEE 1076-1993, IEEE 1164.
Language-Sensitive Editor	Automatic HDL syntax and synthesis checks for both Verilog and VHDL.
Intuitive Use Model w/ Intelligent Defaults	Be instantly productive with the tools.
Direct Synthesis Technology™ (DST™)	Leverages architecture-specific features to deliver the highest Quality of Results.
Automatic RAM Inferencing	Bypasses tedious hand instantiation of RAM.
Third-Party Tool Integration	Cross-probing with popular simulators and design entry tools.
FSM Explorer	Automatically finds and selects the best coding style option for the fastest performance.
Graphical State Machine Viewer	Fast debugging and documentation for all state machines in your design.
Register Balancing for Pipelined Multipliers and ROMs	Automatic pipelining provides better throughput and faster circuit performance.
Probe Point Creation	Allows any signal to be tied to an external pin for testing without HDL code changes.
Generic Cross-Probing of Critical Paths	Cross-probe between the HDL Analyst tool and 3rd-party timing reports.
HDL Analyst RTL Analysis & Debugging Tool	Instantly generates an RTL block diagram from HDL code; helps identify critical paths.

The Synplify Pro advanced-FPGA solution

This product delivers unmatched circuit performance with the most efficient area utilization for million-gate-plus designs. Like the Synplify product, Synplify Pro synthesis software is driven by Synplicity's proprietary Behavior Extraction Synthesis Technology® (B.E.S.T.), and also includes the Synthesis Constraint Optimization Environment® (SCOPE) multi-level, graphical constraints editor.

Standard with the Synplify Pro product is the powerful, easy-to-use HDL Analyst RTL graphical analysis and debugging tool. Providing an instant graphical view of both high-level block diagrams and gate-level schematics linking back to the HDL source code, the HDL Analyst product is an easier, faster way to debug and optimize high-density, HDL-based programmable logic.

FSM Explorer

One of several impressive new features of the Synplify Pro solution is the FSM Explorer, an enhancement to the Synplify product's unique finite state machine (FSM) compiler. FSM Explorer automatically finds state machines, then runs through many coding styles and selects the one that gives the best performance for the design. FSMs are displayed as bubble diagrams, providing an easy-to-read graphical representation of your results. This graphical view is especially useful for design debugging and documentation.

Pipelining

To dramatically increase performance with arithmetic operations, the Synplify Pro product has register balancing for multipliers and ROMs.

The Amplify™ Physical Optimizer™

When your highest priority is the fastest performance possible from your programmable logic, the Amplify Physical Optimizer is an option available with the Synplify Pro product. The Amplify Physical Optimizer is the first and only physical synthesis tool available for FPGA design. It combines RTL graphical physical constraints with innovative algorithms that simultaneously employ timing and physical constraints to produce up to 35% faster circuit performance.

Design flow

The Synplify Pro solution interfaces to simulators such as Verilog-XL, NC-VHDL, Active-HDL, ModelSim and SpeedWave, plus major graphical entry tools. It integrates with place & route tools from Actel, Altera, Atmel, Cypress, Lattice, Lucent, QuickLogic, and Xilinx.

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