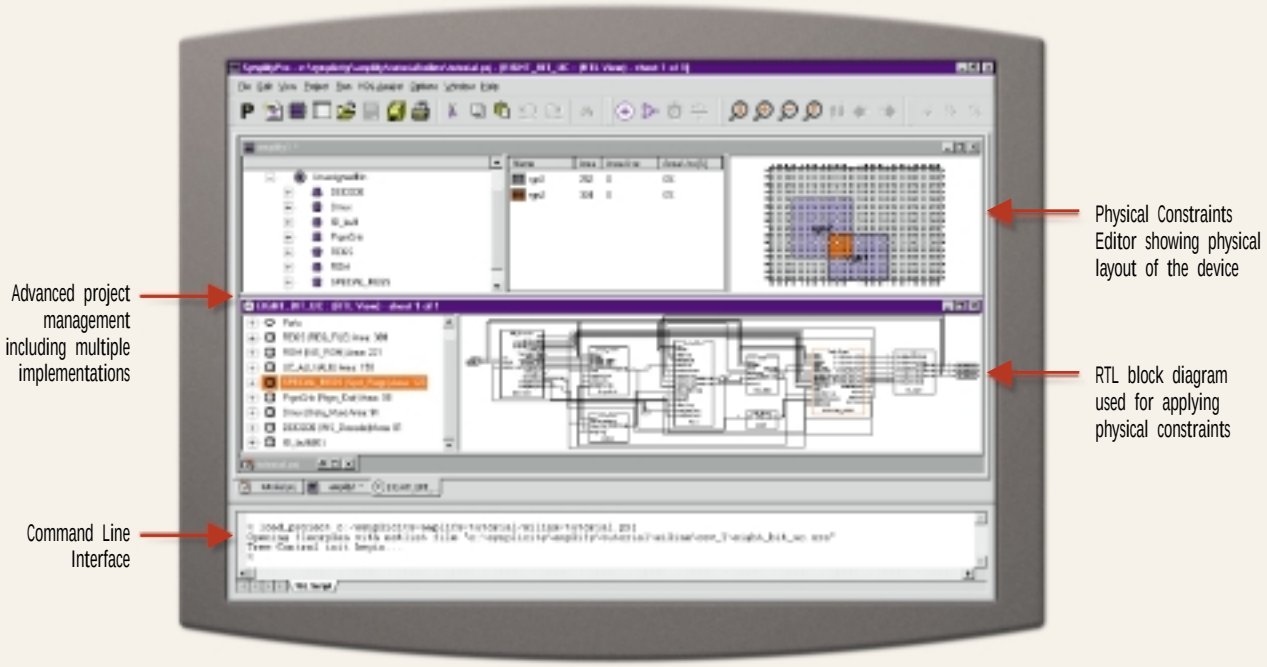
Amplify™ Physical Optimizer™

Physical Synthesis for Programmable Logic



With the introduction of Amplify Physical Optimizer, Synplicity has officially launched its latest product line — Amplify Physical Synthesis for FPGAs. Complementing Synplicity's market-leading Synplify® FPGA synthesis products, the Amplify Physical Optimizer is the first and only FPGA synthesis product to improve performance and accelerate productivity by utilizing physical design information during the synthesis process. Amplify Physical Optimizer was created specifically for programmable logic designers who need the highest performance possible from high-density Altera® and Xilinx® devices. Amplify Physical Optimizer combines an RT level graphical physical constraints editor with highly innovative new algorithms that simultaneously employ timing and physical constraints to produce superior circuit performance.

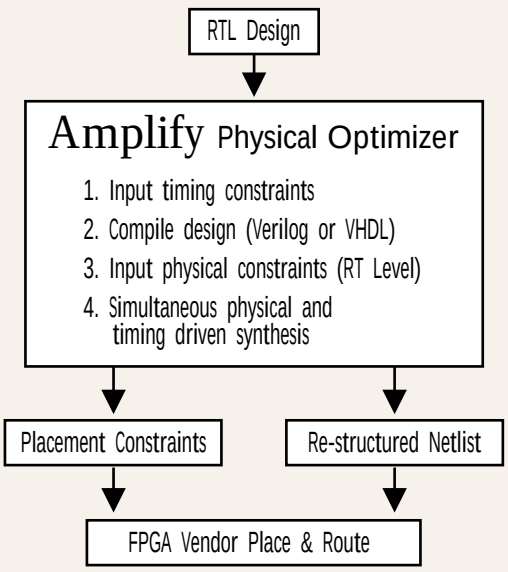
Significantly improved circuit performance

- Up to 35% better timing performance is achieved with Amplify Physical Optimizer when compared to traditional synthesis tools alone.
- Performance is significantly boosted by using physical synthesis techniques such as interconnect-based logic optimization, automatic replication of logic and boundary optimizations on critical paths. Improved performance is achieved without making changes to the HDL source code.

Enabling Features of Amplify	Benefits
Physical Constraint-Driven Optimizations	• Automatic replication of logic for performance. • Accurate placement-driven routing estimations enable the right optimizations without time-consuming iteration through synthesis and place-and-route • Tunneling (region-based interconnect estimations).
Work at Optimal Level of Abstraction	The RTL schematic of Amplify provides just the right level of abstraction for creating physical constraints. It features the same names of HDL modules with which designers are already familiar.
Team Design	Optimization across hierarchical boundaries increases performance while separate teams work on different parts of the chip in parallel.
Partial Physical Constraints	Focus only on critical areas of design limiting performance.
Persistent Physical Constraints	Changes in the HDL source code (i.e., widening a bus) do not require changes to previously created physical constraints.
Logic Replication	Easily force logic replication at the RT level for performance.

Saves weeks achieving aggressive performance goals

- Amplify Physical Optimizer displays the critical paths of a circuit in an easy-to-read schematic diagram. These critical paths are easily turned into physical constraints for the device and merged into the synthesis process reducing design iterations and saving valuable time.
- No changes to the physical constraints are needed when making RTL code changes. In other words, adding a state to a state machine or increasing the size of an adder does not invalidate the constraints and force rework as is the case with traditional netlist-level "floorplanning" tools.



- Amplify Physical Optimizer employs Synplicity's lightning-quick logic synthesis technology for performing the area estimations, providing useful feedback on how physical constraints should be applied.

Supports and improves team design

- Amplify Physical Optimizer manages the physical hierarchy of a design
- Amplify optimizes for performance across hierarchical boundaries, regardless of how a design is allocated across a team

Easy to learn and use

- As with all Synplicity products, Amplify Physical Optimizer's clean, intuitive user interface makes learning and using it a quick and painless experience. Information is presented graphically at the right level of abstraction for maximum efficiency.
- Synplify users will be productive with Amplify Physical Optimizer within a few days. A tutorial is provided with the product to accelerate learning.

Synplicity, Inc.
935 Stewart Drive
Sunnyvale, CA 94086
Phone: (408) 215-6000
Fax: (408) 990-0290
www.synplicity.com

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