System Generator V1.0

October 6, 2000 | Product Datasheet

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Introduction

Xilinx announces the System Generator™ tool V1.0 for Simulink®. The System Generator enables you to develop high-performance DSP systems for Xilinx Spartan®-II and Virtex™/E FPGAs using The MathWorks products, the MATLAB® and Simulink.

Features

- System-level abstraction of FPGA circuits
  - Visual data-flow paradigm
  - Bit-true and cycle-true Simulink library for common functions
  - Sample rate vs. explicit clocking
- Automatic code generation from a Simulink model
  - Synthesizable VHDL for Simulink model
  - Simulink hierarchy is preserved in VHDL
  - HDL testbench
  - ModelSim script files
- Support for user-created Simulink library elements (black boxes)
  - C++ classes to support core modeling (fixed-point arithmetic, S-function base classes)
  - Black Box netlisting (instantiation templates)
- Transparent access to Xilinx IP via the Xilinx CORE Generator™ System
  - FPGA designs are generated using Xilinx LogiCORE algorithms ensuring that the most efficient code is being generated.

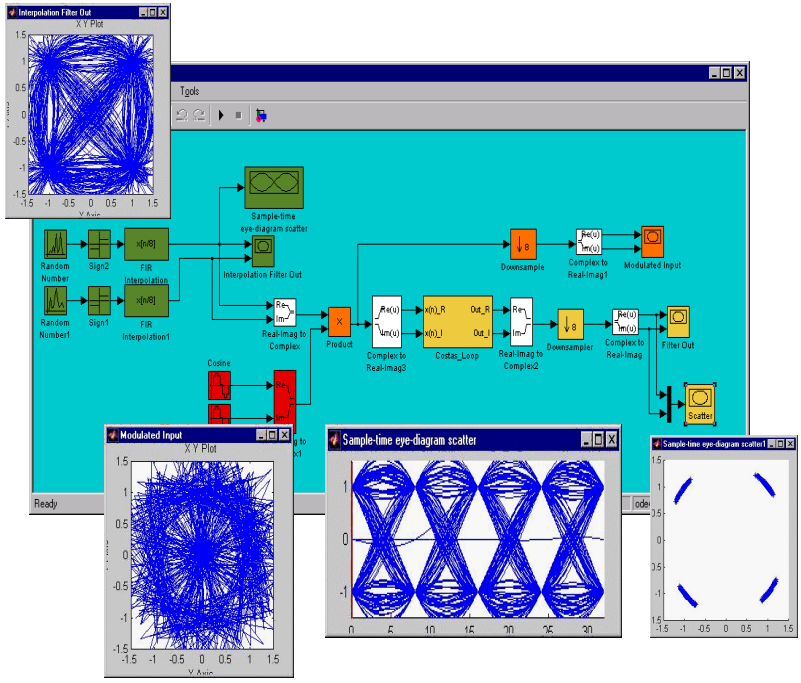

Figure 1: Xilinx System Generator for Simulink

Functional Description

Figure 2 shows the general flow of the System Generator functionality as it fits in with The MathWorks and Xilinx implementation software tools.The Simulink Block Library contains blocksets used to model systems within the Simulink GUI. The System Generator software provides an additional blockset to the library: the Xilinx Blockset. As shown in the flow diagram, the blockset elements can be instantiated within a Simulink model (within the MATLAB environment) just like any other Simulink block. You can model and simulate with the Xilinx Blockset as you are accustomed to doing within Simulink.

When you are through modeling you can then add the System Generator token at the level of hierarchy you would like to generate code. When the HDL code generation software is invoked, VHDL code, cores, and test vectors are generated according to system parameters defined within the model. The cores are created using the Xilinx CORE Generator. The VHDL source can be compiled and simulated in a VHDL simulator, and an FPGA implementation can be obtained by applying a synthesis tool to the VHDL. After synthesis, the System Generator project can be run through the Xilinx implementation tools (build, map, place, and route) to produce a bitstream for download to an FPGA device.

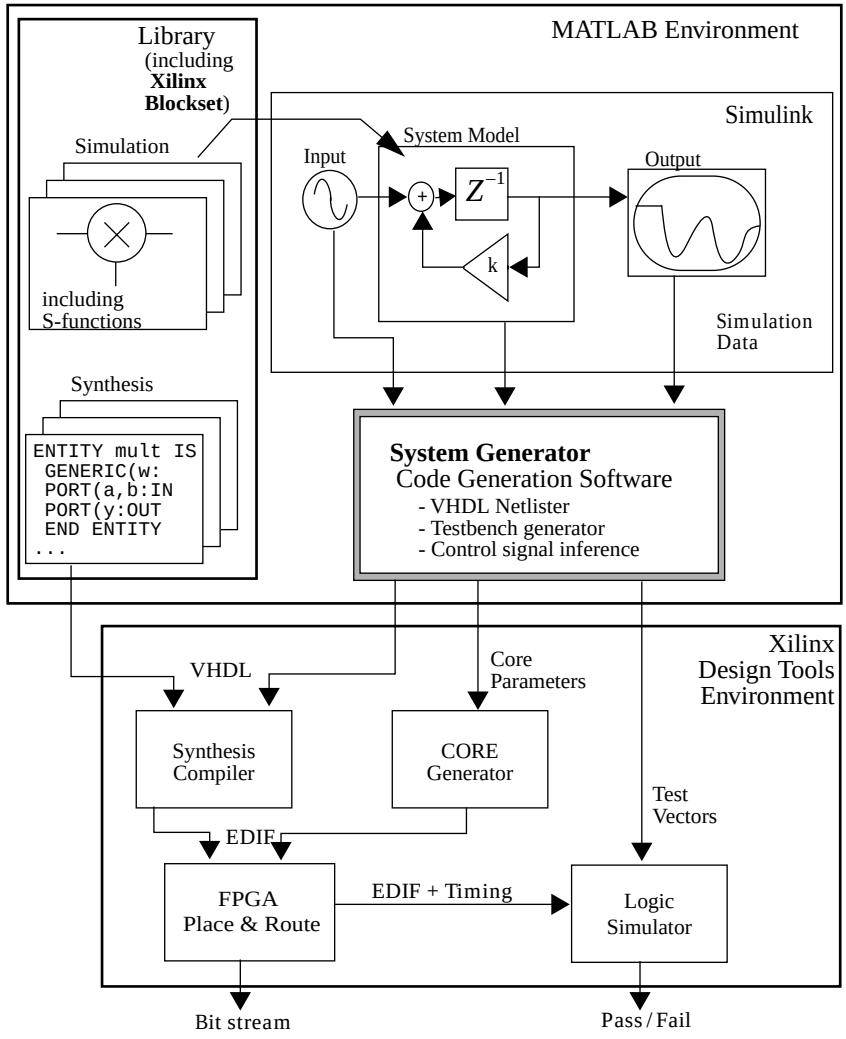

Figure 2: System Generator Flow Diagram

Xilinx Blockset

The Xilinx Blockset is a major component of this release of the System Generator.

Like other Simulink Blocksets, the Xilinx Blockset contains elements that can be used to build simulation models. In addition, models built from the Xilinx Blockset can be translated using the System Generator into synthesizable VHDL circuits. After the System Generator has been installed, the Xilinx Blockset will be visible in the Simulink Library Browser.

Xilinx Blockset elements include VHDL models and association with Xilinx LogiCOREs. These models enable VHDL code to be generated for Simulink designs made up of Xilinx blocks.

Currently, the Xilinx Blockset contains the following elements:

- Basic Elements
  - System Generator
  - Black Box
  - Concat
  - Constant
  - Convert
  - Counter
  - Delay
  - Down Sample
  - Get Valid Bit
  - Mux
  - Register
  - Set Valid Bit
  - Slice
  - Up Sample
- DSP
  - FFT
  - FIR
- Math
  - Accumulator
  - AddSub
  - CMult
  - Inverter
  - Logical
  - Mult
  - Negate
  - Relational
  - Scale
  - Shift
  - Threshold
- MATLAB I/O
  - Clear Quantization Error
  - Display
  - Gateway In
  - Gateway Out
  - Quantization Error
  - Sample Time
  - Scope
- Memory
  - Dual Port RAM
  - ROM
  - Single Port RAM

System Generator Token

A special Xilinx Blockset element is the System Generator token. This token can be selected from the Simulink Library Browser, from within the basic elements of the Xilinx Blockset.

The System Generator token invokes the Code Generation Software, the second major portion of the tool. By placing the System Generator token on your Simulink project sheet, you can generate VHDL code and cores for all the Xilinx Blockset elements on that sheet and on any sheets beneath it in its project hierarchy. This also enables you to simulate a mixed mode design and then generate a digital realization of the digital portion of the design by placing the token in the digital hierarchy only.

VHDL Code Generation Software

The System Generator includes software to enable translation and simulation. The translation software is invoked from Simulink and provides an interface to the Xilinx FPGA software. This interface includes a compiler to translate a Simulink model into a synthesizable VHDL model, including generation of Xilinx cores where appropriate. FPGA designs are generated using Xilinx LogiCOREs, ensuring that the most efficient code is being generated.

Simulation software provides C++ fixed-point arithmetic libraries to support XBS and user-written, run-time parameterizable Simulink S-functions, including support for rounding and overflow. The Simulation software set also includes classes which allow a user to create a C++ executable model and easily incorporate it as a Simulink S-function for simulation.

Testbench Generation

If enabled, a VHDL testbench “wrapper” file is created for your generated designs. The testbench “wrapper” file is named to match the top-level VHDL file generated for your project. For example, if your top-level VHDL file is named integrate, the System Generator will create a wrapper file called integrate_testbench.vhd. The top level of the project is determined by the name of the Simulink sheet from which you have invoked the System Generator token. You may run the testbench (which uses these test vectors) in a behavioral simulator such as ModelSim from Model Technology. It should report any discrepancies between the Simulink simulation and the VHDL simulation. You can verify the translation of your Simulink design using this method.

Black Box Token

The Xilinx Blockset “Black Box” token gives you the ability to instantiate your own specialized functions in your design, and subsequently into a generated model. Any Simulink subsystem may be treated as a “Black Box” if you so choose. You may want to build a model out of non-Xilinx blocks, or you may have a VHDL-representation of functionality that you wish to turn into a Simulink model.Similar to the System Generator token, the Black Box token may be placed on any Simulink subsystem, identifying the subsystem as a Black Box.

Documentation

When you have purchased the System Generator, you may access the online software manuals from the Xilinx home page (http://www.xilinx.com). The System Generator tool from Xilinx is release with the following documents:

- *System Generator Quick Start Guide*
- *System Generator Tutorial*
- System Generator Datasheet

The MathWorks Documentation

The MathWorks provides a printed documentation suite that you should have received with your purchase of MATLAB, and Simulink. The software manuals include the following:

- *Using MATLAB*
- *MATLAB New Features Guide*
- *Getting Started with MATLAB*
- *User’s Guide for MATLAB Toolboxes*, including:
- *Communications Toolbox*
- *Signal Processing Toolbox*
- *Wavelet Toolbox*
- *Control System Toolbox*
- *Image Processing Toolbox*
- *Using Simulink*
- *DSP Blockset User’s Guide - for use with Simulink*

Related Information

Xilinx products are not intended for use in life support appliances, devices, or systems. Use of a Xilinx product in such applications without the written consent of the appropriate Xilinx officer is prohibited.

Ordering Information

The Xilinx System Generator is provided under *Xilinx Time-Based Software License Agreement*. For purchase, price, and availability information, please visit the Xilinx IP Center at **www.xilinx.com/ipcenter** or contact your local Xilinx Sales Representative.