Certify™

Accelerating the first-pass success of complex ASICs with early and rapid RTL prototyping

- 60% of the design flow typically is spent in verifying the ASIC.
- Over 42% of ASICs must be redesigned at least once because functional bugs are not found prior to fabricating the ASIC.
- Redesigning and refabricating an ASIC can take several months and over $1M.
- Software development and systems integration typically must wait for a functionally correct ASIC.
- For one of our customers, missing the market window for their networking product could cost them over $1M per day.

So many gates. So little time.

"We caught over 500 bugs by using Certify to generate an FPGA-based prototype."

Networking ASIC Design Manager

A prudent economic approach

While certainly important, timing and risk are not the only considerations when devising a development strategy. Cost is a primary concern, particularly in the context of advanced silicon system development. Today, NRE alone for a prototype run through an ASIC fab is about $1M — with an expected increase to $1.5M as feature sizes dip below the .25µ realm. Now, more than ever, it's critical a design is fully functional and verified prior to committing to a fab run. Respins not only impact time to market, but also carry a stiff financial penalty.

By contrast to an ASIC prototype, the cost of an RTL prototype can be under $100K — including tools and production costs. PLD-based prototyping leverages the cost and time-to-market advantages of field programmable devices to enable rapid and very cost-effective system implementation. At the same time, the verification and early market entry this prototyping methodology enables significantly reduces your project risk by assuring a viable design prior to ASIC implementation.

Certify

"I've been an ASIC designer for over 10 years and I've emulated designs with Quickturn and IKOS emulation systems. I've also spent time looking at the possibility of prototyping ASICs with FPGAs before, and this product is one of the better ones I've ever used."

Graphics Processor Development Manager

"All of our ASICs from now on will be prototyped with Certify."

Multimedia ASIC Design Engineer

"We're new users of Certify. It's much more powerful than it may seem at first glance."

ASIC Design Engineer

"One of the nicest Certify features is that it provides a GUI interface which allows a designer to view a schematic of his design and provides the ability to "drag and drop" modules into graphical representations of FPGAs."

Video ASSP Developer

"We can freely mix and match FPGAs, memories, and MSI logic on our PCBs with Certify. It's also good for design debugging."

Wireless Device System Architect

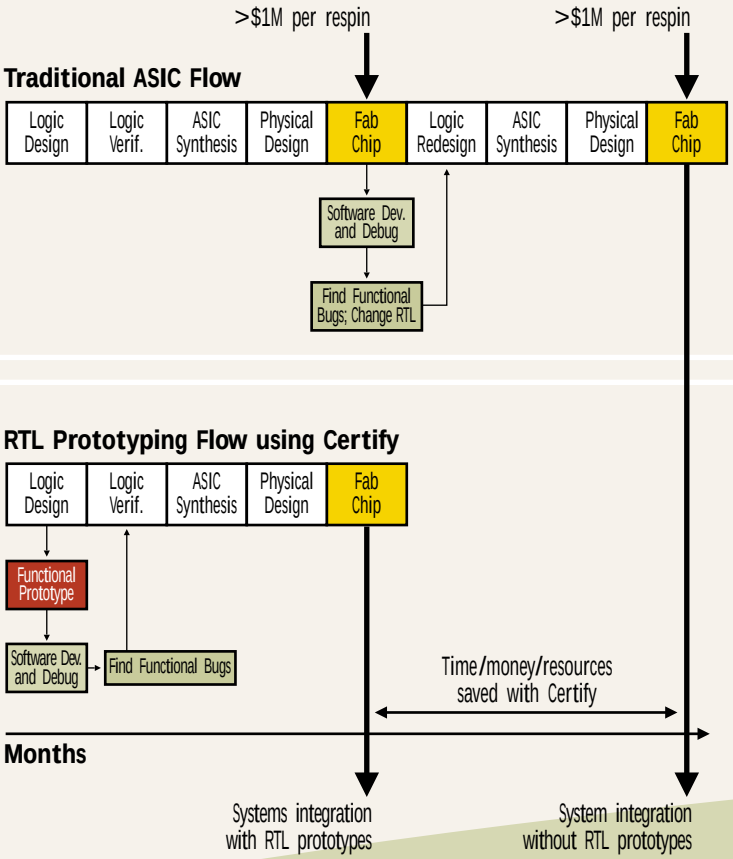
Giving designers control

Today, there is a breakthrough in ASIC functional verification. Using Synplicity's Certify design environment, you can now prototype and debug your million-plus-gate design in programmable logic.

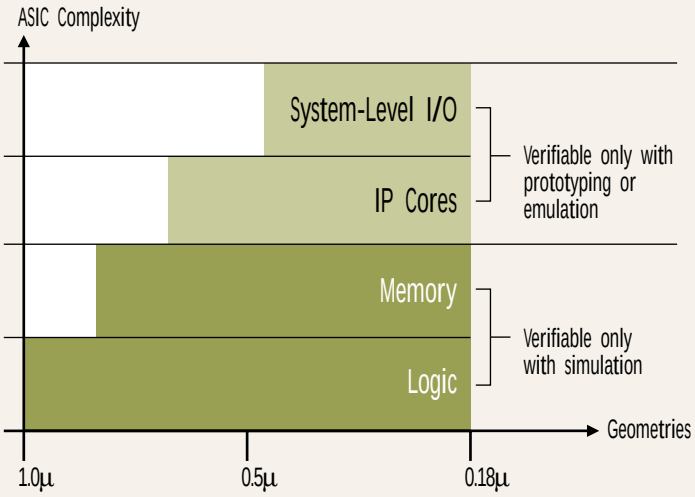
In record time, you can:

- verify and debug hardware and software at near real-time speeds
- create an early market-entry vehicle in about one month's time at a fraction of the cost of ASIC development
- test product features before spending months iterating through ASIC synthesis and place-and-route
- develop derivative products in a fraction of the time

Clearly, the Certify design environment is a process that translates into significant competitive advantages.



Traditional ASIC design and verification methods typically rely on getting first silicon back from the fab in order to verify system-level functionality. This also means that your software team has to wait for ASIC synthesis, place-and-route, and fabrication to begin their efforts with system integration and software debugging. With Certify, you can achieve first-pass design success by using RTL prototypes to test hardware and software functionality, identifying and fixing problems where they occur in your design flow.



Every recent generation of silicon technologies has brought more system-level capability in the ASIC design flow. However, older verification methodologies are sufficient only for verifying logic and memory. With Certify-based prototypes (running typically between 10 and 60 MHz) the ASIC designer now can verify at the RT level full SoC ASIC capabilities, such as complex IP cores and high speed system I/O.

New ASIC designs need new methods

RTL prototyping is the only way to achieve the performance level needed to verify some types of ASICs. Most RTL prototypes operate between 10 and 60 MHz, allowing you to test real-life conditions for your design. Companies serving performance-driven markets such as wireless, networking and multimedia applications are in dire need of a vehicle to validate high-speed system functionality. Traditional emulation methods, which cap out at about 1MHz, have become inadequate for complete and accurate validation of the vast array of functional behaviors of these applications.

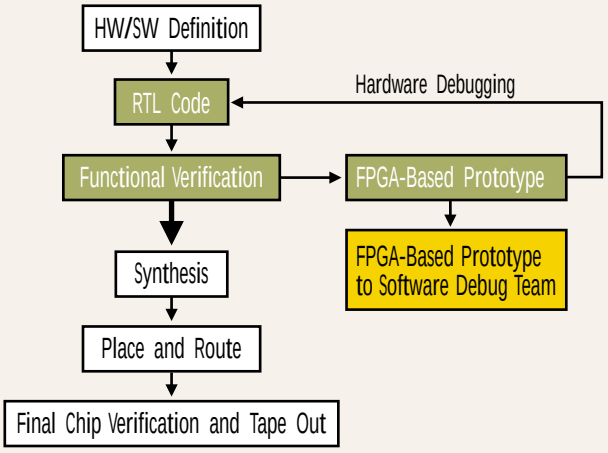
First pass success

Accurate RTL prototypes should help ensure designs go through the fab with first-pass success. With an early hardware prototype, developers of performance-driven applications are gaining valuable insight into device operation at close-to-true speed.

Even more companies are driven to RTL prototyping by time-to-market demands. Fiercely competitive arenas such as communications and computing markets, as well as supply chain intermediaries such as ASIC and ASSP providers, are intensely governed by rapid product delivery. These companies must demonstrate a design as fast as possible, and move it into volume production at the same breakneck pace. Protracted ASIC redesign cycles are proving to be too long and too risky. Using an RTL prototyping methodology, these suppliers are rapidly verifying the functionality of their SoCs or SoC components at the RT level and reducing the risk of perilous design respins.

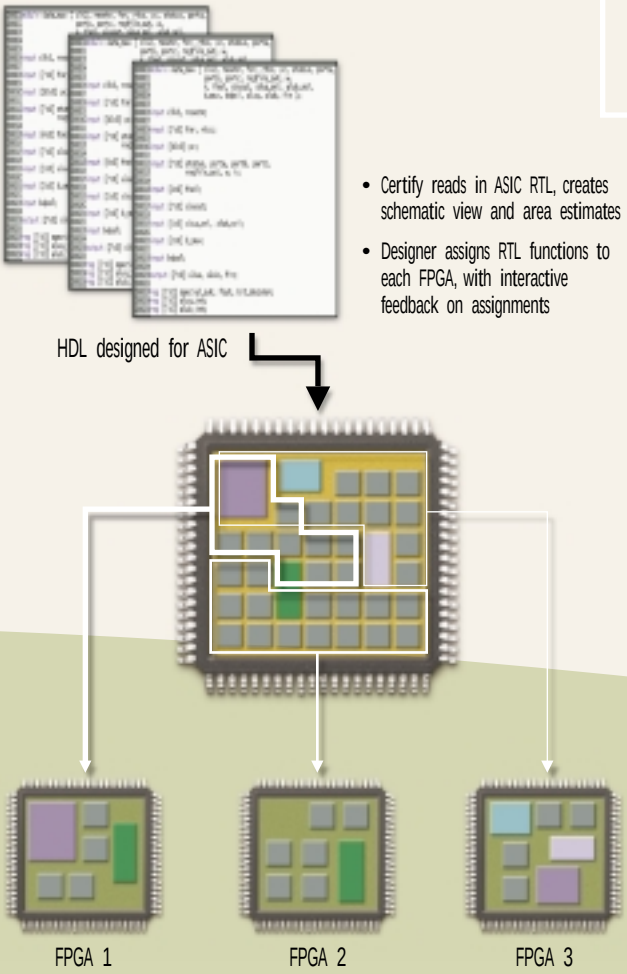
Another strong motivation for RTL prototyping is hardware/software codesign. System-on-chip designers, as well as hard IP providers, must check hardware and software compliance while optimizing their system implementation. Design automation-based codesign solutions have proven impractical due to the high cost and high level of expertise required to use them. RTL prototyping with Certify provides a prudent alternative, making it possible to debug software and verify compliance based upon real hardware early in the design cycle.

If you need to...	Certify Benefit	Savings/Value
avoid ANY design respins	prototype allows full-speed functional verification, tests system-level operation, accelerates simulation	>$1M per respin
provide drivers/firmware with ASIC	typical prototype operation is from 10-60 MHz, sufficient for software development /debug	2-3 month acceleration of software development
prove that ASIC is compliant to external software and hardware standards	prototype processes real-time input, generates real-life output, can test compliance	greatly reduced risk of final product not being compliant; potential savings of millions
beta test system with customers	prototype boards are easily replicated to provide to multiple customers	faster customer adoption, higher product quality at first shipment
get functional hardware to third-party software developers	gives software developers functionally correct hardware prior to ASIC synthesis	brings hardware and software development in parallel, missing piece to true hw/sw codesign
demo functionality at trade shows	programmable parts allow late-stage design modifications, can demo system at or near final speed	accelerates product adoption; potential benefit of millions of dollars
validate late-stage design modifications	implement and test changes in FPGA-based prototype	faster time to market, faster systems re-validation



Improving the ASIC design flow

If RTL prototyping is integrated with an overall ASIC design environment, it's a very effective vehicle for early market entry and design verification. Because it reads in standard ASIC RTL code, Certify ensures that RTL-prototyping does not interfere with your standard development flow. RTL prototyping is effective in helping to resolve design flow issues downstream.



Certify — RTL prototyping in record time

Leveraging Synplicity's core FPGA synthesis and partitioning technologies, Certify enables creating a functional hardware prototype of your ASIC at the RT level, prior to synthesis. Advanced synthesis algorithms coupled with the latest FPGA architectures ensure the highest performance prototypes.

Certify is based on Synplicity's proprietary Behavior Extraction Synthesis Technology™ (B.E.S.T.™) and Partition Aware System Synthesis (P.A.S.S.) algorithms. Unlike alternative methods that optimize at the gate level, B.E.S.T. algorithms maintain high levels of abstraction during RTL optimization, resulting in unprecedented performance levels. The P.A.S.S. technology utilizes partitioning information in the synthesis process, providing performance-driven partitioning of the prototype components. Certify is the only tool for ASIC prototyping that performs timing analysis and synthesis across all FPGAs in one operation. This means your performance is optimized for the entire prototype — not individual FPGAs.

Some of Certify's advanced ASIC prototyping features:

- complete GUI and command line interfaces for user efficiency
- no RTL code changes for prototyping
- concurrent multi-FPGA synthesis and timing analysis
- support for black box timing models
- cross-probing across all design views and RTL source
- automated what-if analysis
- automated MUX decomposition
- automated logic replication and probe point creation

Results

The productivity of Certify-based RTL prototyping is unparalleled. Translating your verified RTL code into a functionally equivalent set of FPGAs for prototyping takes days. Compare this to the months involved with traditional ASIC synthesis or place-and-route techniques. With Certify, you can typically generate a complete hardware prototype, in the form of a FPGA-based board, in under a month, for less than $100K, including the tools.

Leveraging Synplicity's industry expertise

To successfully adopt a new design methodology, you must successfully adopt the right technology partner. This is especially critical when selecting an EDA partner for RTL prototyping with FPGA/PLD technology. A successful RTL prototyping methodology relies upon state-of-the-art design automation technology that works with the most advanced FPGA devices and is well integrated with ASIC implementation tools you already use. The extent to which all of this technology is brought together in a workable, productive solution depends largely on the EDA partner involved.

Synplicity's focus on FPGA design and its access to the latest FPGA technology are legendary in the electronic design automation industry. Since 1994, Synplicity has focused on developing fast and easy-to-use products delivering the best Quality of Results — all backed by the smartest and most responsive technical support team in the business. This dedication to successful FPGA design has resulted in strong partnerships with leading PLD suppliers. With these close alliances in place, Synplicity supports the absolute latest FPGA solutions from the moment they become available. Leveraging Synplicity's industry expertise, you can access the latest programmable technology with highly productive synthesis and partitioning solutions. Simply put, Synplicity and Certify provide you the best opportunity to be the most competitive with your next product.

Synplicity®

Simply Better Results™

Synplicity, Inc.
935 Stewart Drive
Sunnyvale, CA 94086
Phone: (408) 215-6000
Fax: (408) 990-0290
www.synplicity.com

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