



PRESENTS

NETWORLD INTEROP



Faster than a Speeding Packet: Network Processors hit \$7 Billion in 2005

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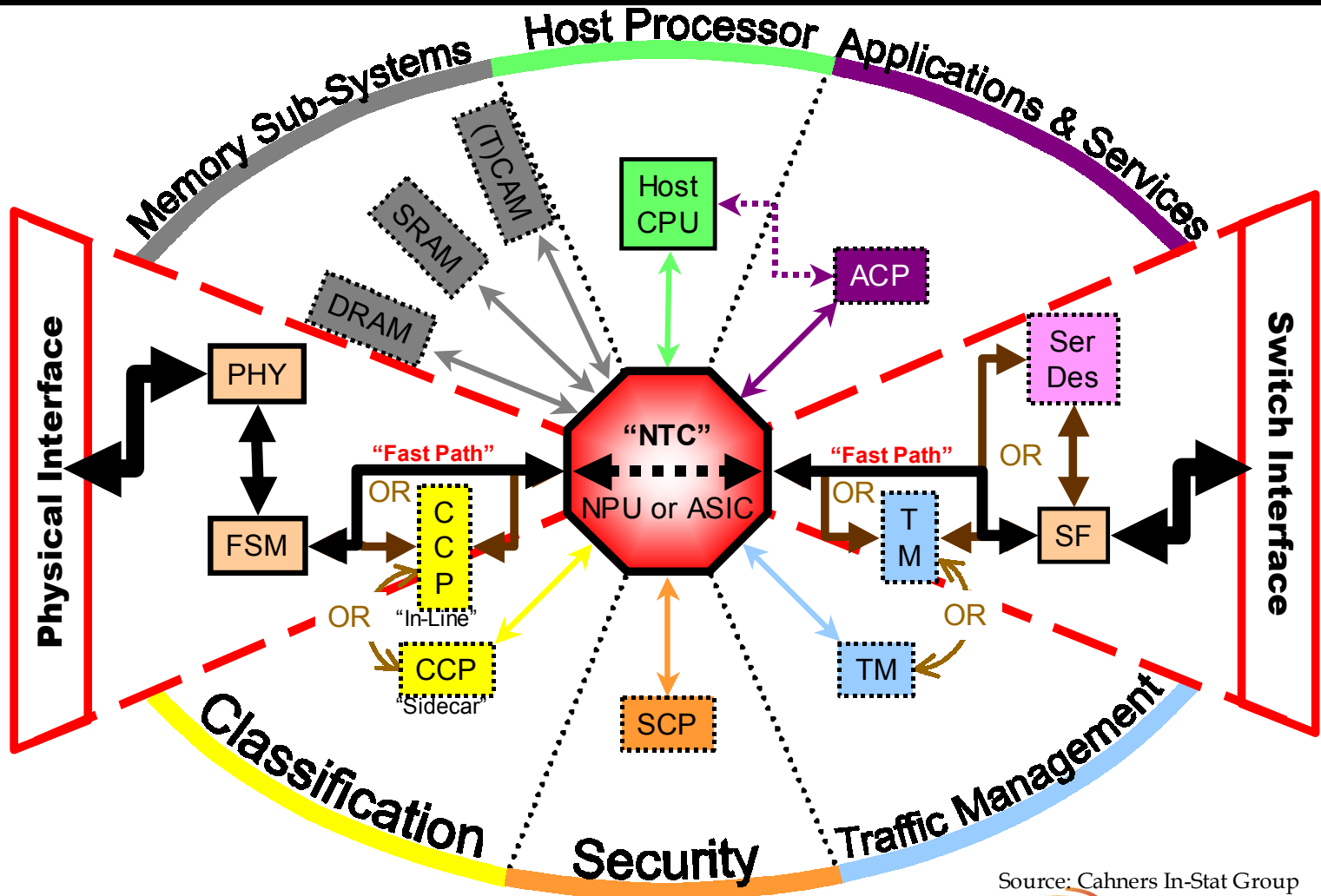
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What is a Network Processor?

- **Network Processor (NPU)**: a non-ASIC based Integrated Circuit (IC) or IC Chip-set that is software programmable and performs all packet header operations between the physical layer interface and the switching fabric. Further, there are two grades of NPUs that will be addressed in this presentation based on the wire speed they can handle doing a minimum of IPv4 forwarding:
 - Mid-Range:
 - ASPs between \$250 and \$640 (1.2 to 4.8 Gbps typical)
 - Defined as Wire Speed from 622 Mbps up to 5 Gbps
 - High-End:
 - ASPs between \$1600 and \$2100 (10 Gbps typical)
 - Defined as Wire Speed of 5 Gbps or higher

Where do NPUs Sit?



Source: Cahners In-Stat Group

Related Components:

- **Classification Co-Processor (CCP)**: A kind of NCP that helps unburden the NPU by parsing and classifying a packet. The classification of packets is currently the most processor intensive portion of Network Processing.
- **Security Co-Processor (SCP)**: A kind of NCP that handles all of the security needs of packet processing. Most common functionality added is IPsec.
- **Application Co-Processor (ACP)**: The newest kind of NCP that helps an NPU that only handles Layer 2 & 3 of the OSI reference model. The ACP will handle Layer 4 through 7 (Application Layer) functions including billing, Load Balancing, and Virtual Private Networks (VPNs); among others.

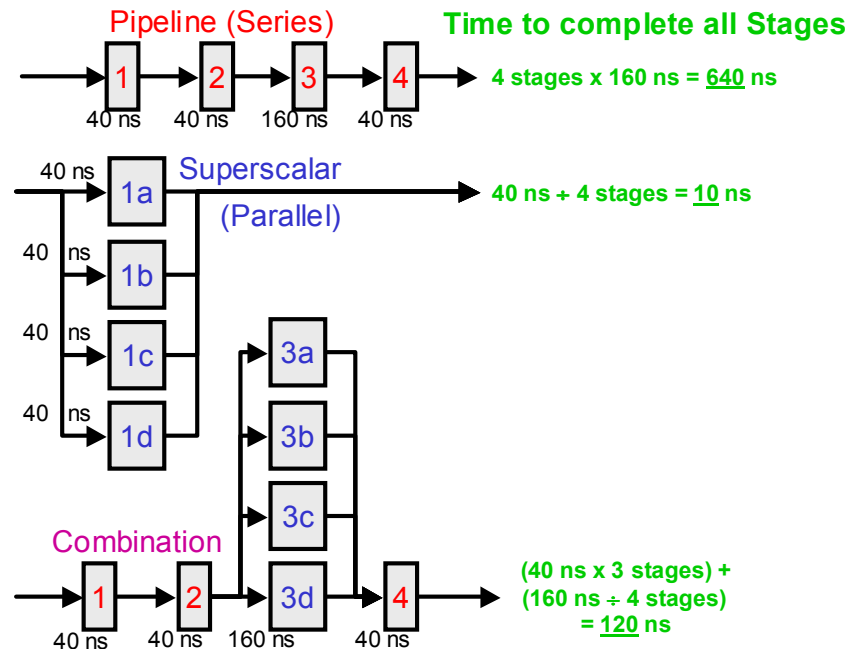
Related Components:

- **Traffic Manager (TM)**: Handles Queuing and Transmission along with other output functions like Load Balancing and Quality of Service (QoS). Not all NPU solutions will have a TM chip as some vendors integrate these functions within the NPU. Currently, the TM will almost always sit in the data path between the NPU and Switch Fabric.
- **Switch Fabric (SF)**: The chip through which one NPU will connect to another, often on a switching card or back plane. SFs vary greatly, but they are a crucial and fundamental aspect of any network processing solution.

Why is Network Processing Difficult?

- ATM over SONET:

- Time between SONET frames is 125msec:
- At OC-48: 5.4 million ATM hdrs/s or a new ATM header every 186 ns.
- At OC-192: 21.5 million ATM hdrs/s or a new ATM header every 46.5 ns.



Source: Cahners In-Stat Group

- IP acknowledgement packets (40 byte) encapsulated in SONET:

- At OC-192: a new IP header every 37.4 ns. or 0.0000000374 Secs

- Number of Possible IP Address with IPv6:

- 56,713,727,820,156,400,000,000,000,000

Trends and Upcoming Attractions

- **Software Companies:**
 - LVL7, Teja Technologies, RADLAN, IP Infusion, Microware Systems, and others
 - Shorter Time-To-Market
- **Complete PHY to Fabric Solutions**
 - Use NPU to leverage the rest of the design wins
 - Approximately double the revenue potential.
- **High-End NPU vendors:**
 - EZchip, Cognigine, Internet Machines, Bay Microsystems, Agere, AMCC, Silicon Access, Xelerated Packets, ONEX
 - First products to be released this year
 - Buyouts & Mergers will happen
 - At least a year for “real” volumes

Based on 15 Market Segment analysis:

- ATM WAN Switches
- ATM LAN Switches
- Fast Ethernet Switches
- Gigabit Ethernet Switches
- Mid-Range Routers
- High-End Routers
- SAN Switches
- DSLAMs
- Terabit Routers
- Purpose Built VoIP Gateways
- Remote Access Concentrators
- 10 Gigabit Ethernet Switches
- Basestation Controllers
- Mobile Switching Centers
- Wireless Base Stations

Sample Segment: Terabit Routers

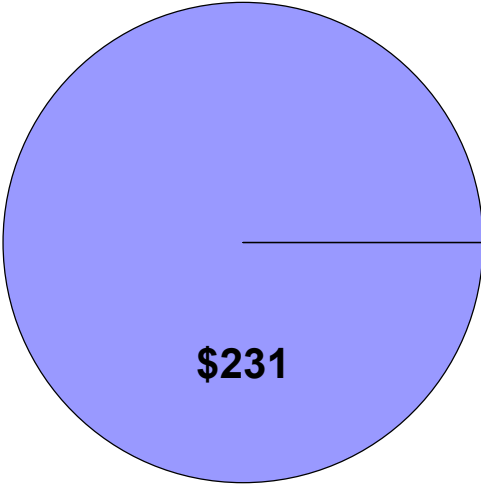
Terabit Routers	2001	2002	2003	2004	2005	CAGR
Total NPU (k)	17	101	529	1,263	2,367	193.9%
% Change	58%	495%	421%	139%	87%	
Total Revenue (\$k)	\$ 9,069	\$ 65,602	\$ 306,454	\$ 697,120	\$ 1,372,400	160.5%
% Change	107%	623%	367%	127%	97%	
Weighted ASP	\$ 532.24	\$ 646.78	\$ 579.86	\$ 552.06	\$ 579.77	6.1%
% Change	31%	22%	-10%	-5%	5%	

Source: Cahners In-Stat Group

Network Processor Forecast 2001 to 2005

2001

■ Mid-Range NPU Revenue (\$M)



2005

■ Mid-Range NPU Revenue (\$M)

■ High-End NPU Revenue (\$M)

