# Instructions to boot pre-packaged operating system on OpenSPARCT1 soft core

## What is needed to complete this exercise

1. Xilinx ML505-XC5VLX110T or ML411 board
2. Internet access to download reference design from the web and to access online documentation
3. PC, laptop, or a workstation with a spare serial port
4. RS232 null model cable to connect ML505 serial port with the host computer
5. If you do not have a serial port on your computer, you will need serial to USB converter and corresponding software driver

   RS232 null modem and Serial to USB converter can be purchased from Amazon or a local electronics store. Sample links listed below.

http://www.amazon.com/Deluxe-Null-Modem-Cable-Female/dp/B000AA2PSA/ref=sr_1_1?ie=UTF8&s=electronics&qid=1210271084&sr=1-1

http://www.amazon.com/TRENDnet-USB-to-Serial-Converter/dp/B0007T27H8/ref=sr_1_1?ie=UTF8&s=electronics&qid=1210271198&sr=1-1

**NOTE – Apple Mac may require different cables and drivers**

6. Hyperterminal on a laptop, or similar facility, to communicate on a serial/USB port
7. At least 1GB Compact Flash to load the reference design in the memory of the ML505-XC5VLX110T board
8. Flash reader/writer to copy files on to compact flash from a computer. Sample link from Amazon listed below:

http://www.amazon.com/SanDisk-ImageMate-Reader-Writer-SDDR-92-A15/dp/B00064V6R6/ref=sr_1_1?ie=UTF8&s=electronics&qid=1210288581&sr=1-1

## Instructions to get started

1. Download the latest version of OpenSPARC T1 hardware tar ball from

   http://opensparc-t1.sunsource.net/download_hw.html

   Downloaded hardware bundle should have following file name OpenSPARCT1.1.6.tar.bz2

2. Expand the tar ball by executing following commands at the UNIX prompt

   ```
   # bunzip2 OpenSPARCT1.1.6.tar.bz2
   # tar -xvf OpenSPARCT1.1.6.tar
   ```

   Go over README file, located in the top directory, for the details on the package contents and quick way to run logic synthesis, functional simulation, and FPGA synthesis.

For more detailed description of the design and the verification environment, refer to the PDF documents included in /doc directory.

3. For the quick operating system boot on the FPGA board (details below), we have included a pre-compiled reference design with single-core four-thread OpenSPARCT1 core. The reference design also includes pre-compiled disk image of stripped-down OpenSolaris snv_77 installation.

   Location of the System Ace file with the pre-packaged reference design:

   design/sys/edk/ace/OpenSPARCT1_1_6_os_boot.ace

4. Connect the Flash Reader/Writer with the computer and copy the ace file to one of the rev[0-7] directories on the Compact Flash.

   Typical directory structure of Compact Flash card should look like this:

```
E:\
  |
  |---- xilinx.sys     (This file is generated by Xilinx EDK, do not modify)
  |
  |---- config
              |
              |---- rev0
              |---- rev1
              |---- rev2
              |---- rev3
              |---- rev4
              |---- rev5
              |---- rev6
              |---- rev7
```

   The SW3 DIP switches on the ML505 board tell the board where to look for the System Ace file. Switches 4-8 select the device that is used to program the system. These switches must be set to 10101 to select the compact flash drive. Switches 1, 2, and 3, tell the system where to look for the System Ace file on the compact flash. A setting of 000 corresponds to the rev0 directory on the compact flash, while setting of 111 selects the rev7 directory.

   For more details on the board, cables, and DIP settings refer to following documents on the Xilinx web page:

   http://www.xilinx.com/products/boards/ml505/reference_designs.htm

   Documents titled “ML505 Getting Started Tutorial” and “ML505 QuickStart” should be the most useful.

5. Set up the ML505-XC5VLX110T board by connecting power cord, and null serial model with an optional serial to USB converter. Also gently insert the Compact Flash into the CF slot on

the back side of the FPGA board. Also select the appropriate SW3 DIP switch settings to correspond to where the ACE file is placed on the CF.

For more details refer to “Board Setup” section of “ML505/ML506 Getting Started Tutorial” located at - http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf

6. Open Hyperterminal, connect to the proper COM port for the serial cable, and set the port settings to 9600 Baud, 8 data bits, no parity, one stop bit, and flow control none. Details of this settings can be found in the “ML505/ML506 Getting Started Tutorial” mentioned above.

7. Power on the ML505-XC5VLX110T board.

**What happens at Power On**

- The FPGA bit file is transferred from the compact flash card to configure the FPGA
- The compressed OpenSolaris ramdisk installation image is copied from compact flash card to DRAM starting at address 0x5af00000
- The ccx-firmware code running on microBlaze processor takes the following actions.
  - uncompress ramdisk image
  - initialize OpenSPARC T1 memory.
  - initialize peripherals
  - poweron OpenSPARC T1

- OpenSPARC T1 actions
  - Execute poweron reset code
  - Hypervisor initialized
  - Open Boot Prom (OBP) booted

- At OBP prompt (“ok”), type "boot -mverbose" command

  ok  boot -mverbose

  The above command will boot disk image of the OpenSolaris operating system with all the services enabled. This boot process will take approximately 60 minutes.

  If you wish to achieve a faster boot (about 30 minutes), type following at the OBP command prompt

  ok boot -m milestone=none

  For more details on the difference between these two options, refer to the Frequently Asked Questions (FAQ) under:

  design/sys/edk/os/OpenSolaris/docs/t1_fpga_opensolaris_faq.txt

  Once you see login prompt, login as “root” at the console. there is no password.

**NOTE** - The system response could be slow in the beginning because OpenSolaris could still be initializing OS services in the background.

## Connecting the FPGA system to the network

OpenSolaris must be booted with full services (with boot -mverbose) option to be able to enable network with the FPGA system. Use "svcs" command to verify that all services are online except for "legacy_run" services before proceeding with network configuration change.

The default IP address and network configuration may not be appropriate for the network to which the system is going to be connected. Default values are listed below:

IP address: 192.168.186.100
Broadcast: 192.168.186.255
Netmask: 255.255.255.0
Gateway: 192.168.186.1
Domain: my_domain_name.com

We recommend changing default configuration with your network specific settings using following sequence of commands:

```
# ifconfig snet0 down
# route -f
# ifconfig snet0 inet <new_ip_address> broadcast <new_broadcast_address> netmask <new_netmask>
# domainname <new_domain_name>
# ifconfig snet0 up
# route add default -gateway <new_gateway_address>
```

DNS is not enabled on the FPGA system, therefore IP addresses have to be used instead of hostnames.

```
# ping <remote_machine_ip_address>
```

This completes the OpenSolaris boot on OpenSPARC T1 FPGA system running on Xilinx ML505-XC5VLX110T board. Source code for all the components used to build this system is included in the OpenSPARC T1 v1.6 download bundle. You can modify and recompile any or all these components to develop your own reference design.

For more information, visit www.opensparc.net.

If you have specific questions, post them in OpenSPARC forums at
http://forum.java.sun.com/category.jspa?categoryID=120

Have fun,

OpenSPARC Team.