XILINX®

Chapter 4

PCB Design Considerations

Summary

This chapter covers the following topics:

- Pinout Information
- Pinout Diagrams
- Package Specifications
- Flip-Chip Packages
- Thermal Data
- Printed Circuit Board Considerations
- Board Routability Guidelines
- Power Consumption
- IBIS Models
- BSDL and Boundary Scan Models

Pinout Information

Introduction

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the **Virtex-II Data Sheet**). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4-1 provides definitions for all pin types.

The FG256 pinouts (Table 4-2) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the **www.xilinx.com** website.

Pin Definitions

Table 4-1 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4-1: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, DIN/D0 – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
DIN / D0, D1, D2, D3, D4, D5, D6, D7	Input/Output	In SelectMAP mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. In bit-serial modes, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.

Table 4-1: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins[1]		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pullups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input	Power down pin.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Do not connect if battery is not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

FG256 Fine-Pitch BGA Package

As shown in Table 4-2, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256 fine-pitch BGA package. Pins in the XC2V250, XC2V500, and XC2V1000 devices are the same. The No Connect column shows pin differences for the XC2V40 and XC2V80 devices.

The FG256 pinout information (Table 4-2) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at http://www.xilinx.com).

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/DOUT	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		
5	IO_L01P_5/CS_B	T3		
6	IO_L01P_6	P1		
6	IO_L01N_6	N1		
6	IO_L02P_6/VRN_6	N3		
6	IO_L02N_6/VRP_6	N2		
6	IO_L03P_6	M4		
6	IO_L03N_6/VREF_6	M3		
6	IO_L04P_6	M2	NC	
6	IO_L04N_6	M1	NC	
6	IO_L06P_6	L4	NC	
6	IO_L06N_6	L3	NC	
6	IO_L43P_6	L2	NC	NC
6	IO_L43N_6	L1	NC	NC
6	IO_L45P_6	L5	NC	NC
6	IO_L45N_6/VREF_6	K5	NC	NC
6	IO_L91P_6	K4	NC	
6	IO_L91N_6	K3	NC	

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	IO_L93P_6	K2	NC	
6	IO_L93N_6/VREF_6	K1	NC	
6	IO_L94P_6	J4		
6	IO_L94N_6	J3		
6	IO_L96P_6	J2		
6	IO_L96N_6	J1		
7	IO_L96P_7	H1		
7	IO_L96N_7	H2		
7	IO_L94P_7	H3		
7	IO_L94N_7	H4		
7	IO_L93P_7/VREF_7	G1	NC	
7	IO_L93N_7	G2	NC	
7	IO_L91P_7	G3	NC	
7	IO_L91N_7	G4	NC	
7	IO_L45P_7/VREF_7	G5	NC	NC
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		

Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		

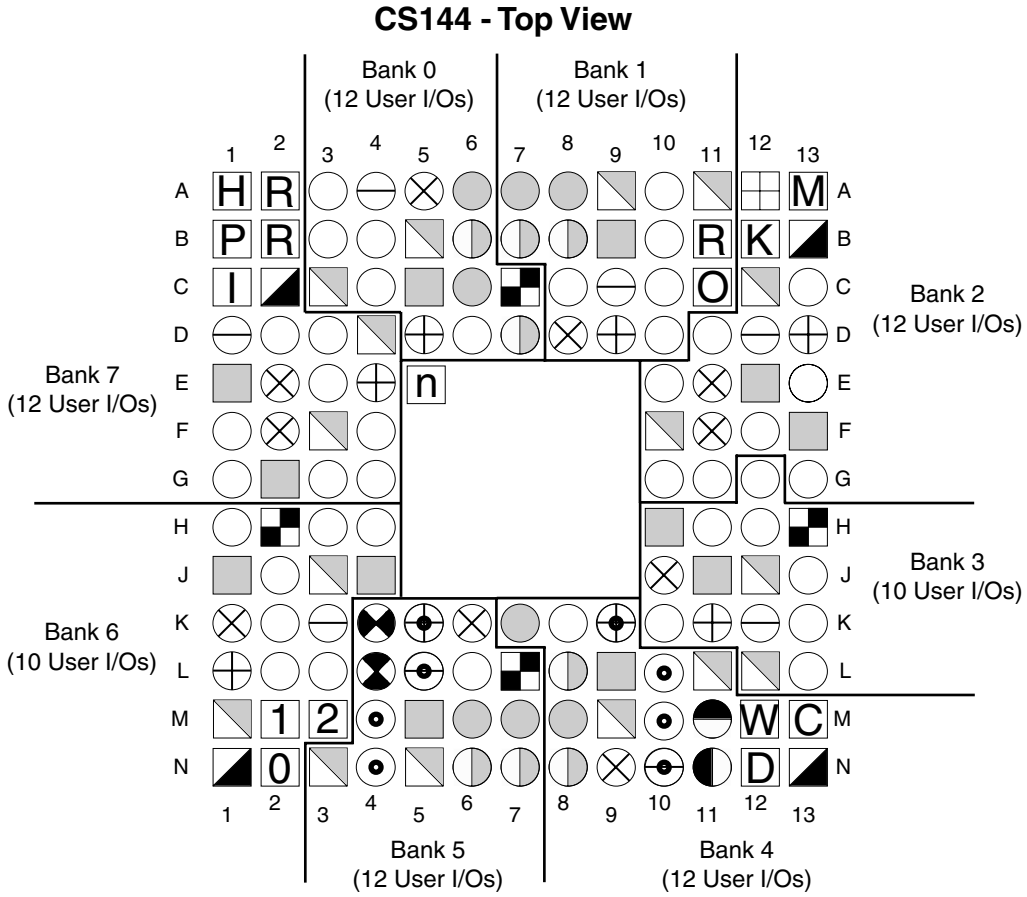
Table 4-2: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

Pinout Diagrams

This section contains pinout diagrams for the following Virtex-II packages:

CS144 Chip-Scale BGA Composite Pinout Diagram

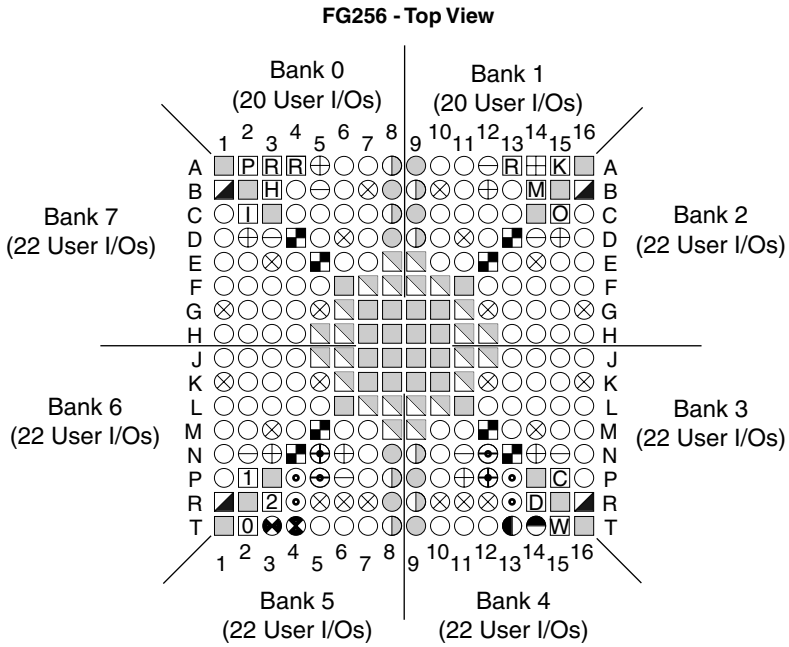


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	C CCLK	⊞ VBATT
Dual-Purpose Pins:	P PROG_B	R RSVD
⊙ DIN/D0-D7	D DONE	▨ VCCO
⊠ CS_B	2 1 0 M2, M1, M0	◪ VCCAUX
⊠ RDWR_B	H HSWAP_EN	▪ VCCINT
◓ BUSY/DOUT	K TCK	▩ GND
◐ INIT_B	I TDI	n NO CONNECT
● GCLKx (P)	O TDO	
◑ GCLKx (S)	M TMS	
⊖ VRP	W PWRDWN_B	
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_46_031501

Figure 4-1: **CS144 Chip-Scale BGA Composite Pinout Diagram**

FG256 Fine-Pitch BGA Composite Pinout Diagram



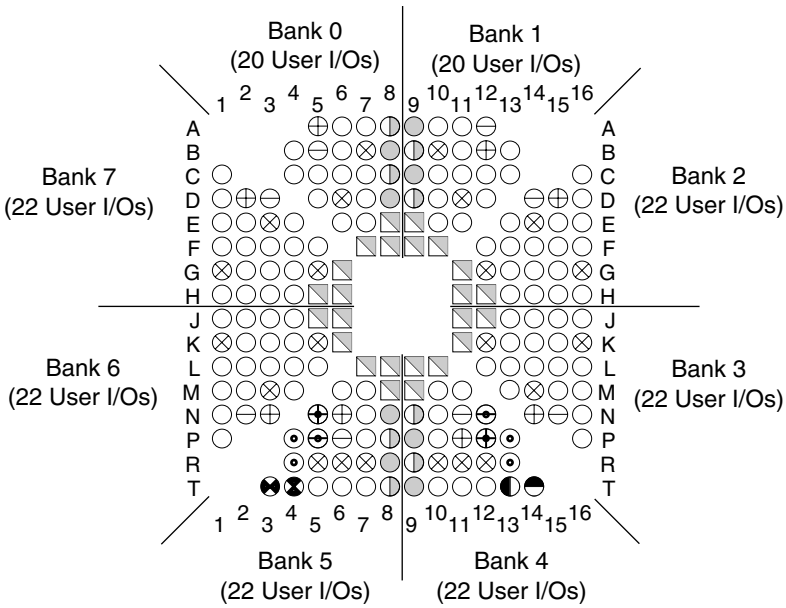
User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK		
Dual-Purpose Pins:		P	PROG_B		
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊠	CS_B	2 1 0	M2, M1, M0	R	RSVD
⧖	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◪	VCCAUX
◐	INIT_B	I	TDI	▪	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊙	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_47_031501

Figure 4-2: **FG256 Fine-Pitch BGA Composite Pinout Diagram**

FG256 Bank Information

FG256 - Top View



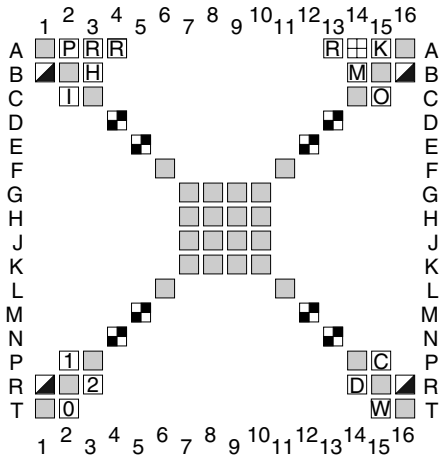
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
Dual-Purpose Pins:		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▨ VCCO
◓ BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◑ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_47b_031501

Figure 4-3: **FG256 Bank Information**

FG256 Dedicated Pins

FG256 - Top View

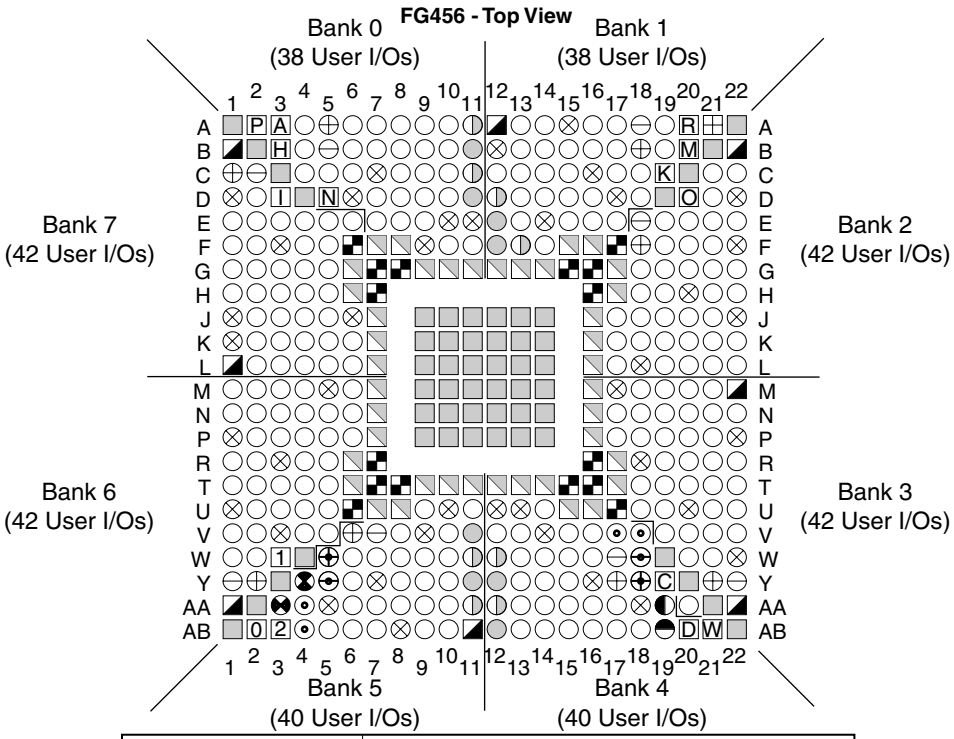


User I/O Pins	Dedicated Pins	
	C CCLK	
	P PROG_B	
	D DONE	⊞ VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	◪ VCCAUX
	I TDI	◪ VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_47c_120400

Figure 4-4: **FG256 Dedicated Pins**

FG456 Fine-Pitch BGA Composite Pinout Diagram



User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊗	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊗	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◢	VCCAUX
◐	INIT_B	I	TDI	▚	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊖	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_48_031501

Figure 4-5: **FG456 Fine-Pitch BGA Composite Pinout Diagram**

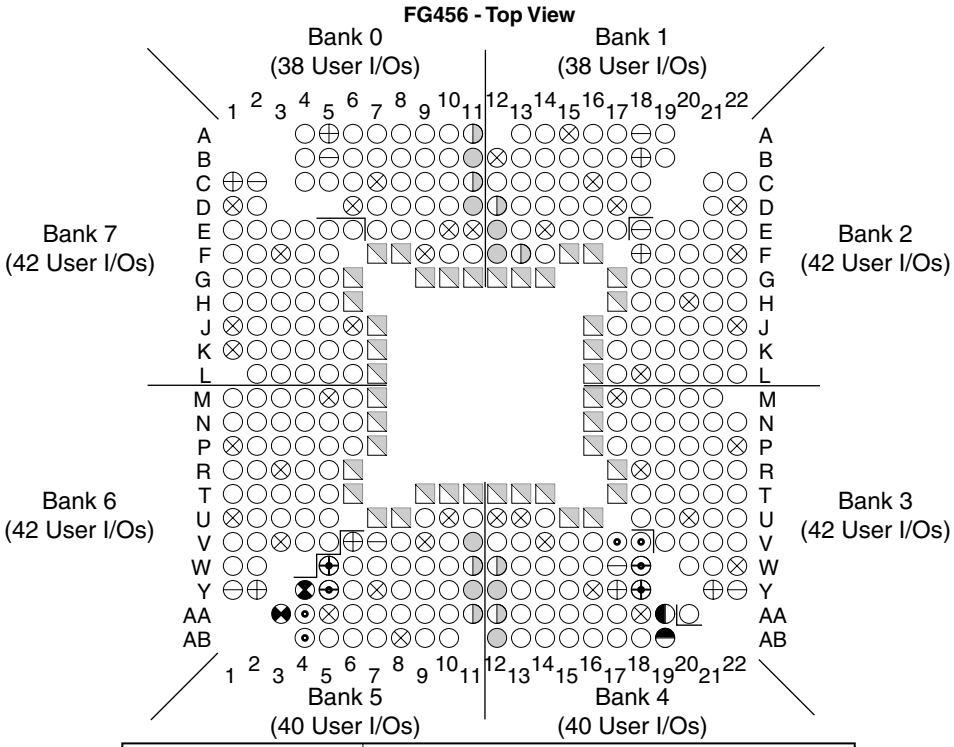
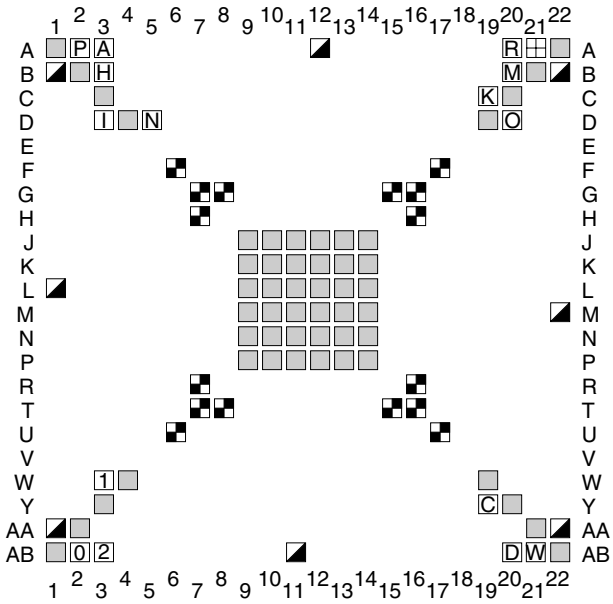


Figure 4-6: **FG456 Bank Information**

FG456 - Top View

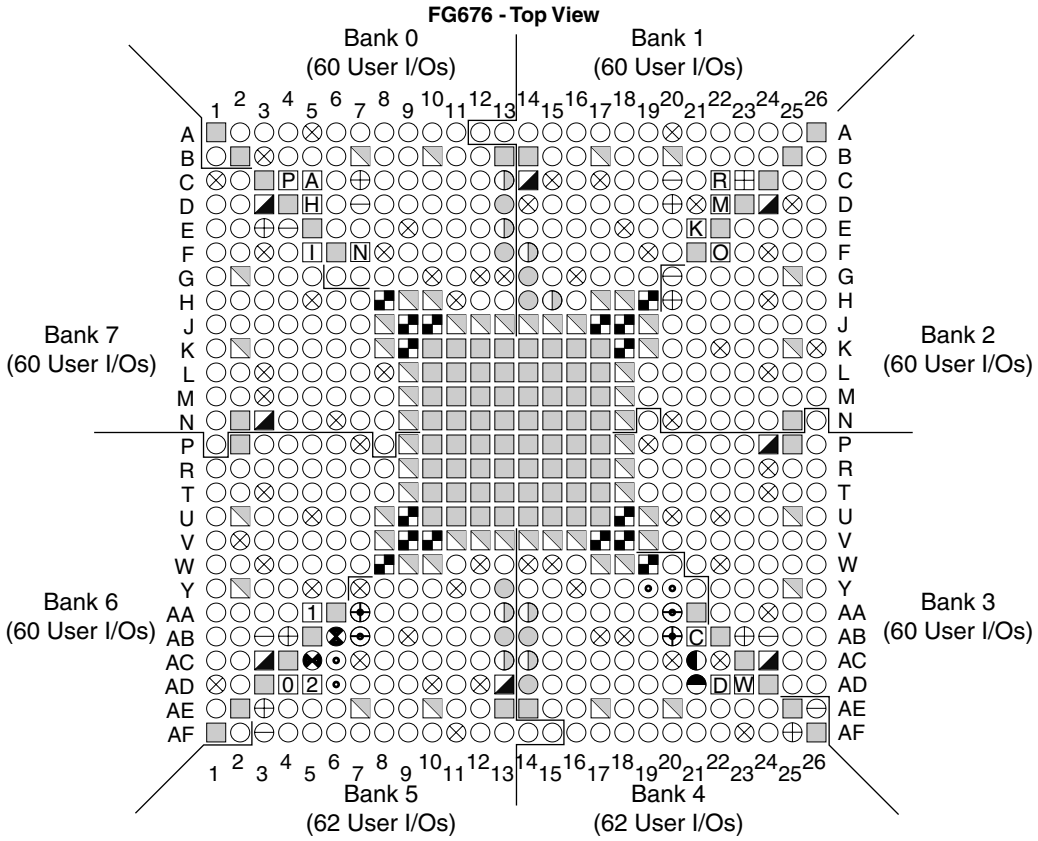


User I/O Pins	Dedicated Pins			
	C	CCLK	N	DXN
	P	PROG_B	A	DXP
	D	DONE		VBATT
	2 1 0	M2, M1, M0	R	RSVD
	H	HSWAP_EN		
	K	TCK		VCCAUX
	I	TDI		VCCINT
	O	TDO		GND
	M	TMS	n	NO CONNECT
	W	PWRDWN_B		

ug002_c4_48c_120400

Figure 4-7: **FG456 Dedicated Pins**

FG676 Fine-Pitch BGA Composite Pinout Diagram

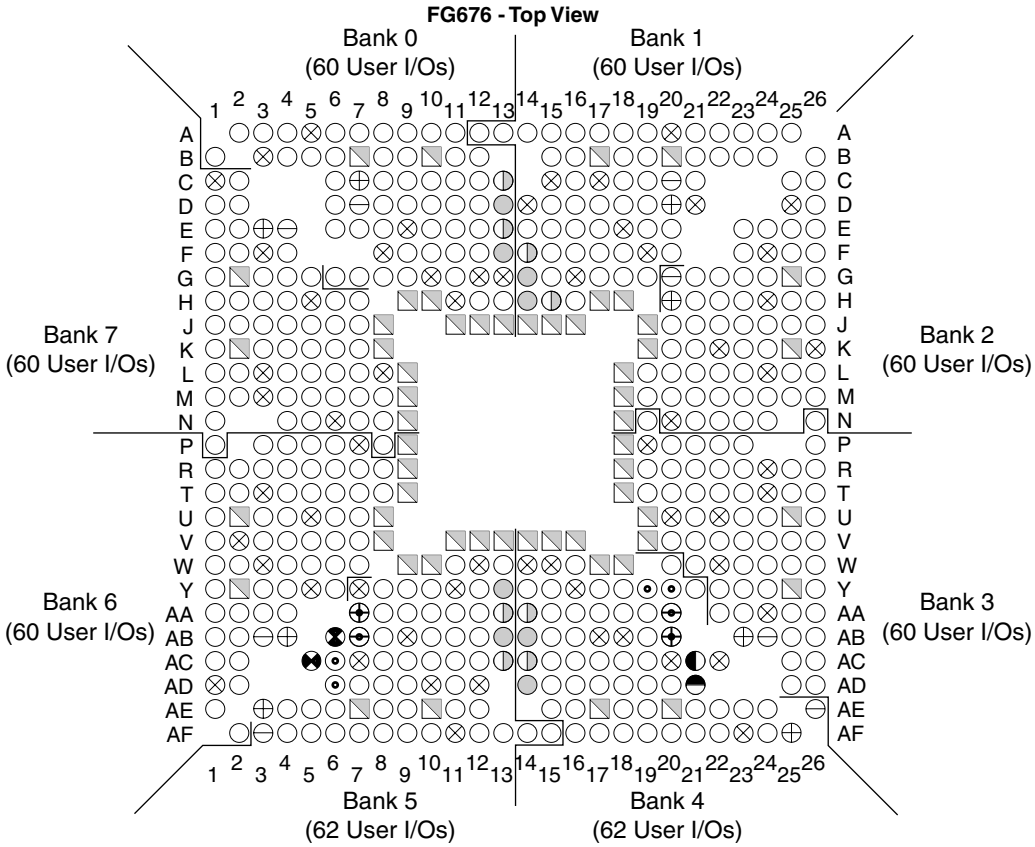


User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊗	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊗	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◪	VCCAUX
◐	INIT_B	I	TDI	▩	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊛	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_49_031501

Figure 4-8: **FG676 Fine-Pitch BGA Composite Pinout Diagram**

FG676 Bank Information

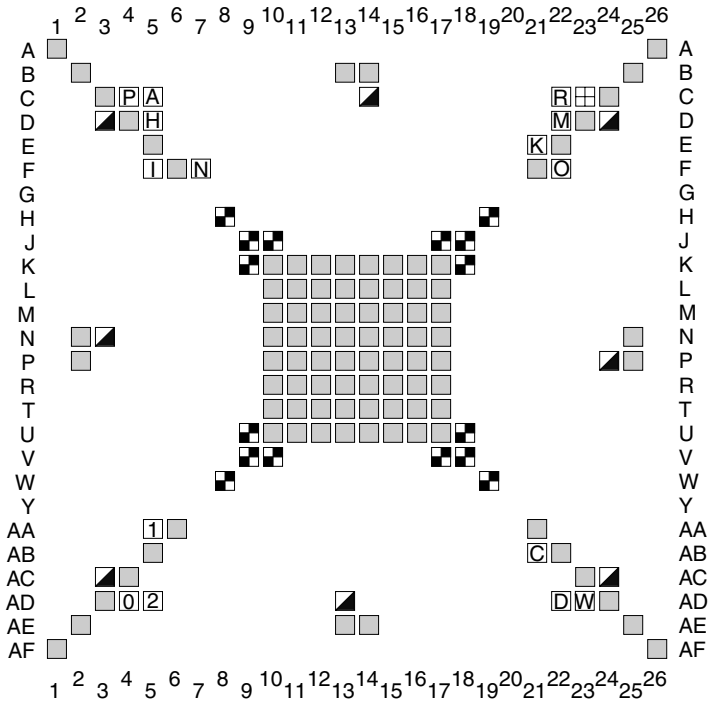


User I/O Pins	Dedicated Pins	
IO_LXXY_#		
Dual-Purpose Pins:		
DIN/D0-D7		
CS_B		
RDWR_B		VCCO
BUSY/DOUT		
INIT_B		
GCLKx (P)		
GCLKx (S)		
VRP		
VRN		
VREF		
Triple-Purpose Pins:		
D2, D4/ALT_VRP		
D3, D5/ALT_VRN		

ug002_c4_49b_031501

Figure 4-9: **FG676 Bank Information**

FG676 - Top View

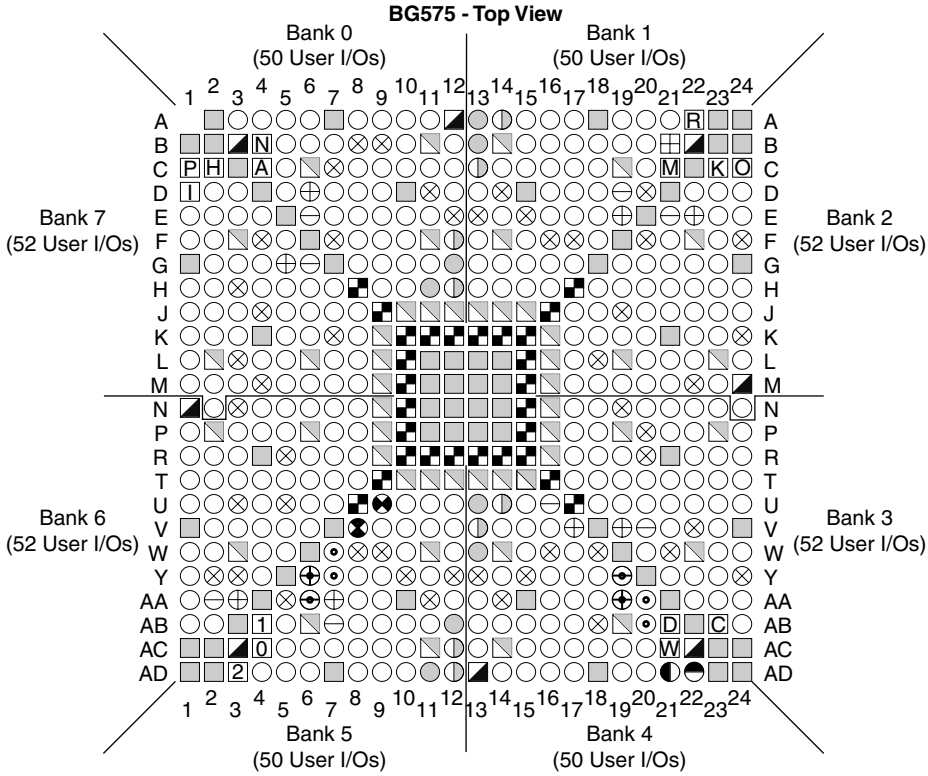


User I/O Pins	Dedicated Pins	
	C CCLK	N DXN
	P PROG_B	A DXP
	D DONE	VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	VCCAUX
	I TDI	VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_49c_120400

Figure 4-10: **FG676 Dedicated Pins**

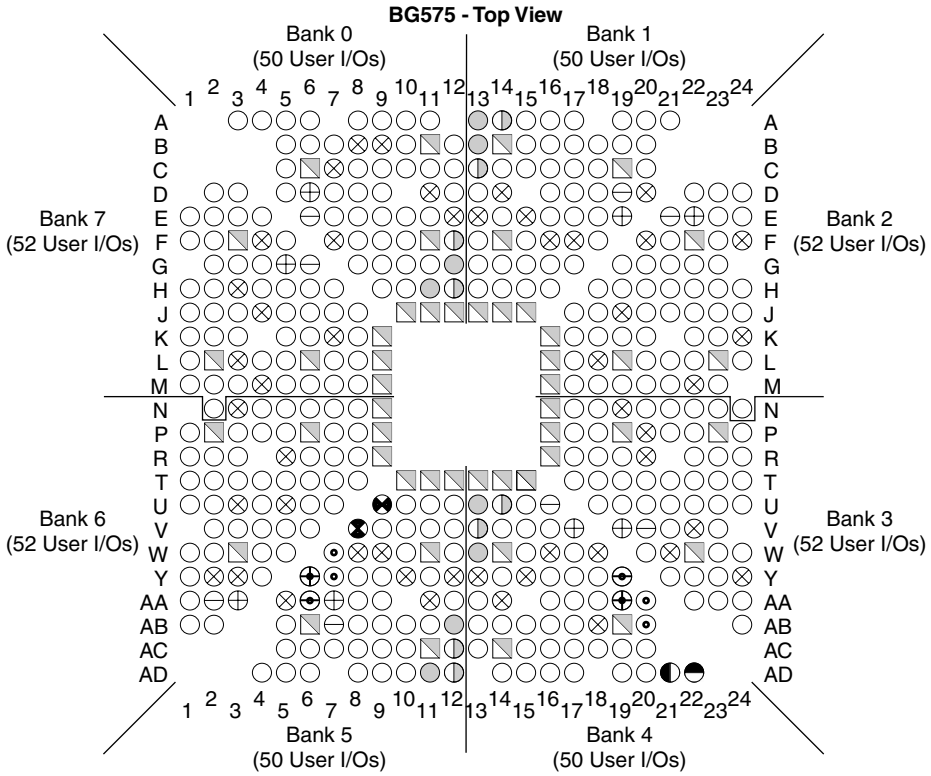
BG575 Standard BGA Composite Pinout Diagram



User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊗	CS_B	2 1 0	M2, M1, M0	R	RSVD
⧓	RDWR_B	H	HSWAP_EN	◹	VCCO
◓	BUSY/DOUT	K	TCK	◢	VCCAUX
◐	INIT_B	I	TDI	▞	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊖	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_50_031501

Figure 4-11: **BG575 Standard BGA Composite Pinout Diagram**

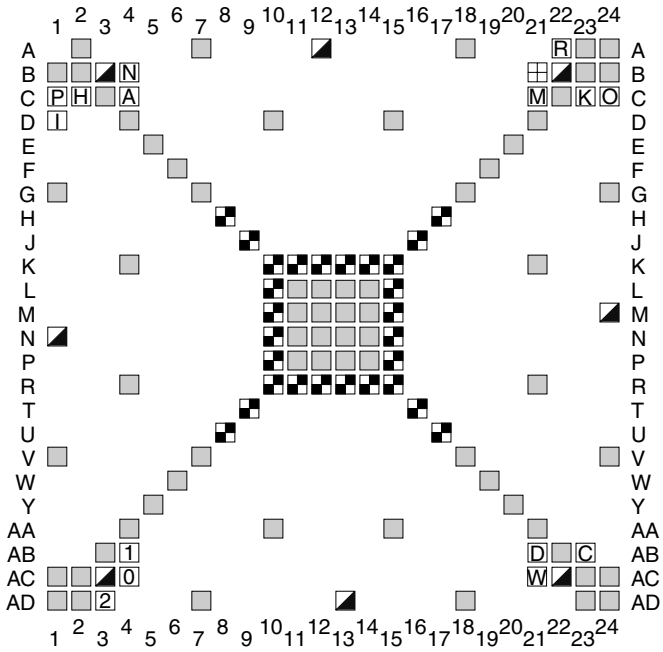


User I/O Pins		Dedicated Pins	
○	IO_LXXY_#		
Dual-Purpose Pins:			
⊙	DIN/D0-D7		
⊗	CS_B		
⊗	RDWR_B		▨ VCCO
◓	BUSY/DOUT		
◐	INIT_B		
●	GCLKx (P)		
◑	GCLKx (S)		
⊖	VRP		
⊕	VRN		
⊗	VREF		
Triple-Purpose Pins:			
⊖	D2, D4/ALT_VRP		
⊕	D3, D5/ALT_VRN		

ug002_c4_50b_031501

Figure 4-12: **BG575 Bank Information**

BG575 - Top View

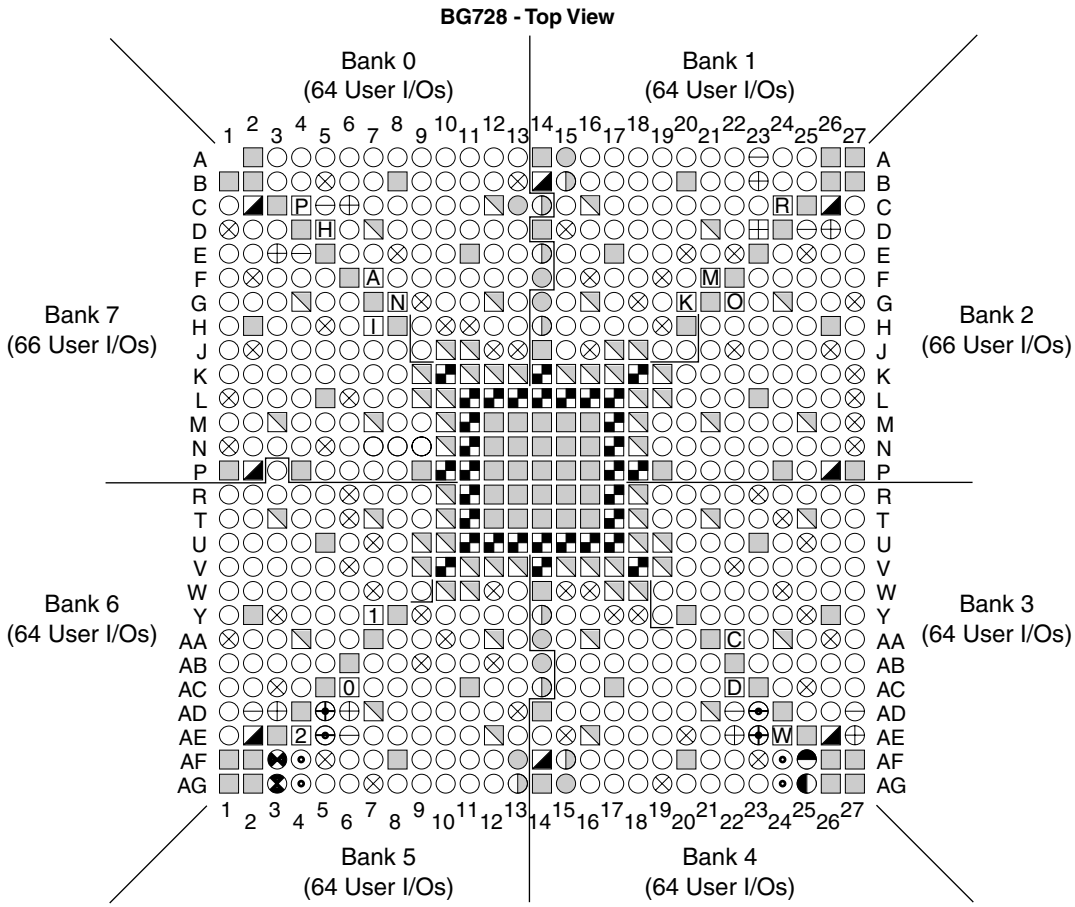


User I/O Pins	Dedicated Pins			
	C	CCLK	N	DXN
	P	PROG_B	A	DXP
	D	DONE		VBATT
	2 1 0	M2, M1, M0	R	RSVD
	H	HSWAP_EN		
	K	TCK		VCCAUX
	I	TDI		VCCINT
	O	TDO		GND
	M	TMS	n	NO CONNECT
	W	PWRDWN_B		

ug002_c4_50c_120400

Figure 4-13: **BG575 Dedicated Pins**

BG728 Standard BGA Composite Pinout Diagram

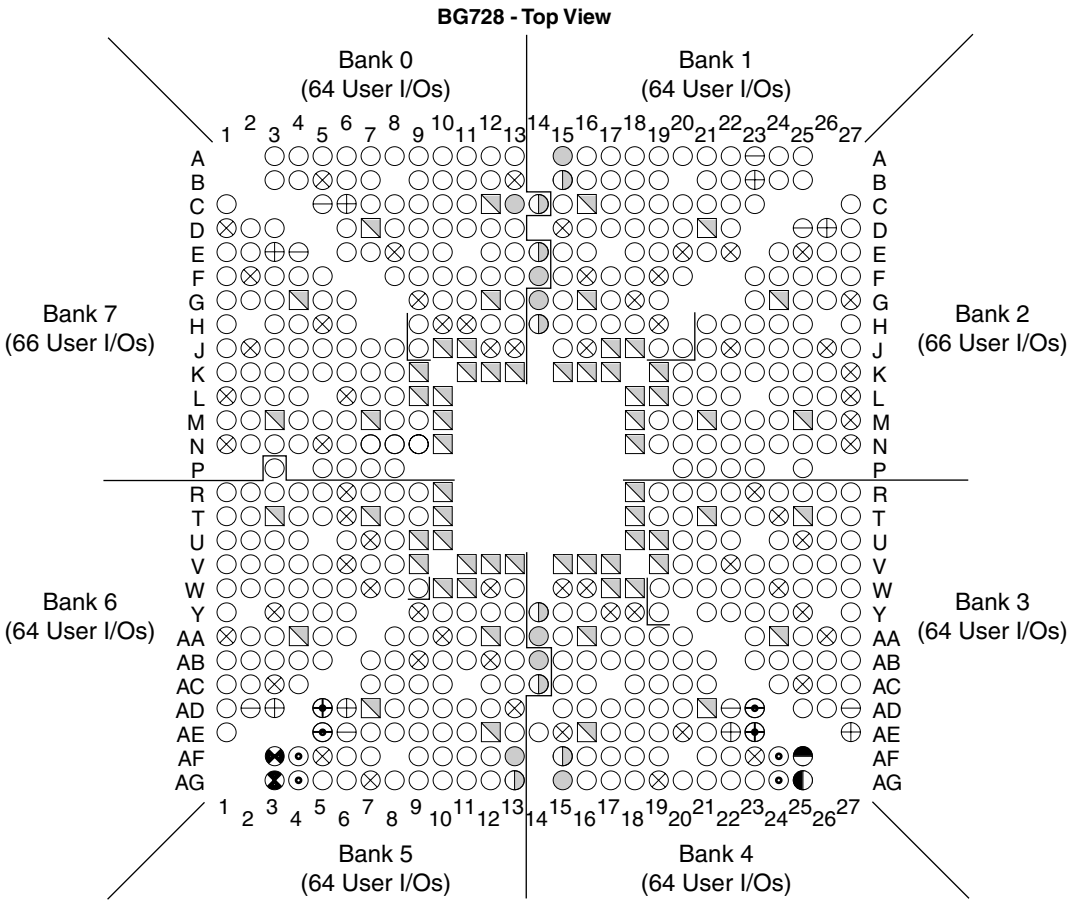


User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊠	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊠	RDWR_B	H	HSWAP_EN	▧	VCCO
◓	BUSY/DOUT	K	TCK	◢	VCCAUX
◐	INIT_B	I	TDI	▩	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊖	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_51_031501

Figure 4-14: **BG728 Standard BGA Composite Pinout Diagram**

BG728 Bank Information

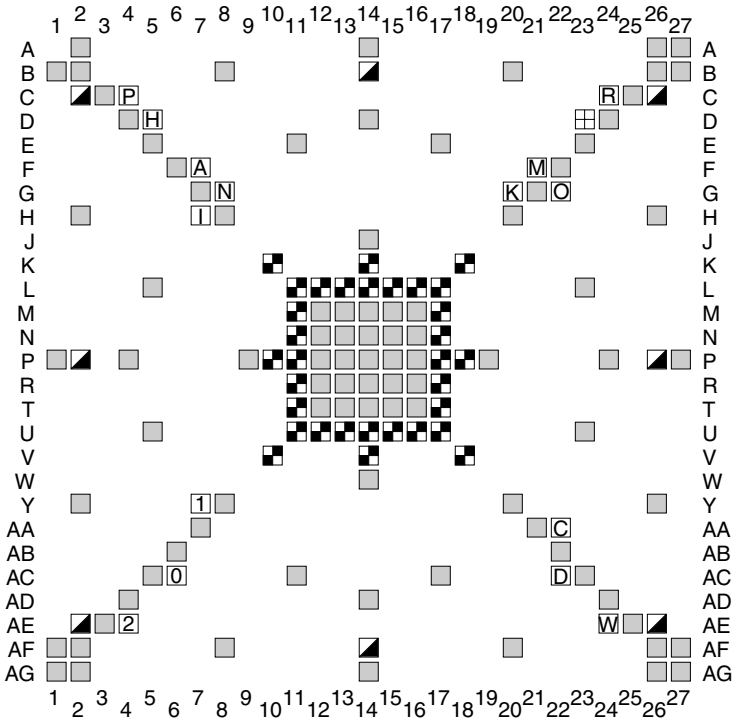


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
Dual-Purpose Pins:		
⊙ DIN/D0-D7		
CS_B		
RDWR_B		▨ VCCO
BUSY/DOUT		
INIT_B		
GCLKx (P)		
GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
D2, D4/ALT_VRP		
D3, D5/ALT_VRN		

ug002_c4_51b_031501

Figure 4-15: **BG728 Bank Information**

BG728 - Top View

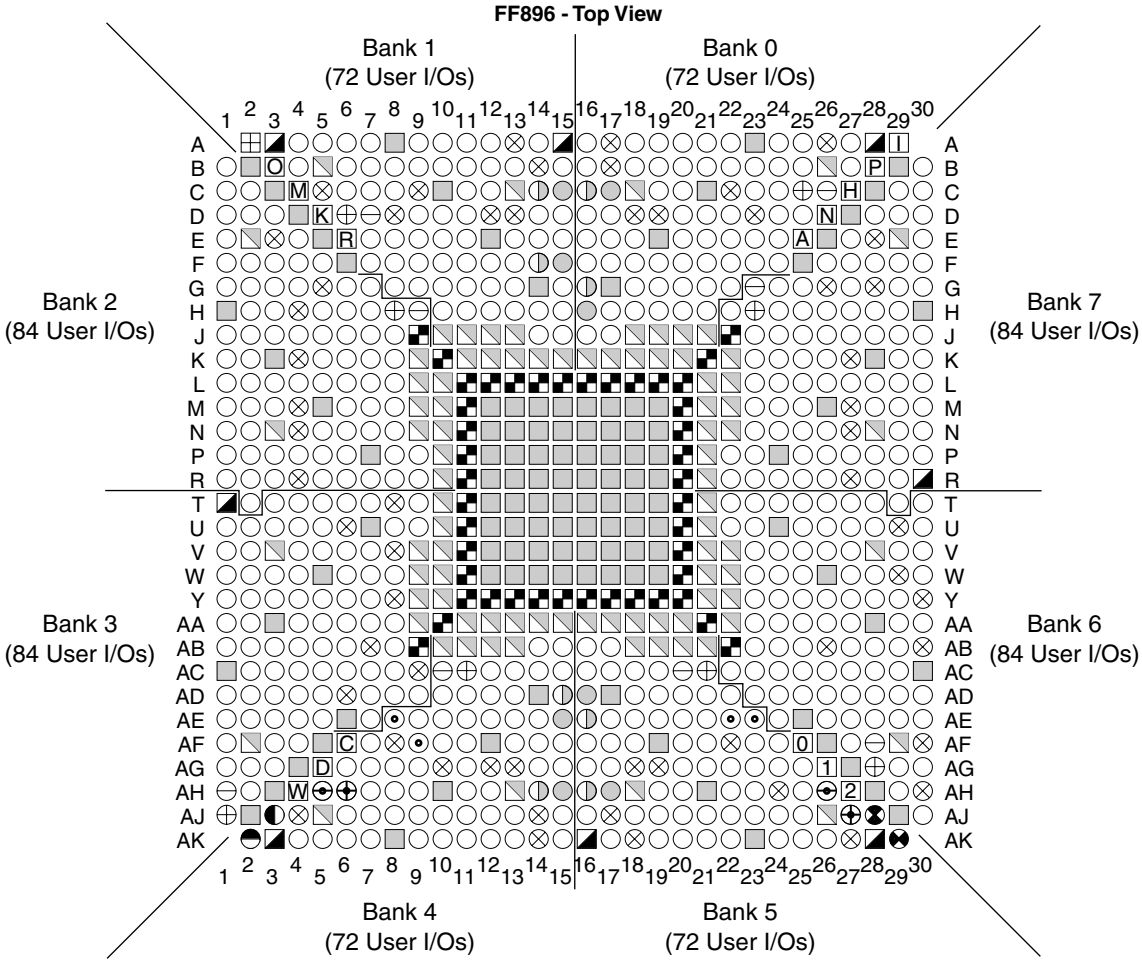


User I/O Pins	Dedicated Pins	
	C CCLK	N DXN
	P PROG_B	A DXP
	D DONE	VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	VCCAUX
	I TDI	VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_51c_120400

Figure 4-16: **BG728 Dedicated Pins**

FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

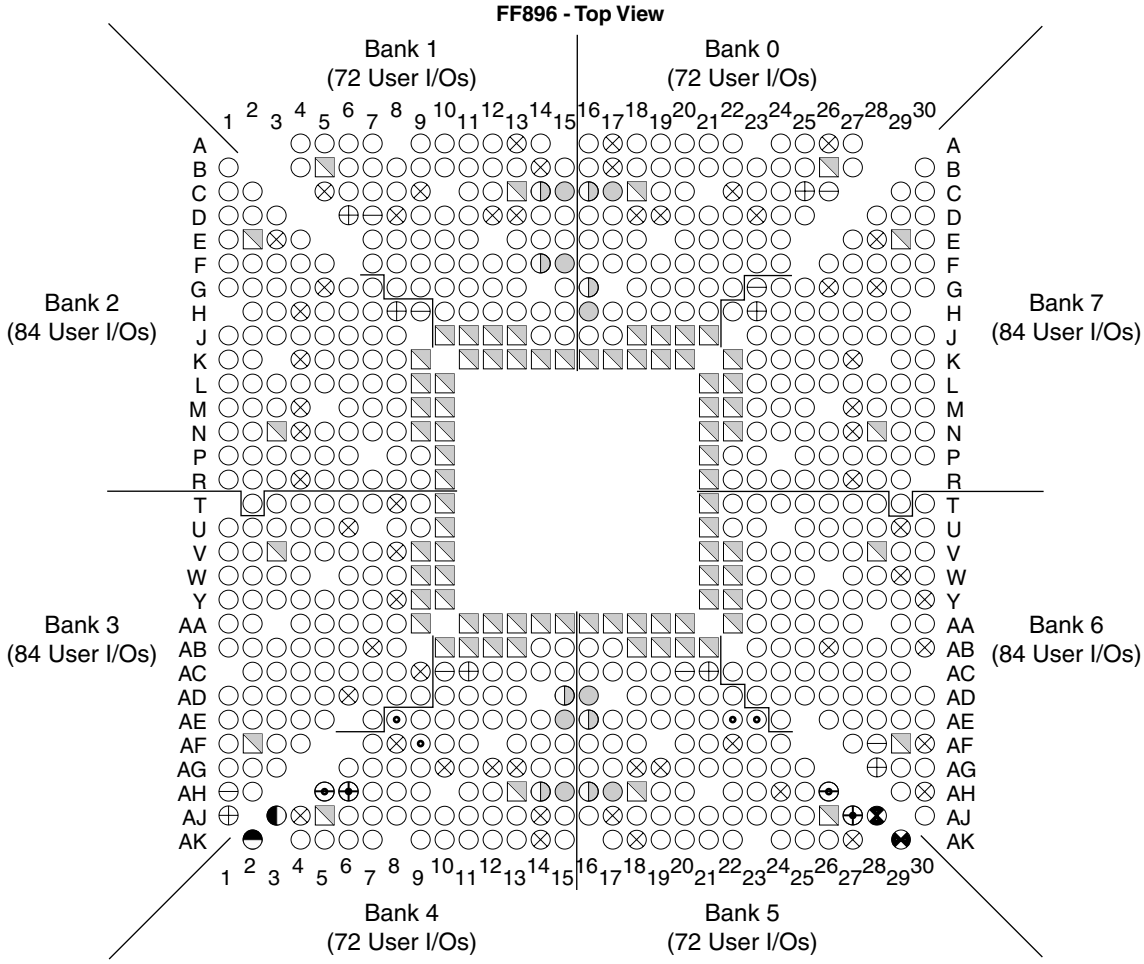


User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊠	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊗	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◪	VCCAUX
◐	INIT_B	I	TDI	▩	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊖	D2,D4/ALT_VRP				
⊕	D3,D5/ALT_VRN				

ug002_c4_52_031501

Figure 4-17: **FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

FF896 Bank Information

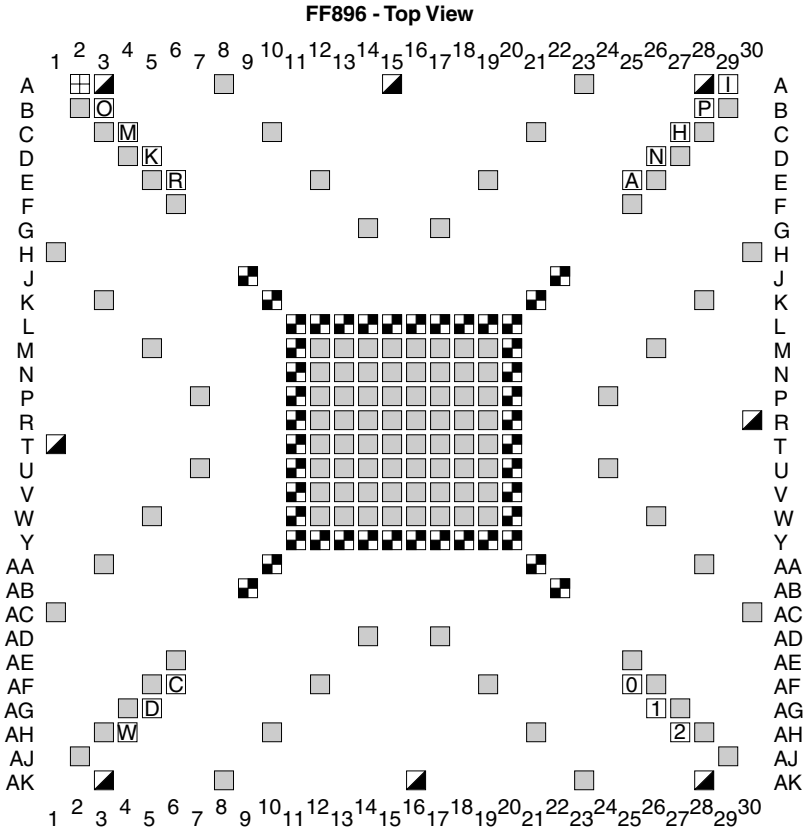


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
Dual-Purpose Pins:		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▨ VCCO
◓ BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◑ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_52b_031501

Figure 4-18: **FF896 Bank Information**

FF896 Dedicated Pins

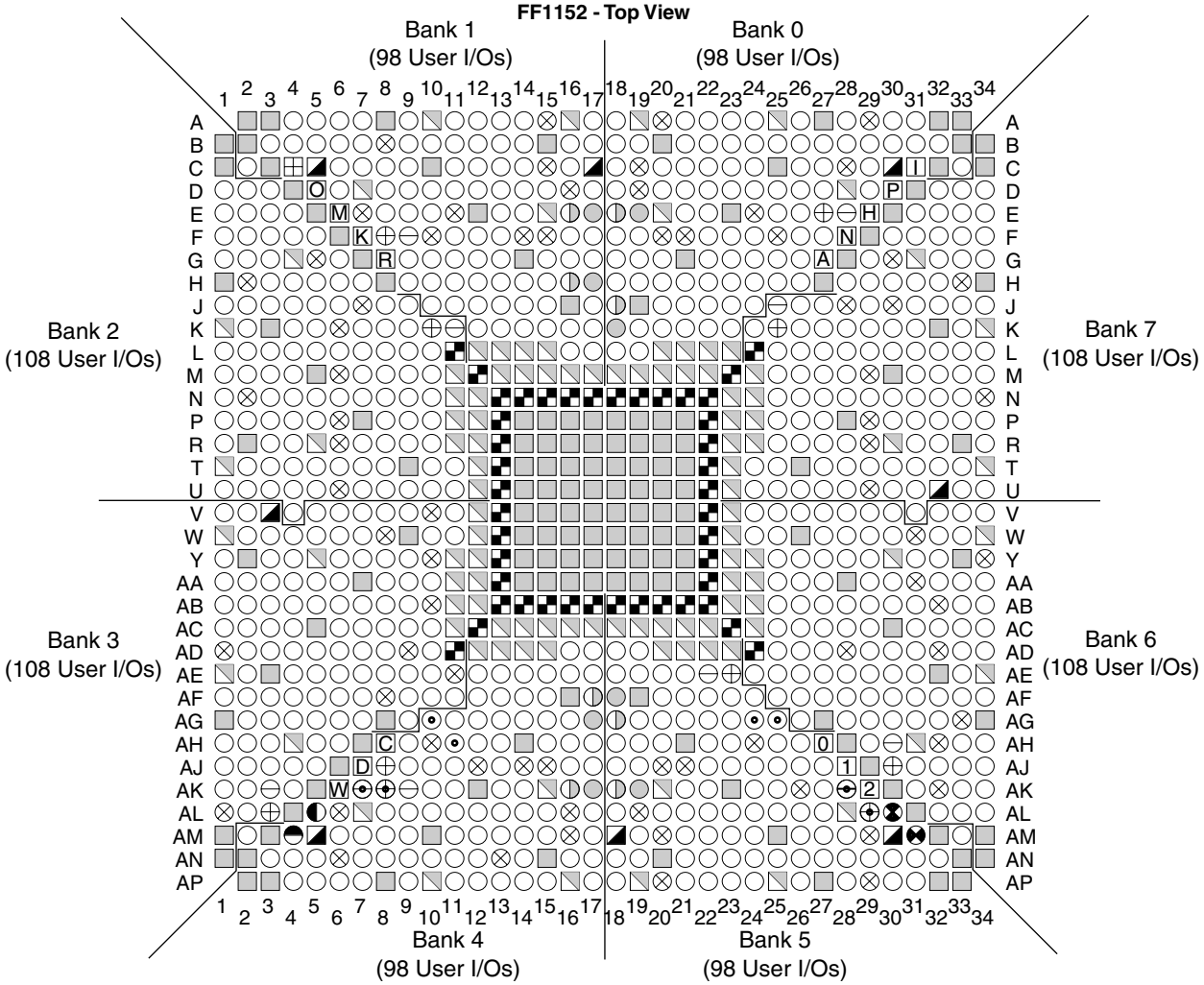


User I/O Pins	Dedicated Pins	
	C CCLK	N DXN
	P PROG_B	A DXP
	D DONE	VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	VCCAUX
	I TDI	VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_52c_120400

Figure 4-19: **FF896 Dedicated Pins**

FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

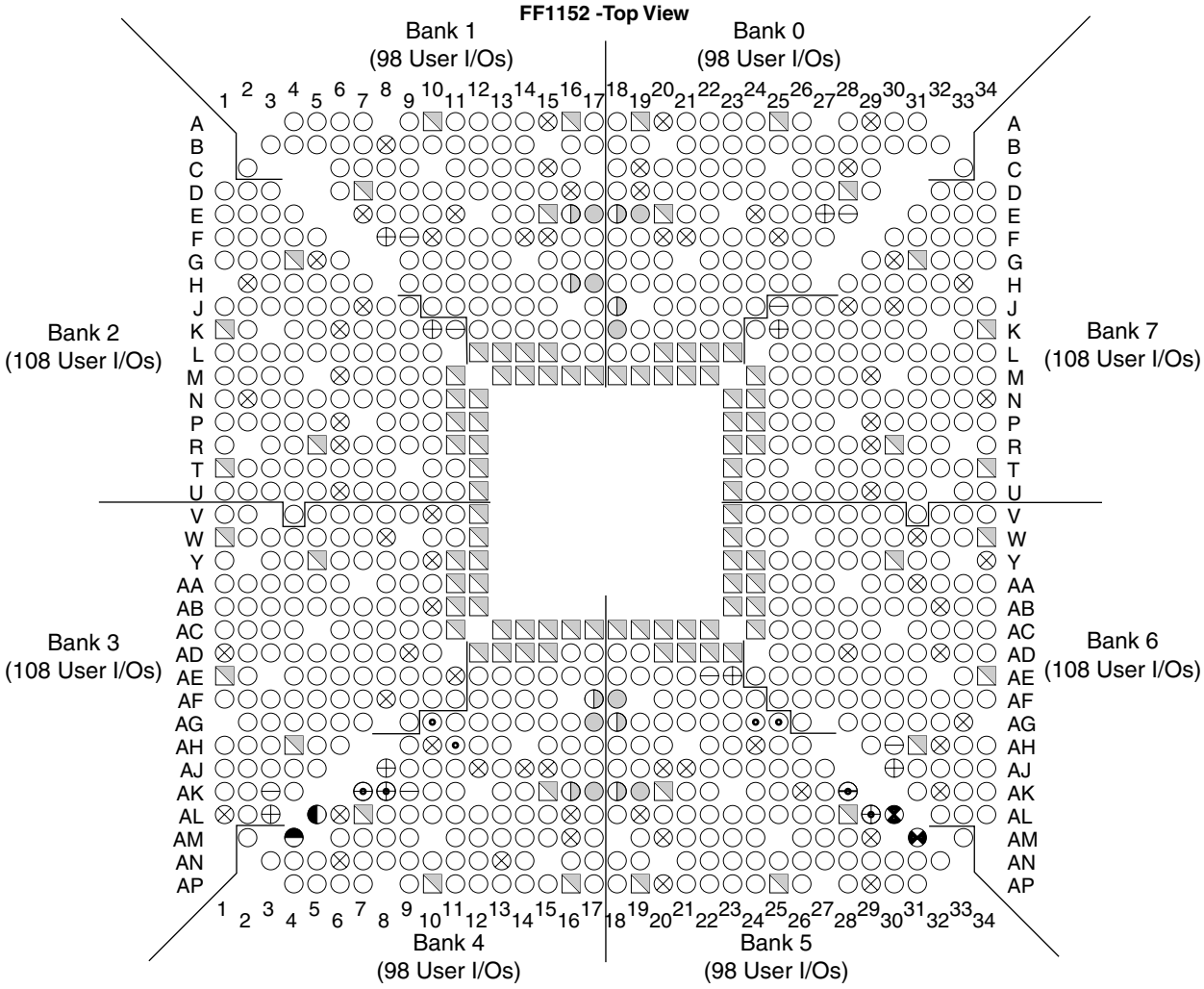


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	C CCLK	N DXN
Dual-Purpose Pins:	P PROG_B	A DXP
⊙ DIN/D0-D7	D DONE	⊞ VBATT
⊗ CS_B	2 1 0 M2, M1, M0	R RSVD
⊗ RDWR_B	H HSWAP_EN	▨ VCCO
◓ BUSY/DOUT	K TCK	◪ VCCAUX
◐ INIT_B	I TDI	▩ VCCINT
● GCLKx (P)	O TDO	■ GND
◑ GCLKx (S)	M TMS	n NO CONNECT
⊖ VRP	W PWRDWN_B	
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_53_031501

Figure 4-20: **FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

FF1152 Bank Information

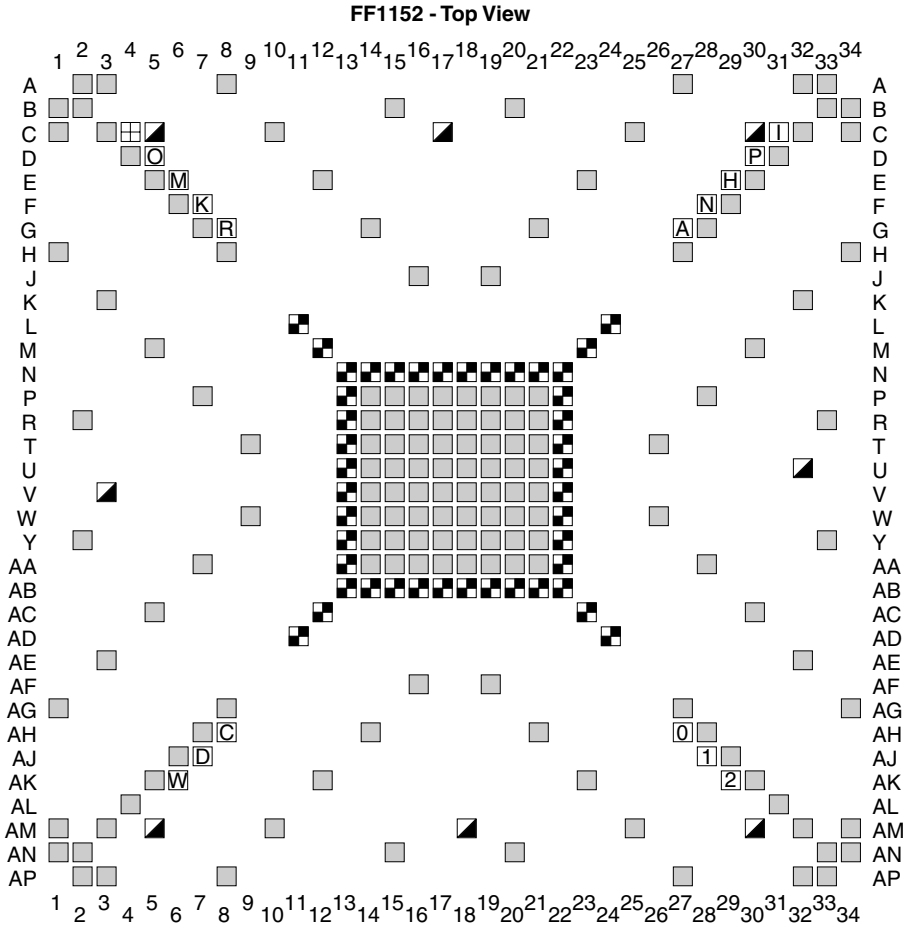


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
Dual-Purpose Pins:		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▨ VCCO
◓ BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◑ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_53b_031501

Figure 4-21: **FF1152 Bank Information**

FF1152 Dedicated Pins

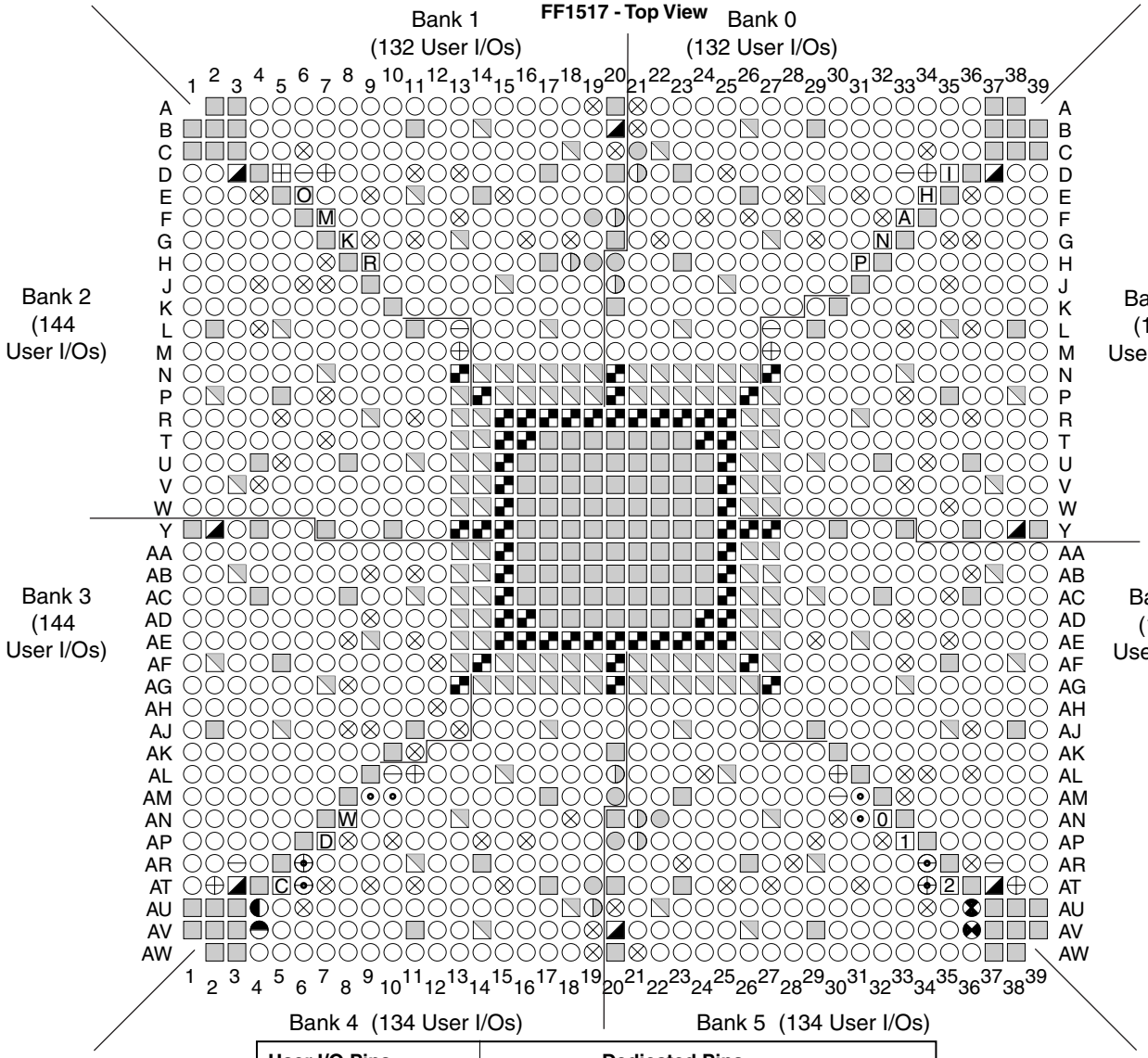


User I/O Pins	Dedicated Pins	
	C CCLK	N DXN
	P PROG_B	A DXP
	D DONE	VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	VCCAUX
	I TDI	VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_53c_120400

Figure 4-22: **FF1152 Dedicated Pins**

FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

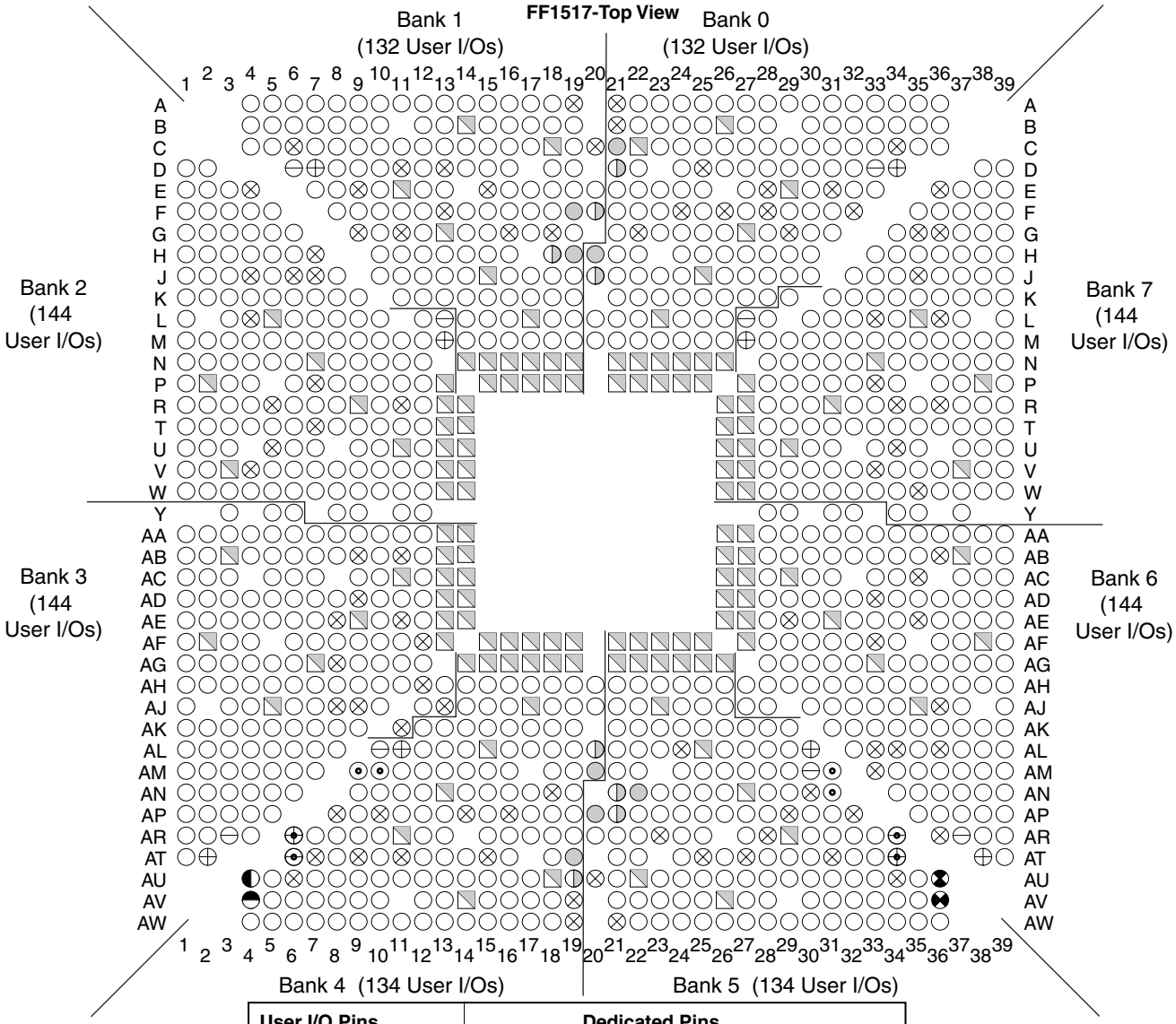


User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊗	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊗	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◪	VCCAUX
◐	INIT_B	I	TDI	▩	VCCINT
●	GCLKx (P)	O	TDO	■	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊛	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_45_031501

Figure 4-23: **FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

FF1517 Bank Information

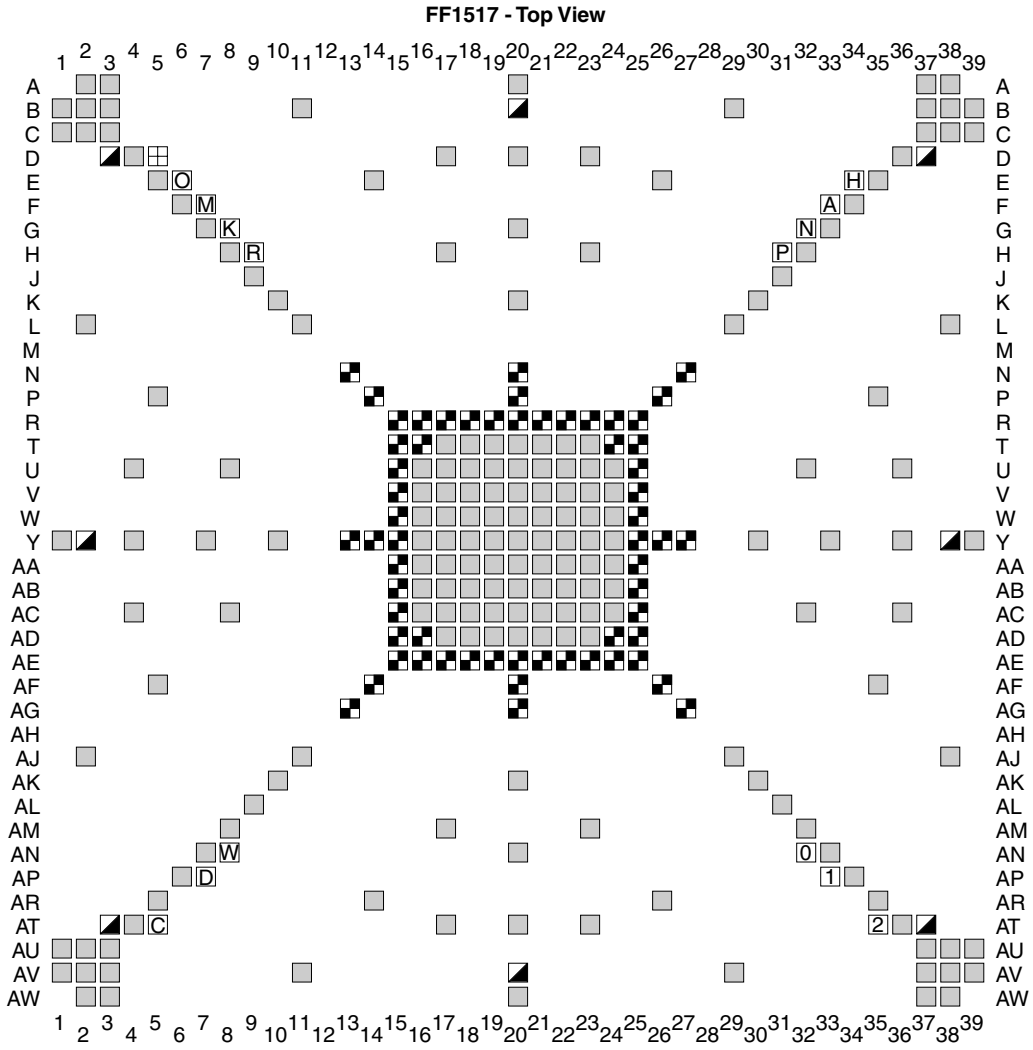


User I/O Pins	Dedicated Pins	
IO_LXXY_#		
Dual-Purpose Pins:		
DIN/D0-D7		
CS_B		
RDWR_B		VCCO
BUSY/DOUT		
INIT_B		
GCLKx (P)		
GCLKx (S)		
VRP		
VRN		
VREF		
Triple-Purpose Pins:		
D2, D4/ALT_VRP		
D3, D5/ALT_VRN		

ug002_c4_45b_031501

Figure 4-24: **FF1517 Bank Information**

FF1517 Dedicated Pins

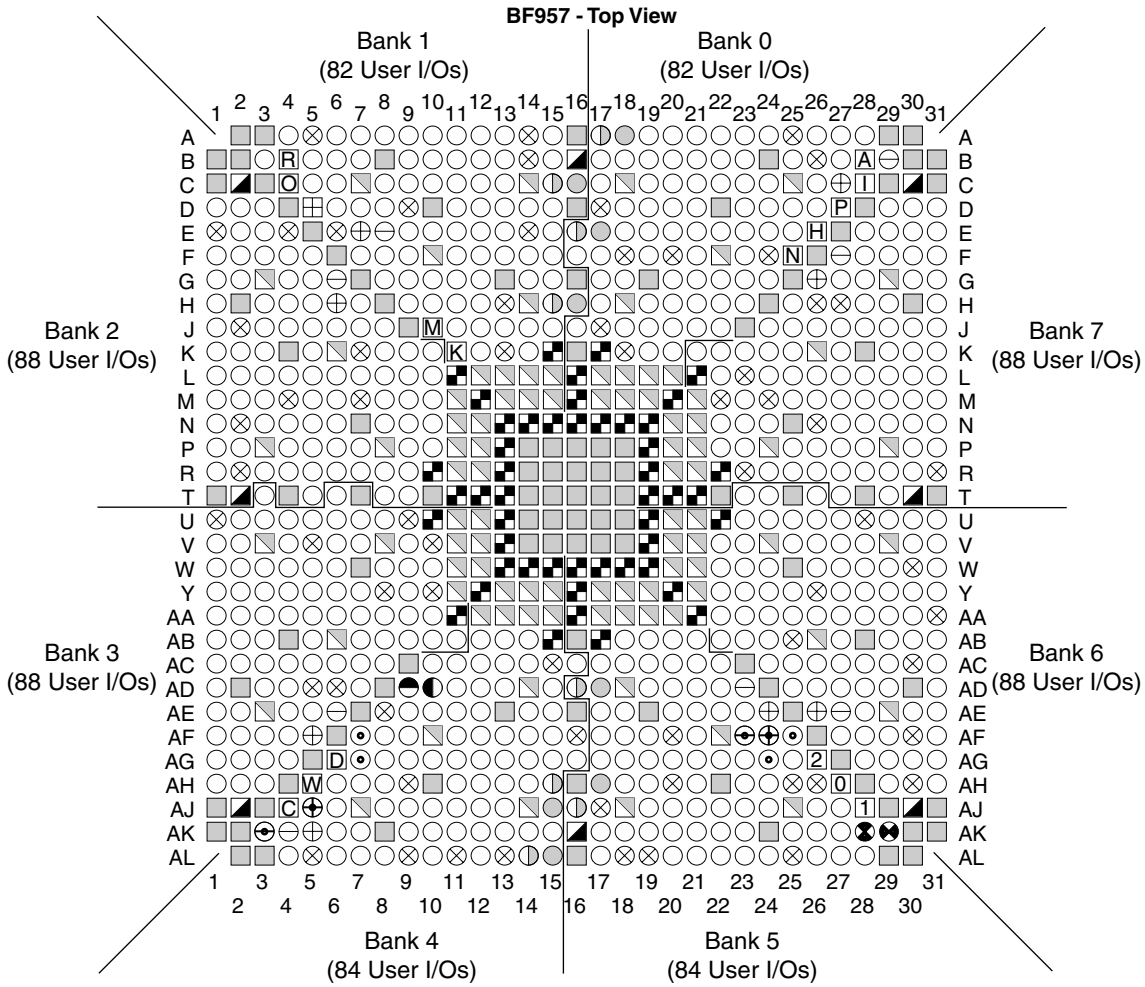


User I/O Pins	Dedicated Pins			
	C	CCLK	N	DXN
	P	PROG_B	A	DXP
	D	DONE		VBATT
	2 1 0	M2, M1, M0	R	RSVD
	H	HSWAP_EN		
	K	TCK		VCCAUX
	I	TDI		VCCINT
	O	TDO		GND
	M	TMS	n	NO CONNECT
	W	PWRDWN_B		

ug002_c4_45c_120400

Figure 4-25: **FF1517 Dedicated Pins**

BF957 Flip-Chip BGA Composite Pinout Diagram

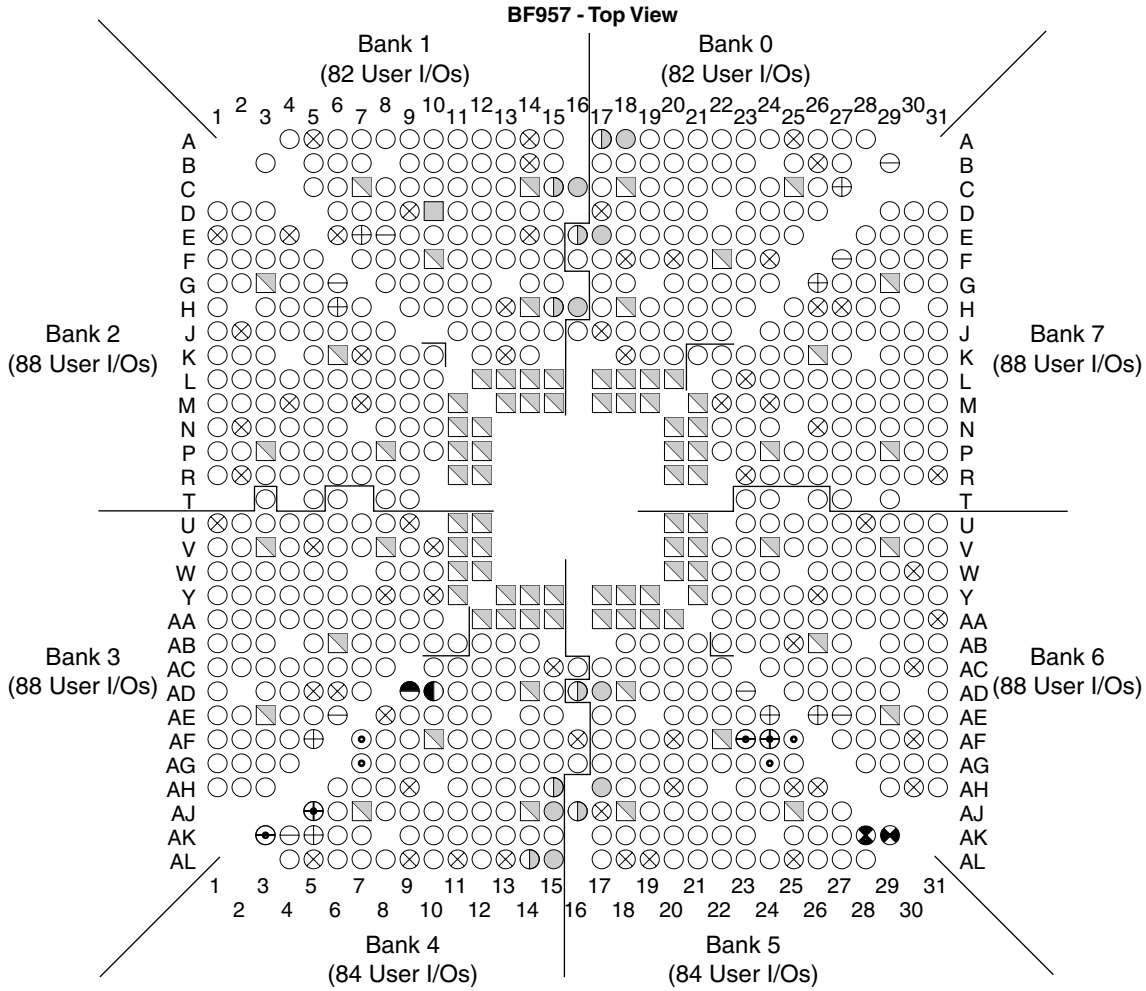


User I/O Pins		Dedicated Pins			
○	IO_LXXY_#	C	CCLK	N	DXN
Dual-Purpose Pins:		P	PROG_B	A	DXP
⊙	DIN/D0-D7	D	DONE	⊞	VBATT
⊗	CS_B	2 1 0	M2, M1, M0	R	RSVD
⊗	RDWR_B	H	HSWAP_EN	▨	VCCO
◓	BUSY/DOUT	K	TCK	◪	VCCAUX
◐	INIT_B	I	TDI	▩	VCCINT
●	GCLKx (P)	O	TDO	▨	GND
◑	GCLKx (S)	M	TMS	n	NO CONNECT
⊖	VRP	W	PWRDWN_B		
⊕	VRN				
⊗	VREF				
Triple-Purpose Pins:					
⊖	D2, D4/ALT_VRP				
⊕	D3, D5/ALT_VRN				

ug002_c4_54_032901

Figure 4-26: **BF957 Flip-Chip BGA Composite Pinout Diagram**

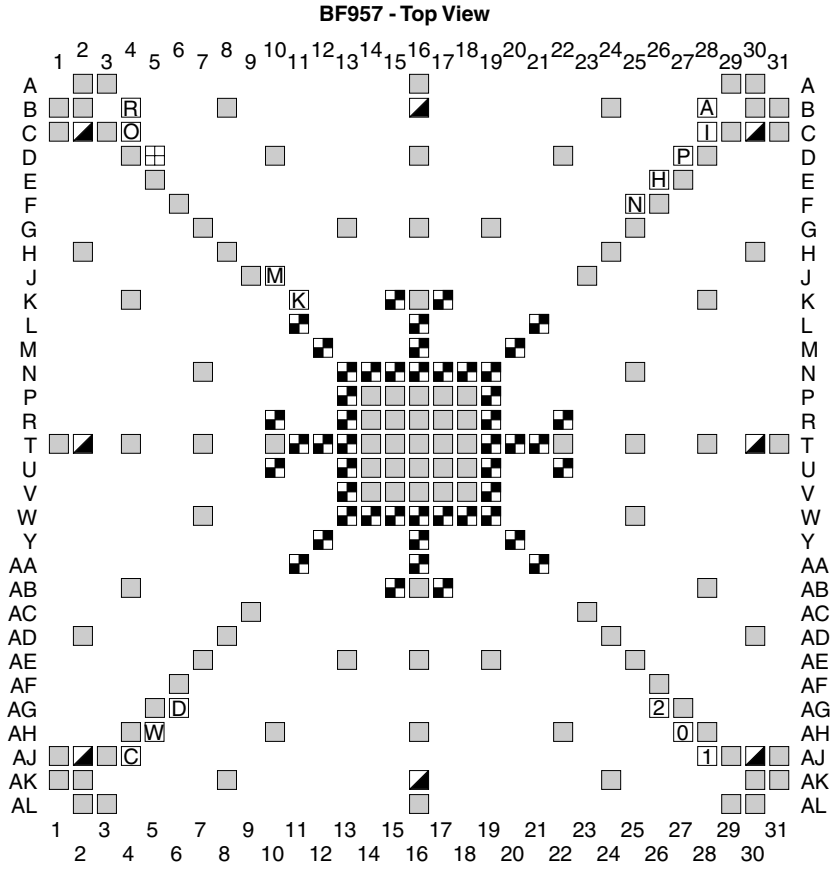
BF957 Bank Information



User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
Dual-Purpose Pins:		
⊙ DIN/D0-D7		
⊗ CS_B		
⧗ RDWR_B		▨ VCCO
◓ BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◑ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊖ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

ug002_c4_54b_032901

Figure 4-27: **BF957 Bank Information**



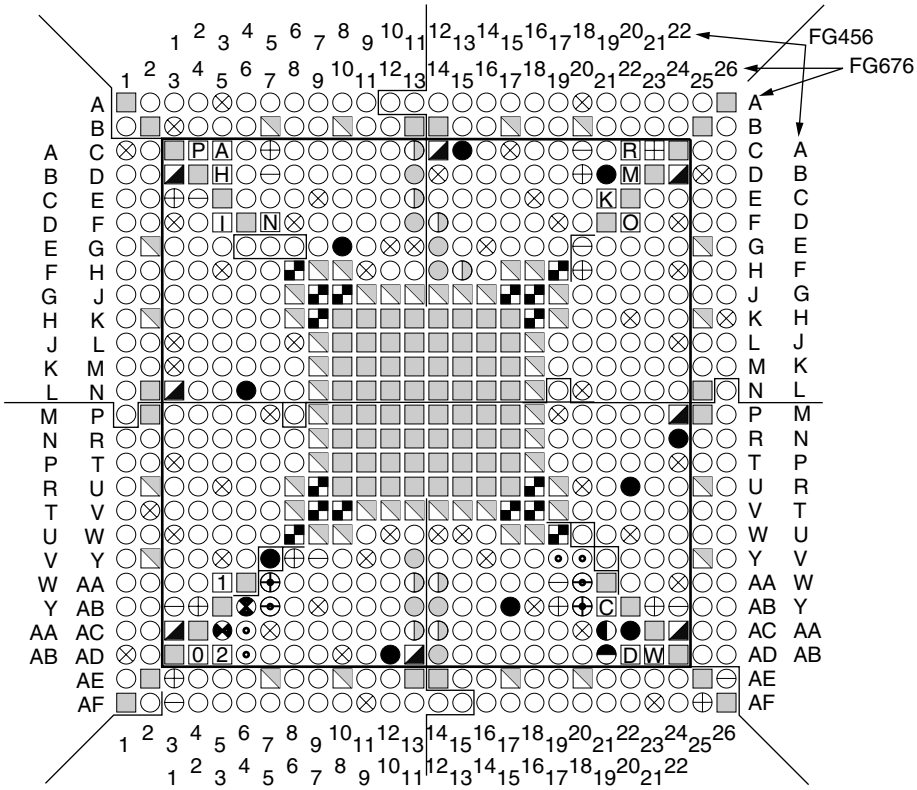
User I/O Pins	Dedicated Pins	
	C CCLK	N DXN
	P PROG_B	A DXP
	D DONE	VBATT
	2 1 0 M2, M1, M0	R RSVD
	H HSWAP_EN	
	K TCK	VCCAUX
	I TDI	VCCINT
	O TDO	GND
	M TMS	n NO CONNECT
	W PWRDWN_B	

ug002_c4_54c_120400

Figure 4-28: **BF957 Dedicated Pins**

FG456 - FG676 Pinout Compatibility Diagram

FG676/FG456 Pinout Compatible Diagram - Top View



Note: FF456 and FG676 are pinout compatible with with the exception of the LVDS pairs. I/O V_{REF} pins in FG676 are user I/O pins in FG456. In addition, some user I/O pins are not in the same bank (see ◯◯ lines). VRP (V7) and VRN (V6) in Bank 5 and VRP (W17) and VRN (Y17) in Bank 4 are only user I/Os in FG676.

User I/O Pins	Dedicated Pins	
◯ IO_LXXY_#	C CCLK	N DXN
Dual-Purpose Pins:	P PROG_B	A DXP
⊙ DIN/D0-D7	D DONE	⊞ VBATT
⊗ CS_B	2 1 0 M2, M1, M0	R RSVD
⊗ RDWR_B	H HSWAP_EN	▨ VCCO
◓ BUSY/DOUT	K TCK	◪ VCCAUX
◐ INIT_B	I TDI	▩ VCCINT
● GCLKx (P)	O TDO	■ GND
◑ GCLKx (S)	M TMS	n NO CONNECT
⊖ VRP	W PWRDWN_B	
⊕ VRN		
⊗ VREF		
● VREF on FG676 User I/O on FG456		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

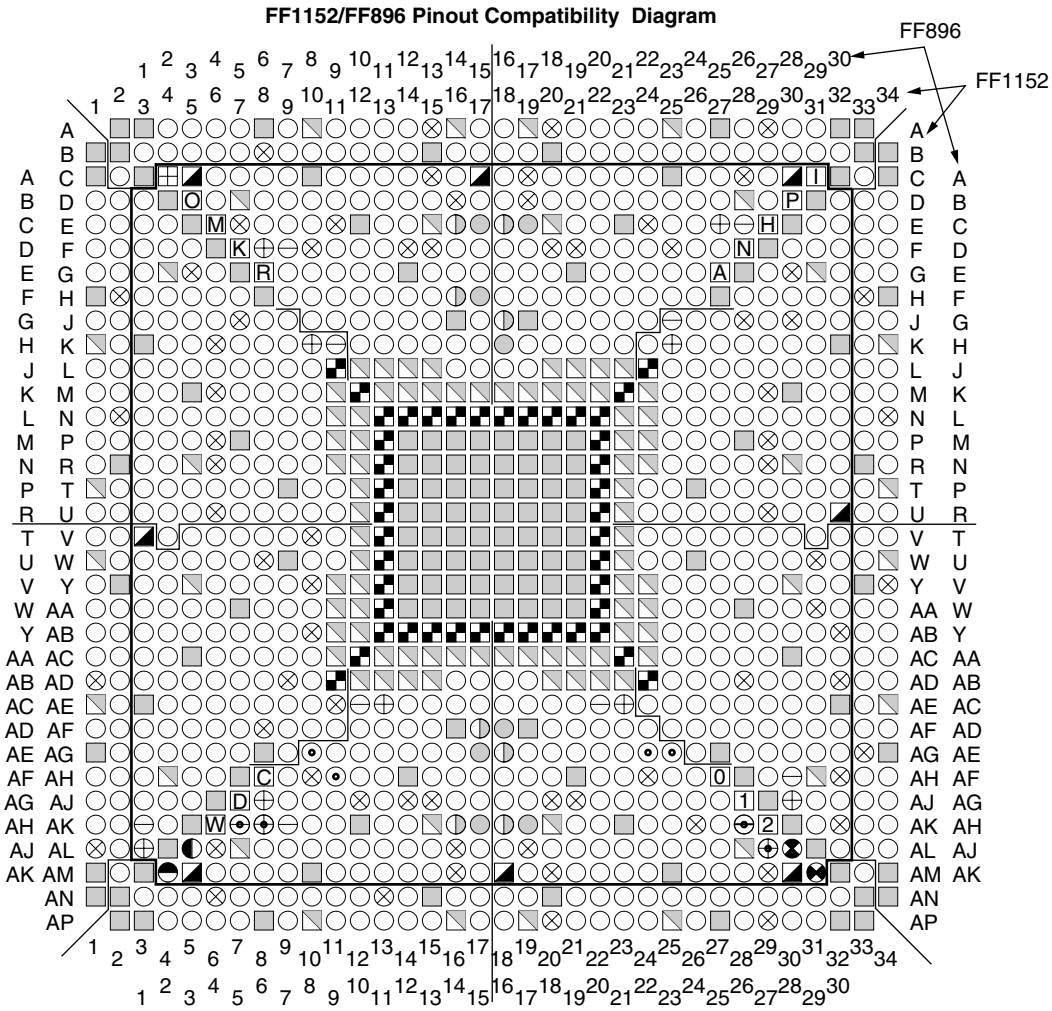
Corresponding Pinouts

FG456	FG676
A1	C3
.	.
.	.
.	.
.	.
.	.
AB22	AD24

ug002_c4_56_080601

Figure 4-29: **FG456 - FG676 Pinout Compatibility Diagram**

FF896 - FF1152 Pinout Compatibility Diagram



Note: FF896 is pinout compatible with the FF1152 except for LVDS pairs. Also, in Bank 4, VRP/VRN pins are not compatible: for FF896, VRP is in AC10 and VRN is in AC11, and for FF1152, VRP is in AK9 and VRN is in AJ8. If DCI is not used in Bank 4, or is used with ALT_VRP or ALT_VRN, then the user I/Os are compatible.

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	C CCLK	N DXN
Dual-Purpose Pins:	P PROG_B	A DXP
⊙ DIN/D0-D7	D DONE	⊞ VBATT
⊠ CS_B	2 1 0 M2, M1, M0	R RSVD
⊠ RDWR_B	H HSWAP_EN	▨ VCCO
◓ BUSY/DOUT	K TCK	◪ VCCAUX
◐ INIT_B	I TDI	▪ VCCINT
● GCLKx (P)	O TDO	▩ GND
◑ GCLKx (S)	M TMS	n NO CONNECT
⊖ VRP	W PWRDWN_B	
⊕ VRN		
⊗ VREF		
Triple-Purpose Pins:		
⊙ D2, D4/ALT_VRP		
⊕ D3, D5/ALT_VRN		

Corresponding Pinouts

FF896	FF1152
A2	C4
.	.
.	.
.	.
.	.
.	.
AK29	AM31

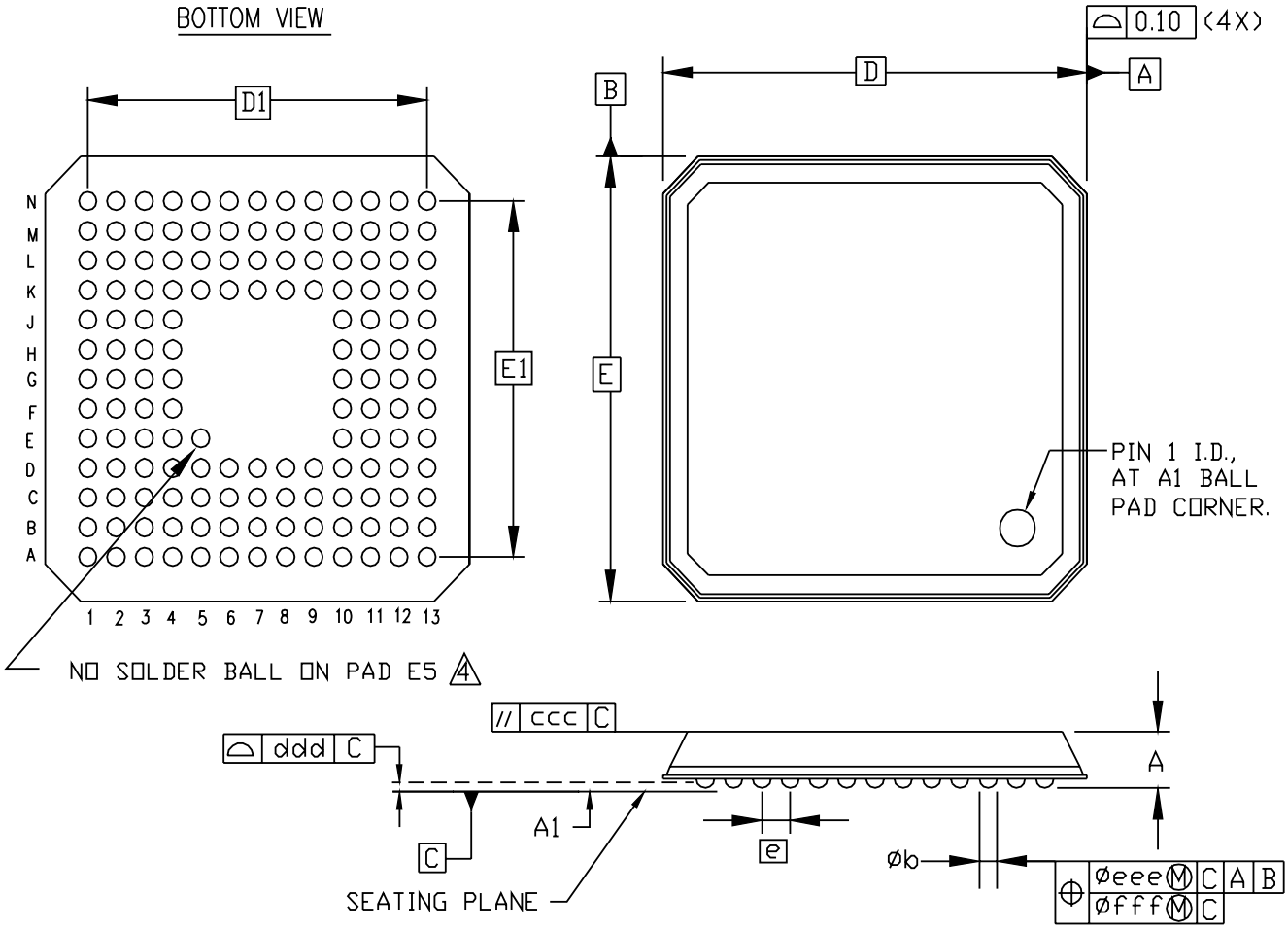
ug002_c4_55_032901

Figure 4-30: **FF896 - FF1152 Pinout Compatibility Diagram**

Package Specifications

This section contains specifications for the following Virtex-II packages:

CS144 Chip-Scale BGA Package (0.80 mm Pitch)



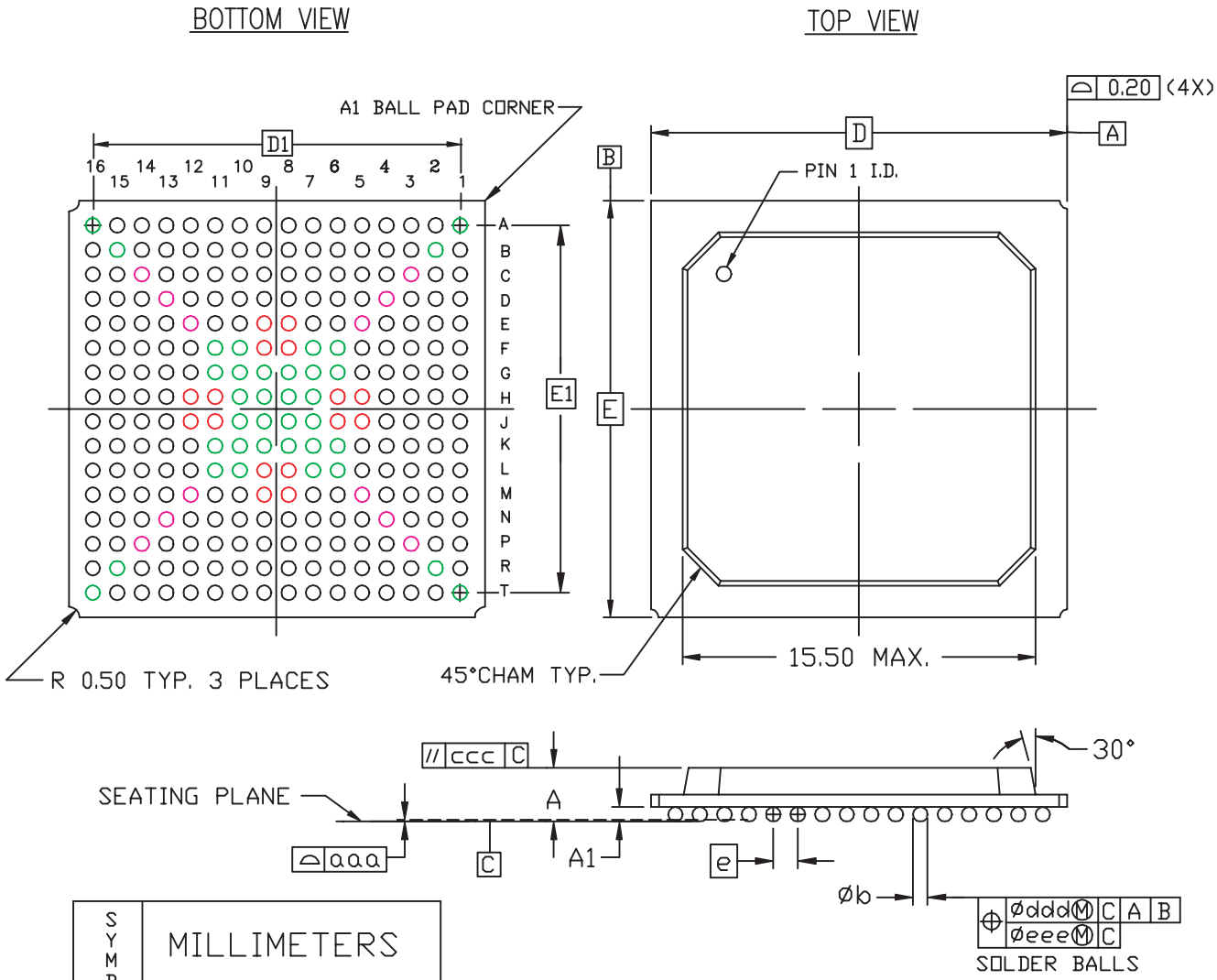
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.20
A_1	0.35	0.40	0.45
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.45	0.50	0.55
ccc			0.10
ddd			0.12
eee			0.15
fff			0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–205–BE (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

Figure 4-31: **CS144 Chip-Scale BGA Package**

FG256 Fine-Pitch BGA Package (1.00 mm Pitch)



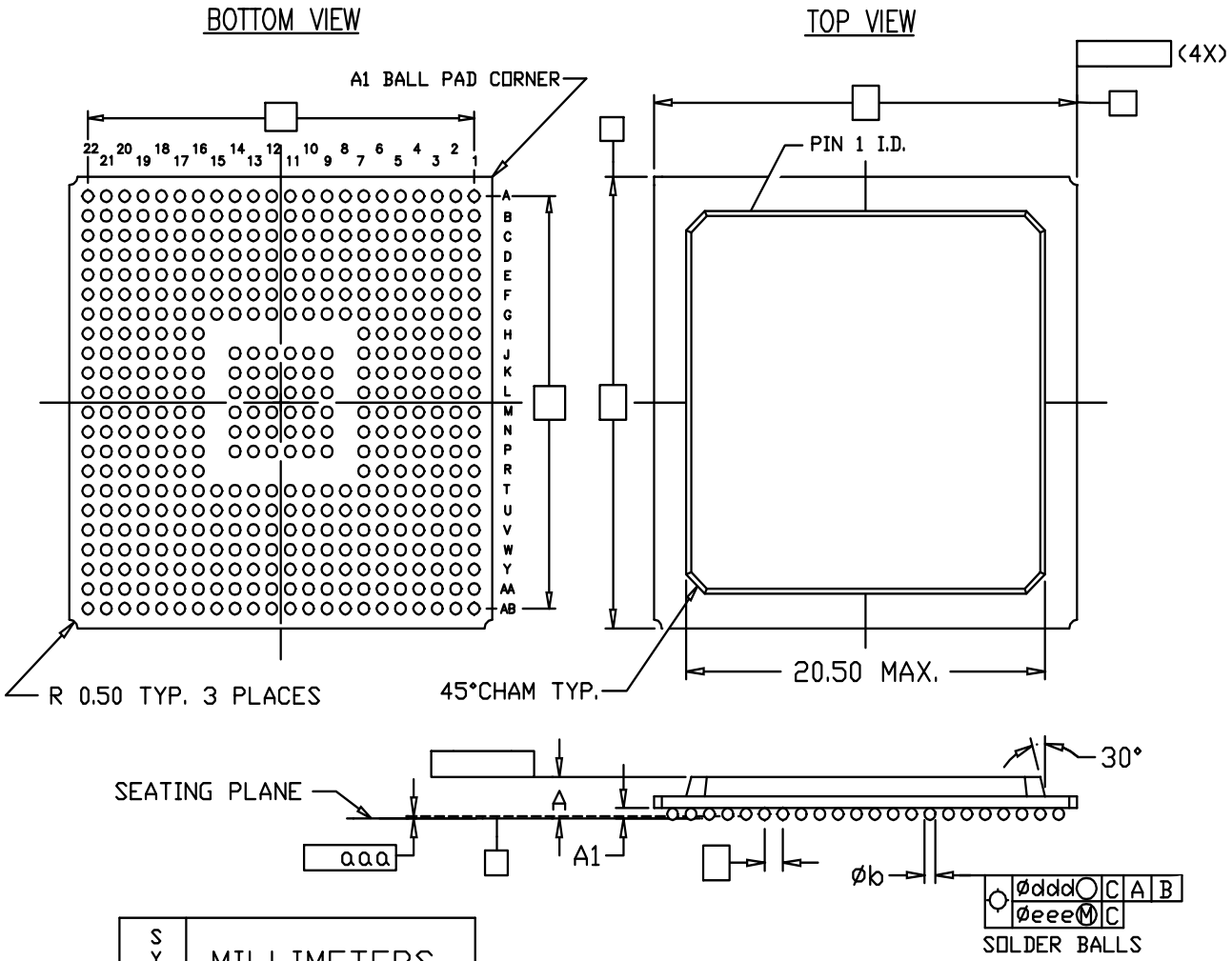
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.73	2.00
A_1	0.40	0.50	0.60
D/E	17.00 BSC		
D_1/E_1	15.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	16		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO–151 AAF–1.

Figure 4-32: **FG256 Fine-Pitch BGA Package**

FG456 Fine-Pitch BGA Package (1.00 mm Pitch)



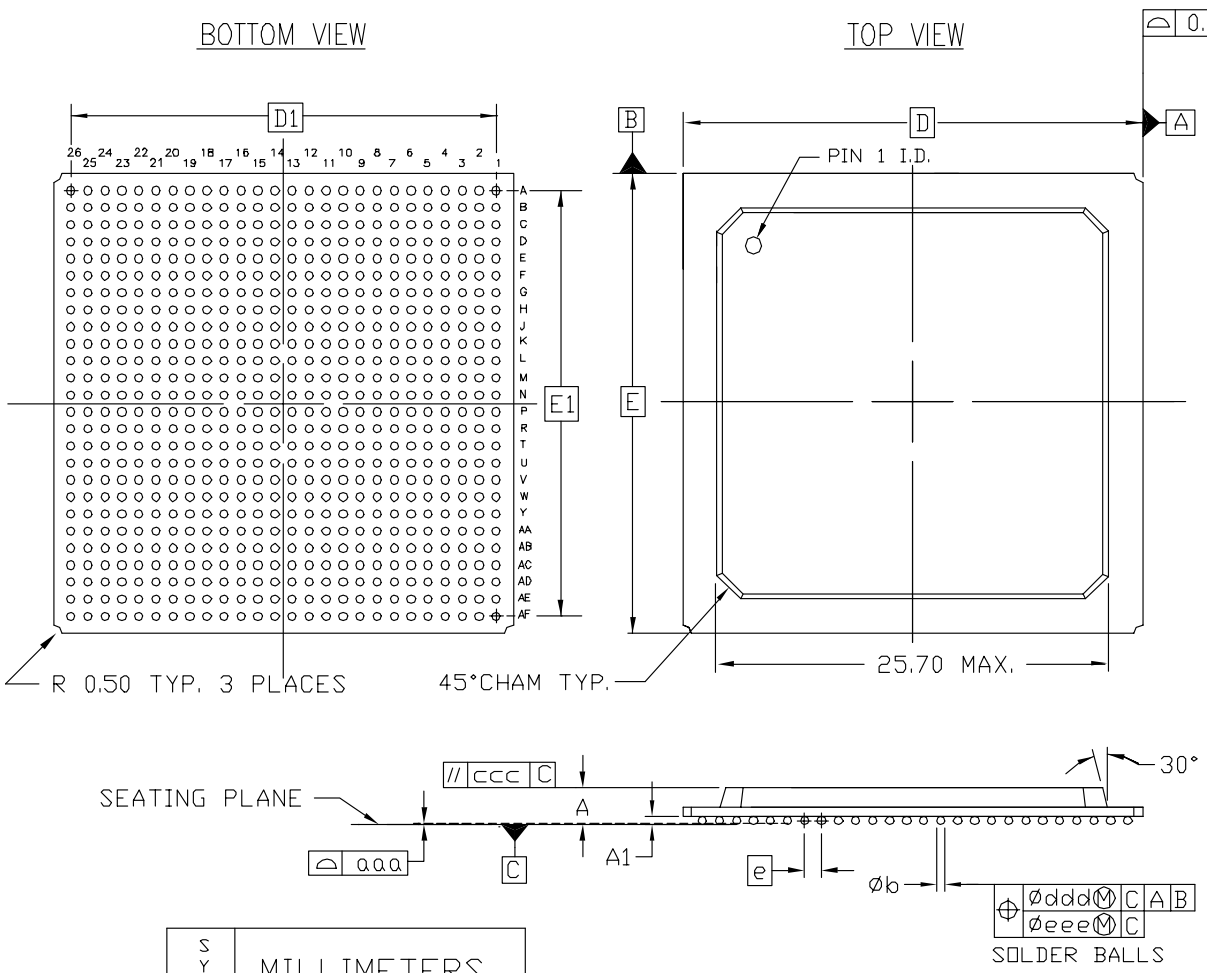
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.20	2.60
A_1	0.40	0.50	0.60
D/E	23.00 BSC		
D_1/E_1	21.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	22		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1 (DEPOPULATED)

Figure 4-33: **FG456 Fine-Pitch BGA Package**

FG676 Fine-Pitch BGA Package (1.00 mm Pitch)



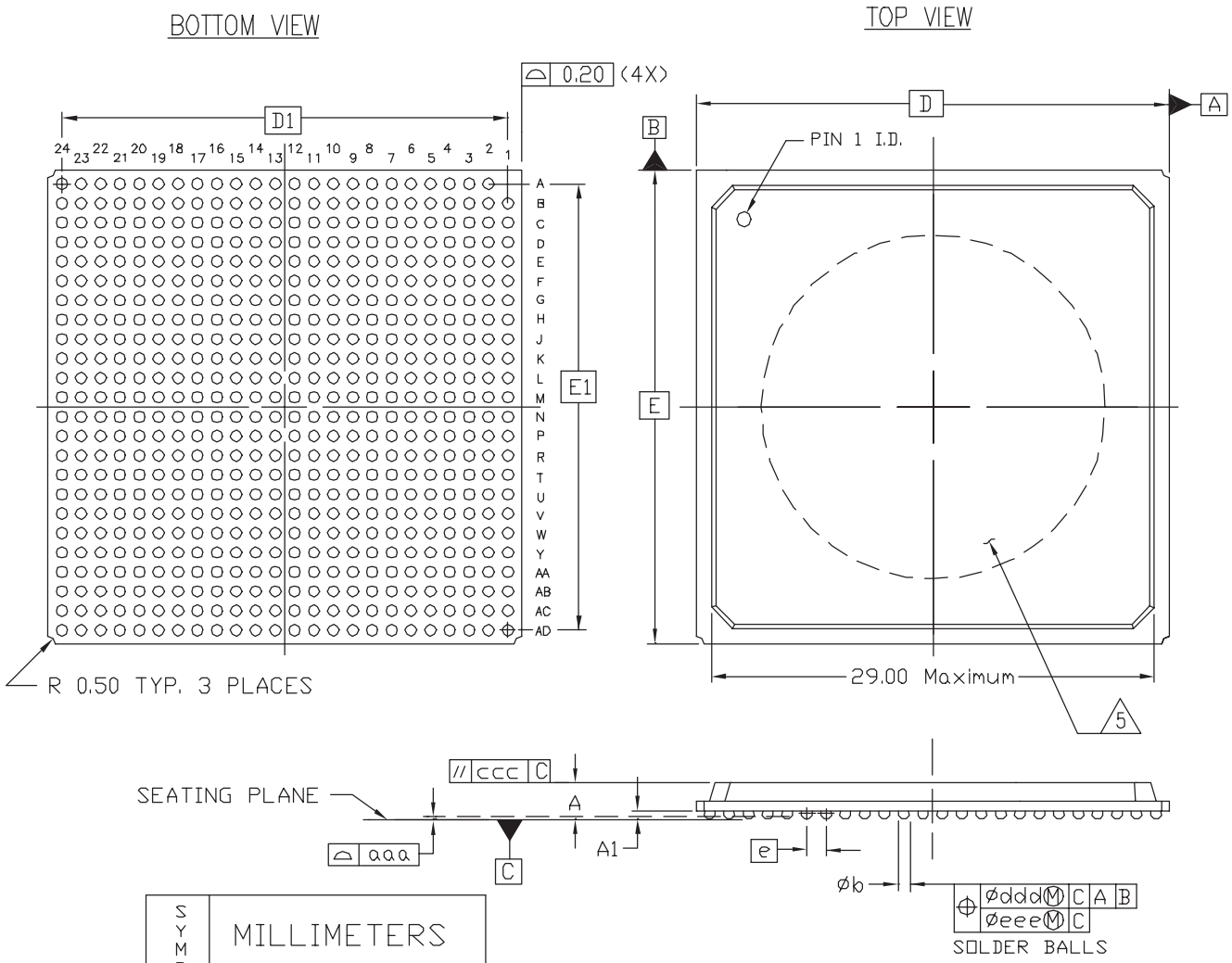
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

Figure 4-34: **FG676 Fine-Pitch BGA Package**

BG575 Standard BGA Package (1.27 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.15
M	24		

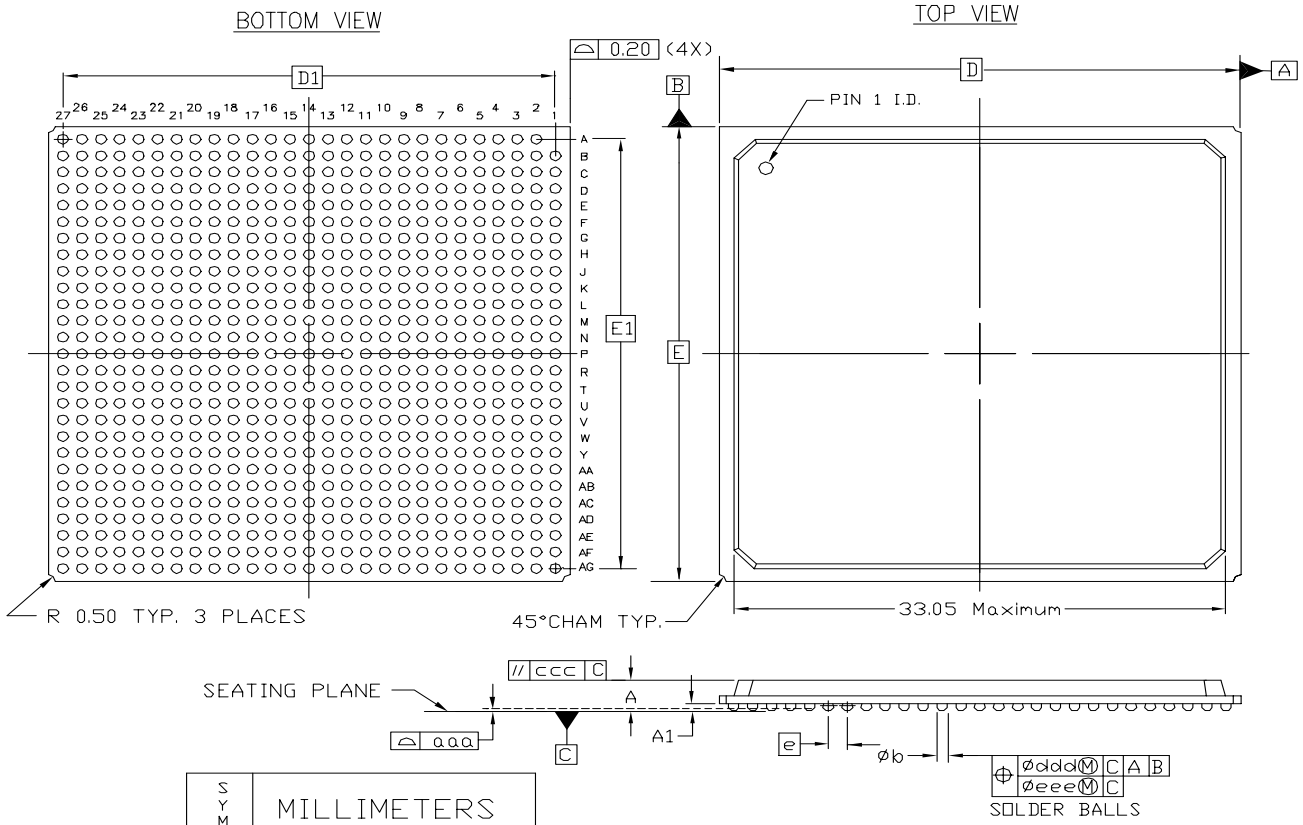
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 BAN–1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

Figure 4-35: **BG575 Standard BGA Package**

BG728 Standard BGA Package (1.27 mm Pitch)



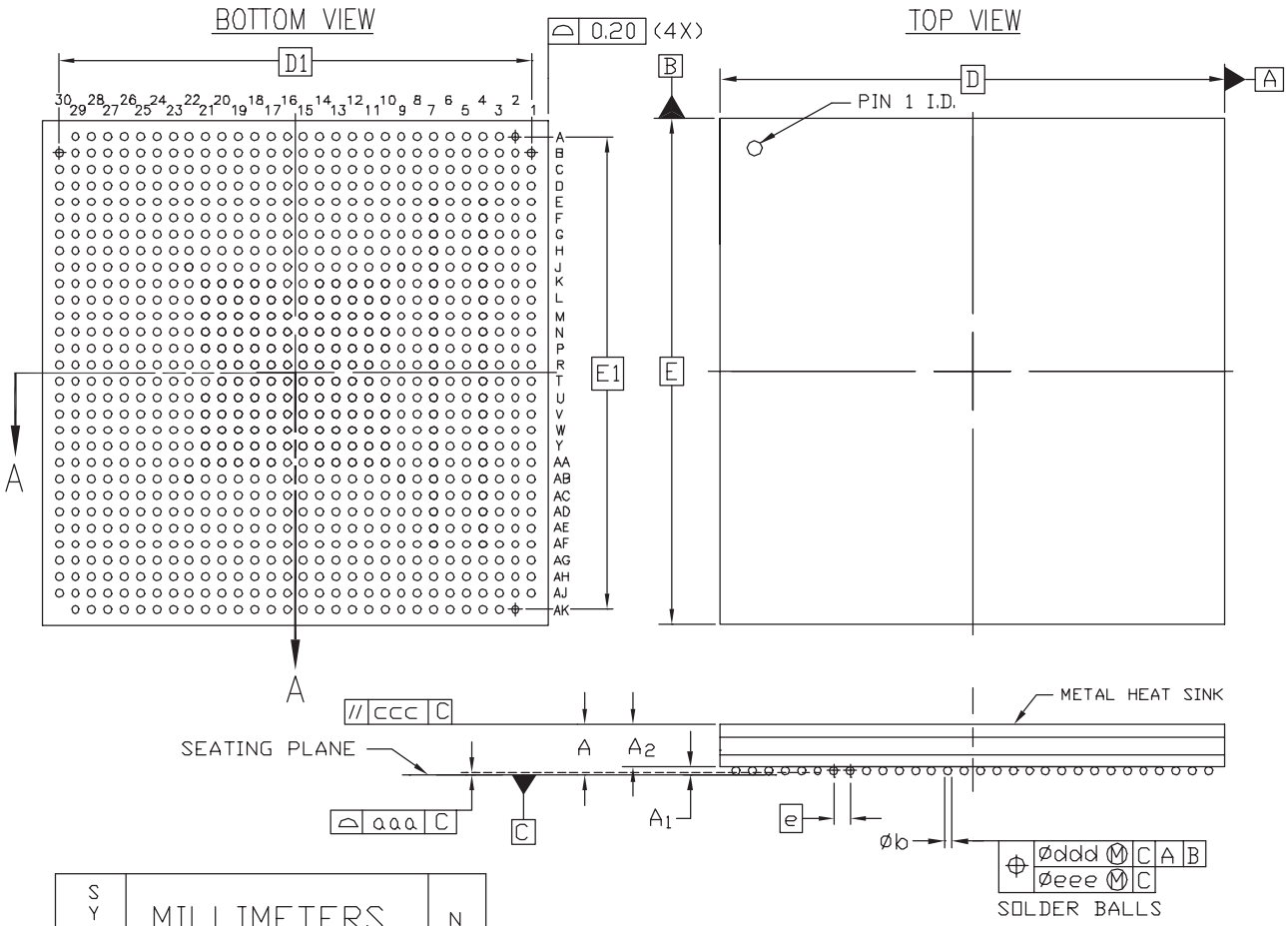
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa	---	---	0.20
ccc	---	---	0.35
ddd	---	---	0.30
eee	---	---	0.15
M	27		

NOTES:

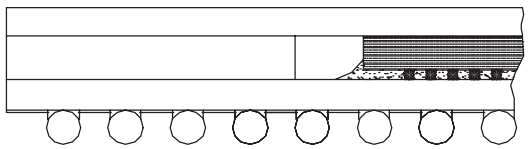
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAR–1
4. NO SOLDER BALL AND LAND ON A1.

Figure 4-36: **BG728 Standard BGA Package**

FF896 Flip-Chip Fine-Pitch BGA Package (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	30			2



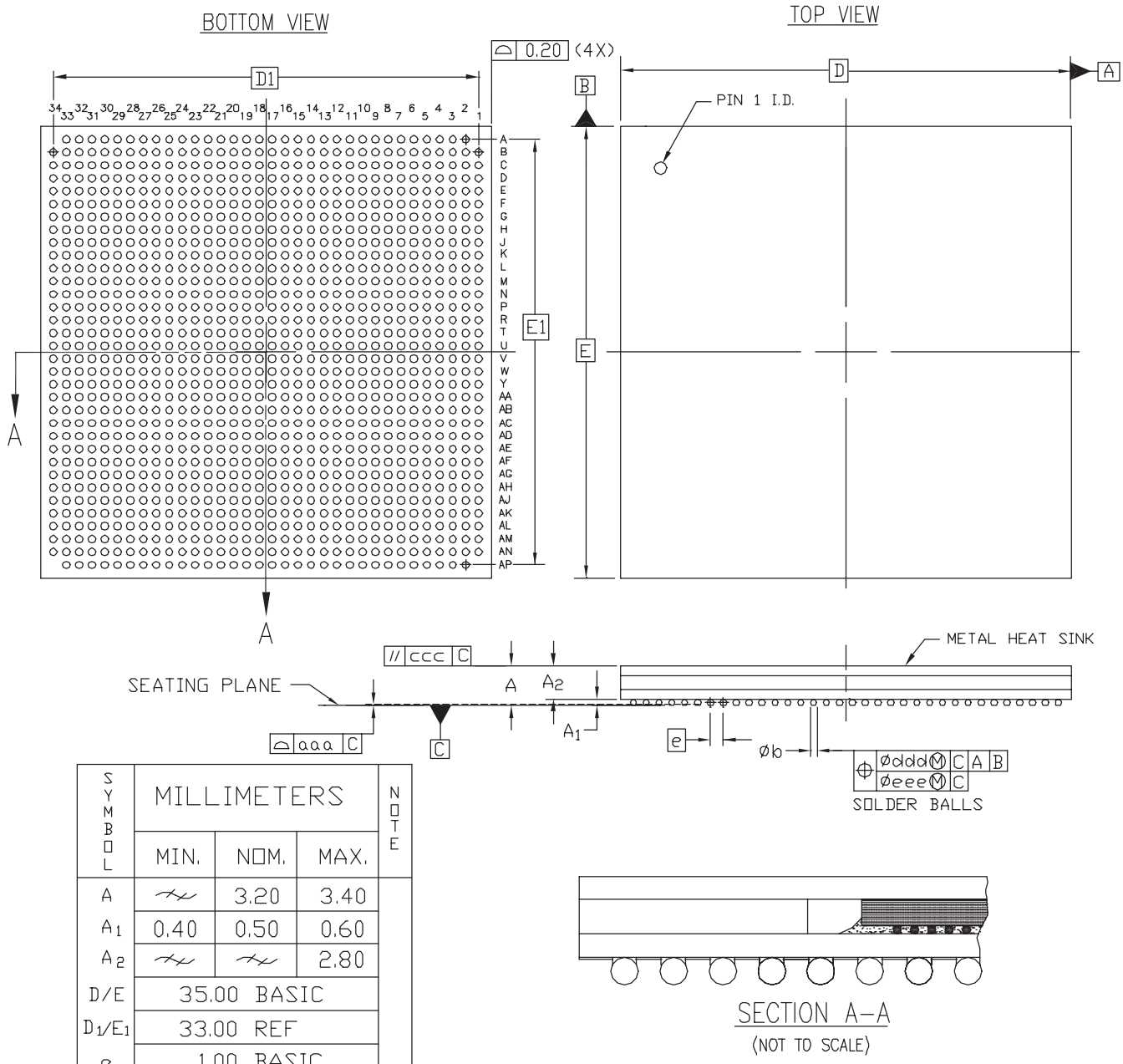
SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAN–1 (DEPOPULATED)

Figure 4-37: **FF896 Flip-Chip Fine-Pitch BGA Package**

FF1152 Flip-Chip Fine-Pitch BGA Package (1.00 mm Pitch)



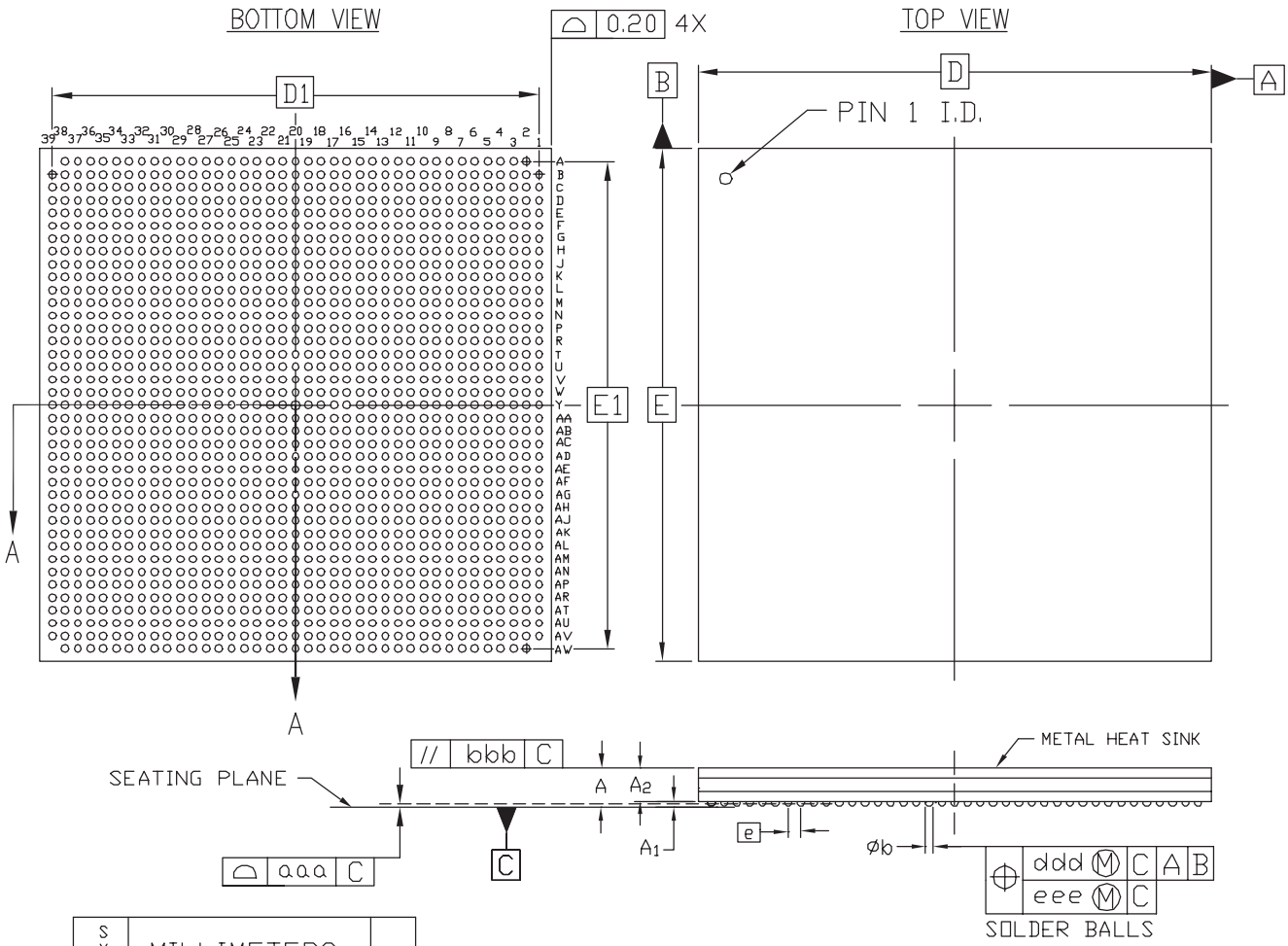
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

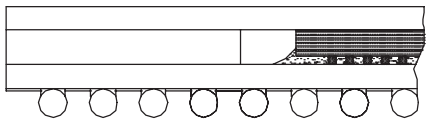
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 4-38: **FF1152 Flip-Chip Fine-Pitch BGA Package**

FF1517 Flip-Chip Fine-Pitch BGA Package (1.00 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		39		2



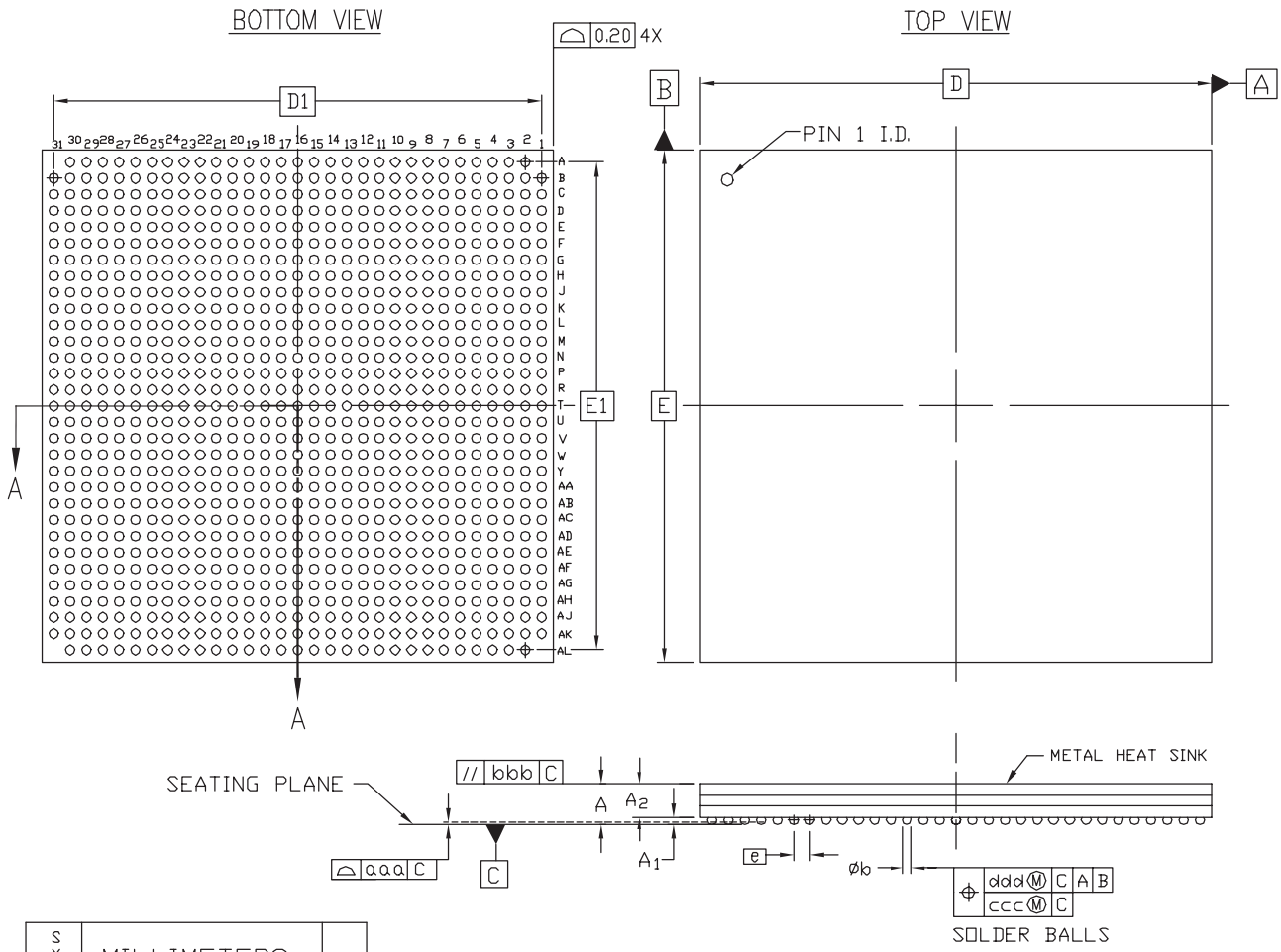
SECTION A–A
(NOT TO SCALE)

NOTES:

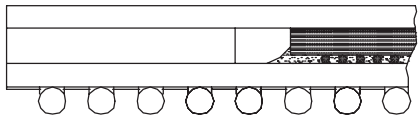
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 4-39: **FF1517 Flip-Chip Fine-Pitch BGA Package**

BF957 Flip-Chip BGA Package (1.27 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.25	3.50	
A_1	0.50	0.60	0.70	
A_2			2.80	
A_3	0.20			
D/E	40.00 BSC			
D_1/E_1	38.10 REF.			
e	1.27 BSC			
øb	0.60	0.75	0.90	
aaa			0.20	
bbb			0.25	
ccc			0.15	
ddd			0.30	
M	31			



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAU–1 (DEPOPULATED)

Figure 4-40: **BF957 Flip-Chip BGA Package**

Flip-Chip Packages

As silicon devices become more integrated with smaller feature sizes as well as increased functionality and performance, packaging technology is also evolving to take advantage of these silicon advancements. Flip-chip packaging is the latest packaging option introduced by Xilinx to meet the demand for high I/O count and high performance required by today's advanced applications.

Flip-chip packaging interconnect technology replaces peripheral bond pads of traditional wire-bond interconnect technology with area array interconnect at the die/substrate interface.

The area array pads contain wettable metallization for solders (either eutectic or high-lead), where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to yield bumped dies with relatively uniform solder bumps spread over the surface of the device. Unlike traditional packaging in which the die is attached to the substrate face up and the connection is made by using wire, the bumped die in a flip-chip package is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chip is placed offset on the substrate.

Flip-chip packages are assembled on high-density, multi-layer ceramic or organic laminate substrates. Since flip-chip bump pads are in area array configuration, very fine lines and geometry on the substrates are required to be able to successfully route the signals from the die to the periphery of the substrates. Multi-layer build-up structures offer this layout flexibility on flip-chip packages, and they provide improvements in power distribution and signal transmission characteristics.

Advantages of Flip-Chip Technology

Flip-chip interconnections in combination with the advanced multi-layer laminated substrates provide superior performance over traditional wire-bond packaging. Benefits include:

- Easy access to core power/ground and shorter interconnects, resulting in better electrical performance
- Better noise control since the inductance of flip-chip interconnect is lower
- Excellent thermal performance due to direct heatsinking to backside of the die
- Higher I/O density since bond pads are in area array format
- Smaller size

Thermal Data

Thermal Considerations

Due to the variety of applications in which Virtex-II FPGA devices are likely to be used, it is traditionally a challenge to predict the power requirements, and thus the thermal management needs, of a particular application. Virtex-II devices in general are characterized by high I/O counts and very high user gate counts. The attributes that make the devices popular with users also give the devices the potential of being clocked fast, which results in high power consumption. Because of this high heat-generating potential, the Virtex-II package offering (see Table 4-3) includes medium and high power capable packaging options.

Table 4-3 shows thermal resistance parameters for Virtex-II packages. These include: Junction-to-ambient, Junction-to-case and Junction-to-board. Estimated power consumption capability is given, as well. These values were derived with some typical thermal management assumptions, stated in the table.

Table 4-3: **Thermal Data for Virtex-II Packages**

Package	Lead Pitch (mm)	Junction to Ambient Theta-J_A Range °C/Watt in Air	Junction to Case Theta-J_C Typical °C/Watt	Junction to Board Psi-J_B ("Theta-J_B") Typical °C/Watt	Max Power Bare Pkg (Watts) T_A = 50 °C T_{JMAX} = 100 °C	Power With Heatsink (Watts) Theta-SA = 1.5 °C/Watt Theta-cs = 0.1 °C/Watt T_A = 50° C T_J = 100° C
CS144 Flex Based 12x12	0.8	32 - 36	1	20	1.5	
FG256 2- 4L PCB 17x17	1.0	30 -35	3.5	19	1.5	
FG456 4L PCB 23x23	1.0	15 - 28	2.0	11	2.4	
FG676 4L PCB 27x27	1.0	14 -22	1.8	9	2.8	15
BG575 4L PCB 31x31	1.27	13 - 20	1.6	7	3.1	16
BG728 4L PCB 35x35	1.27	12 -20	1.5	6	3.3	16
BF957 40x40 Flip-Chip	1.27	8 - 13	0.7	3	5.0	22
FF896 31x31 Flip-Chip	1.0	9 - 14	0.8	4	4.5	21
FF1152 35x35 Flip-Chip	1.0	8 - 13	0.8	4	4.5	21
FF1517 40x40 Flip-Chip	1.0	8 - 12	0.7	3	5.0	22

Virtex-II packages can be grouped into three broad performance categories: low, medium, and high, based on their power handling capabilities. All of the packages can use external thermal enhancements, which can range from simple airflow to schemes that can include passive as well as active heatsinks. This is particularly true for high-performance flip-chip packages where system designers have the option to further enhance the packages to handle in excess of 25 watts, with arrangements that take system physical constraints into consideration. Table 4-4 shows simple but incremental power management schemes that can be brought to bear on flip-chip packages.

Table 4-4: **Virtex-II Flip-Chip Thermal Management**

Power	Technique	Description
Low End (1 - 6 watts)	Bare package with moderate air 8 - 12 °C/Watt	Bare package. Package can be used with moderate airflow within a system.
Mid Range (4 - 10 watts)	Passive heatsink with air 5 - 10 °C/Watt	Package is used with various forms of passive heatsinks and heat spreader techniques.
High End (8 - 25 watts)	Active heatsink 2 - 3 °C/Watt or better	Package is used with active heatsinks, TEC, and board-level heat spreader techniques

Thermal Management Options

The following are thermal management options to consider:

- For moderate power dissipation (2 to 6 watts), the use of passive heatsinks and heatspreaders attached with thermally conductive double-sided tapes or retainers can offer quick thermal solutions.
- The use of lightweight finned external passive heatsinks can be effective for dissipating up to 10 watts. If implemented with forced air as well, the benefit can be a 40% to 50% increase in heat handling efficiency over bare packages. The more efficient external heatsinks tend to be tall and heavy. To help protect component joints from bulky heatsink induced stresses, the use of spring loaded pins or clips that transfer the mounting stress to a circuit board is advisable. The diagonals of some of these heatsinks can be designed with extensions to allow direct connections to the board.
- Flip-chip packages: All flip-chip packages are thermally enhanced BGAs with die facing down. They are offered with exposed metal heatsink at the top. These high-end thermal packages lend themselves to the application of external heatsinks (passive or active) for further heat removal efficiency. Again, precaution should be taken to prevent component damage when a bulky heatsink is attached.
- Active heatsinks can include a simple heatsink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TECs) with a fan to blow away any heat generated. Any considerations to apply TEC in heat management should require consultation with experts in using the device, since these devices can be reversed and cause damage to the components. Also, condensation can be an issue.
- Molded packages (FG456, FG676, BG575, BG728, and so forth) with or without exposed metal at the top can also use heatsinks at the top for further heat removal. These BGA packages are similar in construction to those used in Graphics cards in PC applications, and heatsinks used for those applications can easily be used for these packages, as well. In this case, the Junction-to-Case resistance is the limiting consideration.
- Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. Board designs can be implemented to take advantage of a board's ability to spread heat. The effect of the board is dependent on its size and how it conducts heat. Board size, the level of copper traces on it, and the number of buried copper planes all lower the junction-to-ambient thermal resistance for packages mounted on the board.

  The junction-to-board thermal resistance for Virtex-II packages are given in Table 4-3. A standard JEDEC type board was used for obtaining the data. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources - particularly if the board is not cooled effectively. An otherwise cooler component might be heated by other heat contributing components on the board.

Printed Circuit Board Considerations

Layout Considerations

The PC board is no longer just a means to hold ICs in place. At today's high clock rates and fast signal transitions, the PC board performs a vital function in feeding stable supply voltages to the IC and in maintaining signal integrity between devices.

VCC and Ground Planes

Since CMOS power consumption is dynamic, it is a non-trivial task to assure stable supply voltages at the device pins and to minimize ground differentials. A multi-layer PC board is a must, with four layers for the simplest circuits, 6 to 12 layers for typical boards. Ground and V_{CC} must each be distributed in complete layers with few holes. Slots in these layers would cause an unacceptable inductive voltage drop, when the supply current changes at a rate of 1 A/ns, or even faster. Besides an uninterrupted ground plane, Virtex-II devices require one plane for V_{CCINT} (1.5 V) plus one plane for V_{CCAUX} (3.3 V). V_{CCO} can be distributed on wide signal traces with sufficient bypass capacitors.

Beyond low resistance and inductance, ground and V_{CC} planes combined can also provide a small degree of V_{CC} decoupling. The capacitance between two planes is ~100 pF/inch^2 or ~15 pF/cm^2, assuming 10 mil (0.25 mm) spacing with FR4 epoxy.

V_{CC} Decoupling

Fast changing Icc transitions must be supplied by local decoupling capacitors, placed very closely to the V_{CC} device pins or balls. These capacitors must have sufficient capacitance to supply Icc for a few ns and must have low intrinsic resistance and inductance. X7R or NPO ceramic surface-mounted capacitors of 0.01 to 0.1 µF, one per V_{CC} device pin, are appropriate. 0.1 µF can supply 1A for 2ns with a 20 mV voltage droop.

1A • 2ns = 2 nanocoulomb = 100 nF • 0.02 V

Low impedance at >100 MHz is important, but capacitance variation with temperature is acceptable. These small capacitors are the first-line source for Icc, and they must be placed very close to the V_{CC} pins. A half-inch or 10 mm trace represents an inductance of several nanohenries, defeating the purpose of the decoupling capacitor. Backing up this local decoupling is one tantalum capacitor of 10 to 100 µF, able to supply multiple amperes for about 100 ns.

Finally, each board needs a power-supply decoupling electrolytic capacitor of 1000 to 10,000 µF able to supply even more current for a portion of the supply switching period. As described below, larger capacitors inevitably have higher series resistance and inductance, which is the reason for the above-mentioned hierarchy of supply decoupling. As a general rule, multiple capacitors in parallel always offer lower resistance and inductance than any single capacitor.

Decoupling Capacitors

The ideal decoupling capacitor would present a short circuit to ground for all ac signals. A real capacitor combines a given amount of capacitance with unavoidable parasitics, a small series resistance and inductance. At low frequencies, the composite impedance is capacitive, i.e., it decreases with increasing frequency. At high frequencies, it is inductive and increases with frequency, making the decoupling ineffective. In-between, there is the LC resonant frequency, where the capacitor looks like a small resistor.

Different technologies provide different trade-offs between desirable features like small size and high capacitance, and undesirable features like series resistance and inductance. Electrolytic and tantalum capacitors offer the largest capacitance in a given physical size, but also have the highest inductance. This makes them useful for decoupling low frequencies and storing large amounts of charge, but useless for high frequency decoupling. Surface-mount ceramic capacitors, on the other hand, offer the lowest

inductance and the best high-frequency performance, but offer only a small amount of capacitance, less than a microfarad.

Figure 4-41 shows the frequency-dependent impedance and resistance of a typical electrolytic capacitor of 1500 µF, while Figure 4-42 and Figure 4-43 show the equivalent data for ceramic bypass capacitors of 33,000 and 3,300 pF, respectively. Note that the resonant frequency for the small ceramic bypass capacitor at 100 MHz is 10,000 times higher than the resonance frequency of the large electrolytic capacitor at 10 KHz. For more technical information on decoupling capacitors, see the manufacturers' websites.

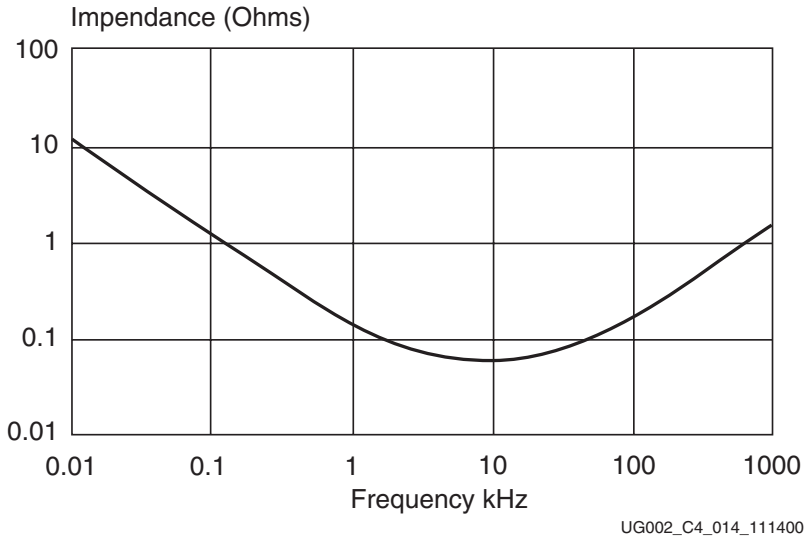


Figure 4-41: **1500 µF Electrolytic Capacitor Frequency Response Curve**

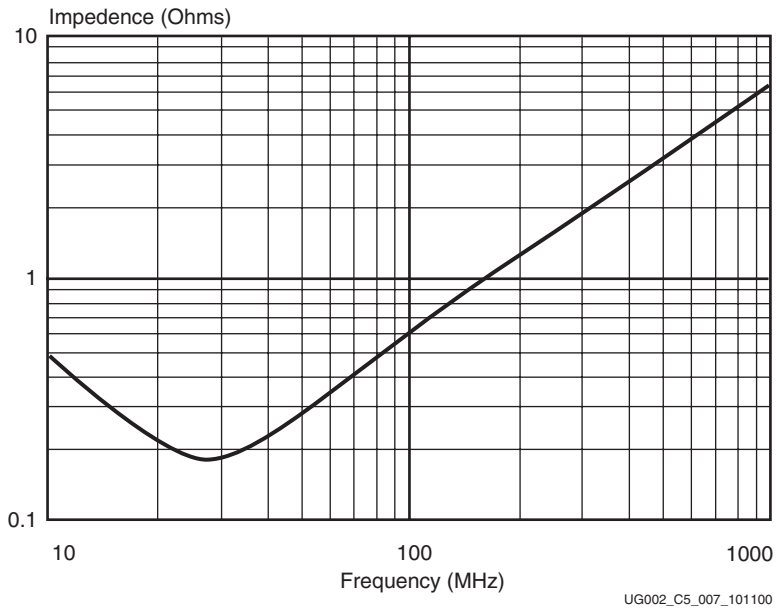


Figure 4-42: **33000 pF X7R Component Frequency Response Curve**

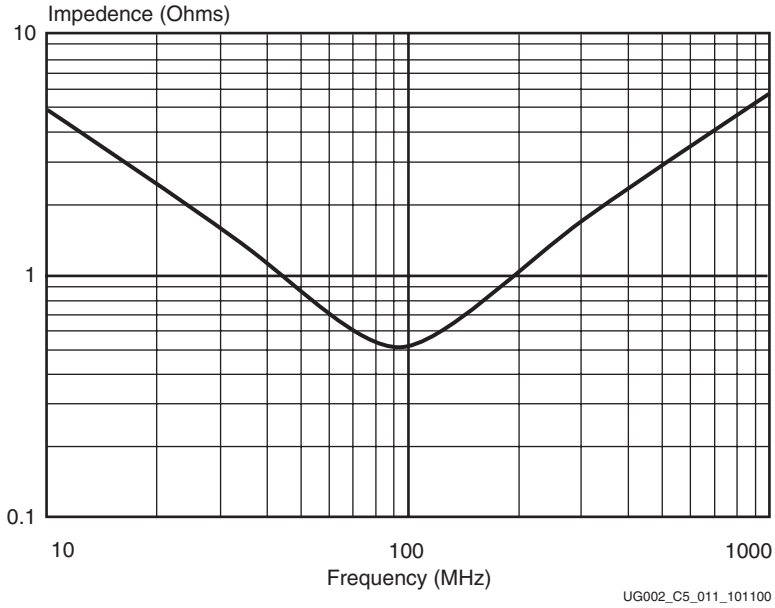


Figure 4-43: **3300 pF X7R Component Frequency Response Curve**

Transmission Line Reflections and Terminations

A PC board trace must be analyzed as a transmission line. Its series resistance and parallel conductance can generally be ignored, but series inductance and parallel capacitance per unit length are important parameters. Any signal transition (rising or falling edge) travels along the trace at a speed determined by the incremental inductance and capacitance.

For an outer-layer trace (air on one side) the propagation delay is 140 ps/inch, or 55 ps/cm. For an inner-layer trace (FR4 with ε=4.5 on both sides), the propagation delay is 180 ps/inch, or 70 ps/cm.

The voltage-to-current ratio at any point along the transmission line is called the characteristic impedance Z_0. It is determined by w/d, the ratio of trace width w to the distance d above the ground or V_{CC} plane.

For an outer layer trace (microstrip),

Z_0=50 Ω when w = 2d (e.g., w = 12 mil, d = 6 mil),

Z_0=75 Ω when w = d (e.g., both 6 mil = 0.15 mm).

For an inner layer trace between two ground or V_{CC} planes (stripline),

Z_0=50 Ω when w = 0.6•d (e.g., w = 5 mil, d = 8 mil),

Z_0=75 Ω when w = 0.25•d (impractical).

Most signal traces fall into the range of 40 to 80 Ω.

A slow transition treats a short narrow trace as a lumped capacitance of about 2 pF per inch (0.8 pF per cm). However, if the trace is so long, or the signal transition is so fast that the potential echo from the far end arrives after the end of the transition, then the trace must be analyzed as a transmission line.

In this case, the driver sees the trace not as a lumped capacitance, but rather as a pure resistance of Z_0. The signal transition then travels along the trace at the speed mentioned above. At any trace-impedance discontinuity all or part of the signal is reflected back to the origin. If the far end is resistively terminated with R=Z_0, then there is no reflection. If, however, the end is open, or loaded with only a CMOS input, then the transition doubles in amplitude, and this new wave travels back to the driver, where it may be reflected again, resulting in the familiar ringing. Such ringing has a serious impact on signal integrity, reduces noise margins, and can lead to malfunction, especially if an asynchronous signal or

a clock signal crosses the input threshold voltage unpredictably. Two alternate ways to avoid reflections and ensure signal integrity are parallel termination and series termination.

Parallel Termination

Reflections from the far end of the transmission line are avoided if the far end is loaded with a resistor equal to Z_0. A popular variation uses two resistors, one to V_{CC}, one to ground, as the Thevenin equivalent of Z_0. This reduces the load current for one signal level, while increasing it for the other. Parallel termination causes dc power consumption which can be eliminated by inserting a capacitor between the terminating resistor and ground. The value of this capacitor is determined as follows:

Signal transition time << RC << signal level duration

For example, 50 Ω • 120 pF for a 2 ns transition every 20 ns. See Figure 4-44.

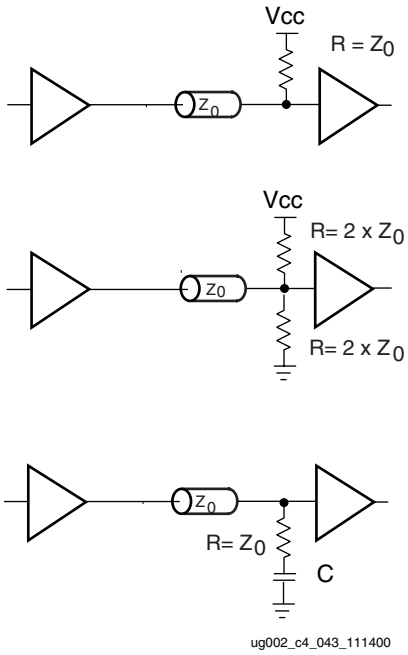


Figure 4-44: **Parallel Termination**

Series Termination

While parallel termination eliminates reflections, series termination relies on the reflection from the far end to achieve a full-amplitude signal. For series termination, the driver impedance is adjusted to equal Z_0, thus driving a half-amplitude signal onto the transmission line. At the unterminated far end, the reflection creates a full-amplitude signal, which then travels back to the driver where it gets absorbed, since the output impedance equals Z_0. See Figure 4-45.

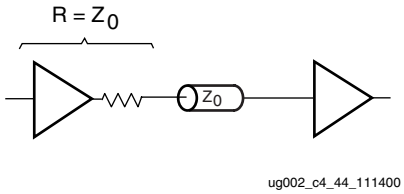


Figure 4-45: **Series Termination**

Series termination dissipates no dc power, but the half-amplitude round-trip delay signal means that there must be no additional loads along the line. Series termination is ideal (and only meaningful) for single-source-single-destination interconnects.

Virtex-II devices offer digitally controlled output impedance drivers and digitally-controlled input termination, thus eliminating the need for any external termination resistors. This feature is extremely valuable with high pin-count, high density packages.

These PC board considerations apply to all modern systems with fast current and voltage transitions, irrespective of the actual clock frequency. The designer of relatively slow systems is more likely caught off-guard by the inherent speed of modern CMOS ICs, where di/dt is measured in A/ns, dV/dt is measured in V/ns, and input flip-flops can react to 1 ns pulses, that are invisible on mid-range oscilloscopes. Powerful tools like HyperLynx can analyze signal integrity on the PC board and can often be amortized by one eliminated board-respin.

JTAG Configuration and Test Signals

Poor signal integrity and limitations of devices in a JTAG scan chain can reduce the maximum JTAG test clock (TCK) rate and reliability of JTAG-based configuration and test procedures. The JTAG TCK and test mode (TMS) signals must be buffered, distributed, and routed with the same care as any clock signal especially for long JTAG scan chains. The devices in a JTAG scan chain should be ordered such that the connections from the TDO of one device to the TDI of the next device are minimized. When high-speed JTAG-based configuration for the Virtex-II devices is required, devices with lower-specified maximum TCK rates can be placed in a separate JTAG scan chain.

Crosstalk

Crosstalk can happen when two signals are routed closely together. Current through one of the traces creates a magnetic field that induces current on the neighboring trace, or the voltage on the trace couples capacitively to its neighbor. Crosstalk can be accurately modeled with signal integrity software, but two easy to remember rules of thumb are:

- Crosstalk falls off with the square of increasing distance between the traces.
- Crosstalk also falls off with the square of decreasing distance to a ground plane.

$$\text{Peak Crosstalk Voltage} = \frac{DV}{1 + (D/H)^2}$$

where

DV is the voltage swing

D is the distance between traces (center to center)

H is the spacing above the ground plane

Example:

3.3V swing, and two stripline traces 50 mils apart and 50 mils above the ground plane.

Peak Crosstalk Voltage = $(3.3\ V)/(1 + (0.05/0.05)^2) = 1.65\ V$

This can cause a false transition on the neighboring trace. Separating the trace by an additional 50 mils is significantly better:

Peak Crosstalk Voltage = $(3.3\ V)/(1 + (0.1/0.05)^2) = 0.66\ V$

Signal Routing to and from Package Pins

Signal escaping (traces leaving the pin/ball area) can be quite difficult for the large FG and flip-chip packages. The number of signal layers required to escape all the pins depends on the PCB design rules. The thinner the traces, the more signals per layer can be routed, and the fewer layers are needed. The thinner traces have higher characteristic impedance, so choose an impedance plan that makes sense, and then be consistent. Traces from 40 to 80 ohms are common.

If only one signal can be escaped between two pads, only two rows of pins can be escaped per layer. For FG packages (1.0mm pitch) one signal of width 5 mils (0.13mm) can be

escaped between two pads, assuming a space constraint equal to the trace width. For a discussion of signal routing specific to Virtex-II devices, see www.xilinx.com for currently available application notes.

As packages are able to handle more I/Os with a minimum increase in size, the signal integrity of those signals must be considered, regardless of clock frequency. Especially with the largest packages, precise PCB layer stackup is required. Parameters such as board material, trace width, pad type, and stackup must be defined based on simulation, and the fabrication drawings must be marked with "precise layer stackup" and the stackup specified. A number of board-level signal integrity simulators exist, and careful attention to PCB design rules creates a robust design with low EMI and high signal reliability.

Board Routability Guidelines

Board-Level BGA Routing Challenges

Xilinx ball grid array (BGA) wire-bond and flip-chip packages contain a matrix of solder balls (see Figure 4-46). These packages are made of multilayer BT substrates. Signal balls are in a perimeter format. Power and ground pins are grouped together appropriately.

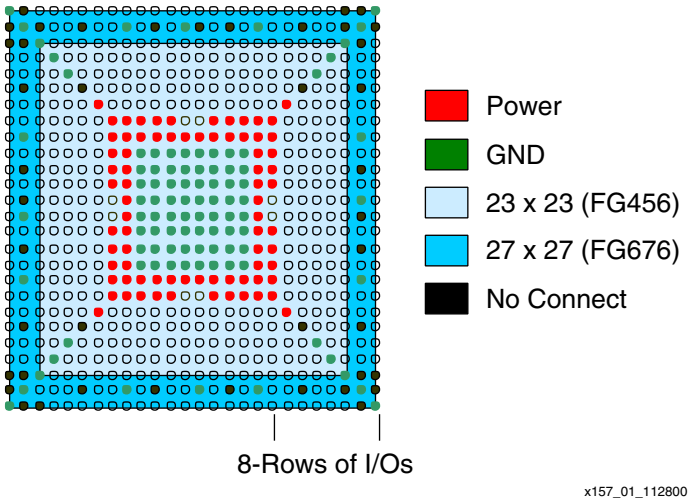


Figure 4-46: **Fine-Pitch BGA Pin Assignments**

The number of layers required for effective routing of these packages is dictated by the layout of pins in each package. If several other technologies and components are already present on the board, the system cost is factored with every added board layer. The intent of a board designer is to optimize the number of layers required to route these packages, considering both cost and performance. This section provides guidelines for minimizing required board layers for routing BGA products using standard PCB technologies (5 mils-wide lines and spaces or 6 mils-wide lines and spaces).

For high performance and other system needs, designers can use premium technologies with finer lines/spaces on the board. The pin assignment and pin grouping scheme in BGA packages enables efficient routing of the board with an optimum number of required board layers.

Board Routing Strategy

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of board layout when designing the board pads to match component-side land geometry. Typical values for these land pads are described in Figure 4-47 and summarized in Table 4-5.

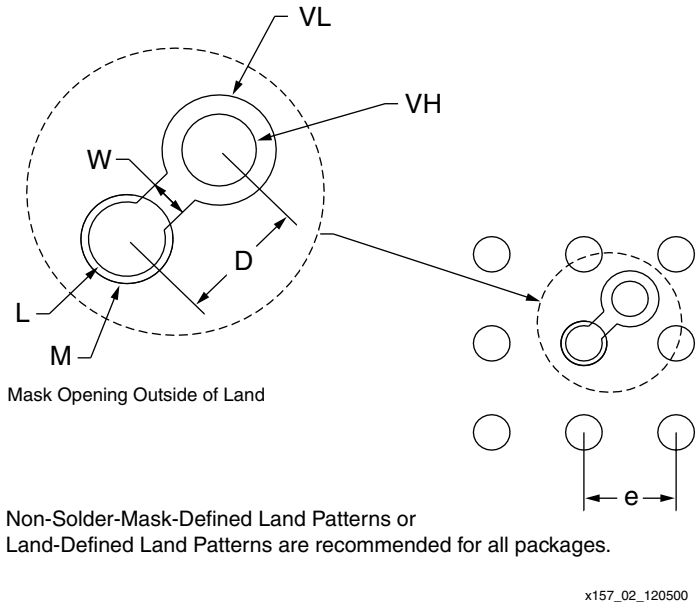


Figure 4-47: **Suggested Board Layout of Soldered Pads for BGA Packages**

Table 4-5: **Summary of Typical Land Pad Values (mm)**

Land Pad Characteristics	CS144	FG256	FG456	FG676	BG575	BG728	FF896	FF1152	FF1517	BF957
Component Land Pad Diameter (SMD)[4]	0.35	0.45	0.45	0.45	0.61	0.61	0.58	0.58	0.58	0.61
Solder Land (L) Diameter	0.33	0.40	0.40	0.40	0.56	0.56	0.50	0.50	0.50	0.56
Opening in Solder Mask (M) Diameter	0.44	0.50	0.50	0.50	0.66	0.66	0.60	0.60	0.60	0.66
Solder (Ball) Land Pitch (e)	0.80	1.00	1.00	1.00	1.27	1.27	1.00	1.00	1.00	1.27
Line Width Between Via and Land (w)	0.130	0.130	0.130	0.130	0.203	0.203	0.130	0.130	0.130	0.203
Distance Between Via and Land (D)	0.56	0.70	0.70	0.70	0.90	0.90	0.70	0.70	0.70	0.90
Via Land (VL) Diameter	0.51	0.61	0.61	0.61	0.65	0.65	0.61	0.61	0.61	0.65
Through Hole (VH), Diameter	0.250	0.300	0.300	0.300	0.356	0.356	0.300	0.300	0.300	0.356
Pad Array	-	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	13 x 13	16 x 16	22 x 22	26 x 26	24 x 24	27 x 27	30 x 30	34 x 34	39 x 39	31 x 31
Periphery Rows	4	-	7[3]	-	-	-	-	-	-	-

Notes:

1. Dimension in millimeters.
2. 3 x 3 matrix for illustration only, one land pad shown with via connection.
3. FG456 package has solder balls in the center in addition to the periphery rows of balls.
4. Component land pad diameter refers to the pad opening on the component side (solder-mask defined).

For Xilinx BGA packages, non-solder-mask defined (NSMD) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 4-47. The space between the NSMD pad and the solder mask, as well as the actual signal trace widths, depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Selection of pad types and sizes determines the available space between adjacent balls for signal escape. Based on PCB capability, the number of lines that can share the available space is described in Figure 4-48. Based on geometrical considerations, if one signal escapes between adjacent balls, then two signal rows can be routed on a single metal layer. This is illustrated in Figure 4-48 as routing with one line/channel, either at 6 mils-wide lines and spaces or 5 mils-wide lines and spaces. Using this suggested routing scheme, a minimum of eight PCB layers are required to route 10 signal rows in a package.

A slightly lower trace width can be used by the inner signal rows routed in internal layers than the width used in top and bottom external or exposed traces. Depending on the signal being handled, the practice of "necking down" a trace in the critical space between the BGA balls is allowable. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.

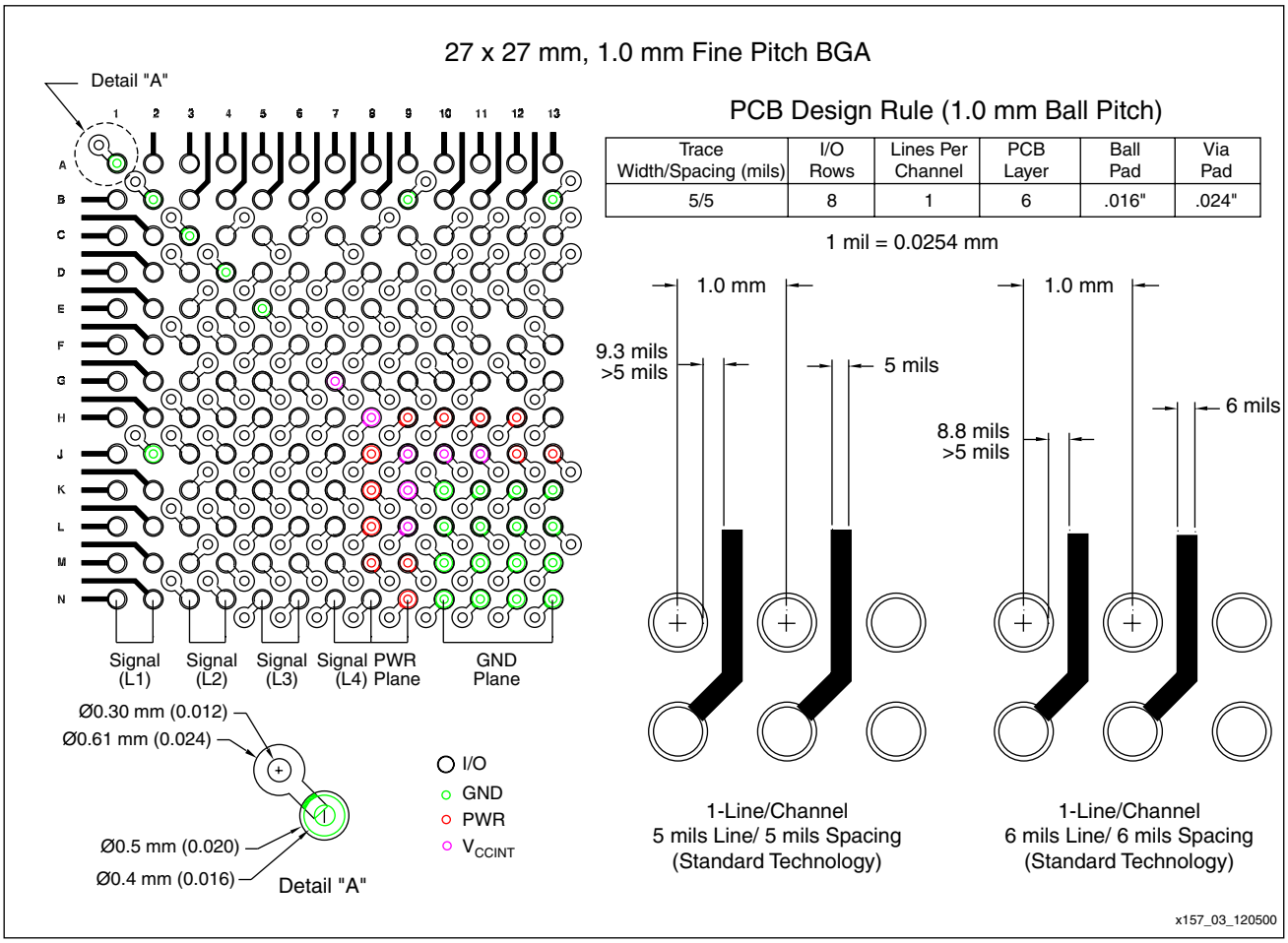


Figure 4-48: **FG676 PC Board Layout/Land Pattern**

Figure 4-48 describes a board-level layout strategy for a Xilinx 1.0 mm pitch FG676 package. Detail A in Figure 4-48 describes the opening geometry for the Land Pad and the Solder Mask. Routing with 5 mils-wide lines or spaces allows one signal per channel (between the balls). For successful routing, eight-row deep signal traces require six PCB layers. Figure 4-49 shows the suggested schematic of layers for the six-layer routing scheme.

Using premium board technology, such as Microvia Technology (allowing up to 4 mils-wide lines and spaces), efficient routing is possible with a reduced number of board layers. A grouping scheme for power, ground, control, and I/O pins, might also enable efficient routing.

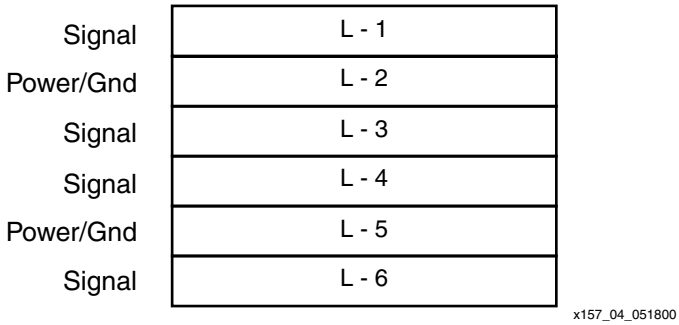


Figure 4-49: **Six-Layer Routing Scheme**

Figure 4-50 through Figure 4-67 show suggested layer-by-layer board routing for each Virtex-II package, including flip-chip packages. These drawings assume a standard PCB technology of 5 mils-wide lines and spaces. Table 4-6 lists the layer-by-layer routing examples provided. More details are contained in XAPP157, which is available on the web at **www.xilinx.com/xapp/xapp157.pdf**, as is a full-color (PDF) version of this document.

Table 4-6: **Layer-By-Layer Board Routing Examples**

Package	Standard Routing	Routing With LVDS Pairs
FG256	Top and bottom layers	Top and bottom layers
FG456	Top, 2nd, and bottom layers	Top, 2nd, and bottom layers
FG676	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
BG575	Top, 2nd, and bottom layers	Top, 2nd, and bottom layers
BG728	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
FF896	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
FF1152	Top, 2nd, 3rd, 4th, and bottom layers	Top, 2nd, 3rd, 4th, and bottom layers
FF1517	Top, 2nd, 3rd, 4th, 5th, and bottom layers	Top, 2nd, 3rd, 4th, 5th, and bottom layers
BF957	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers

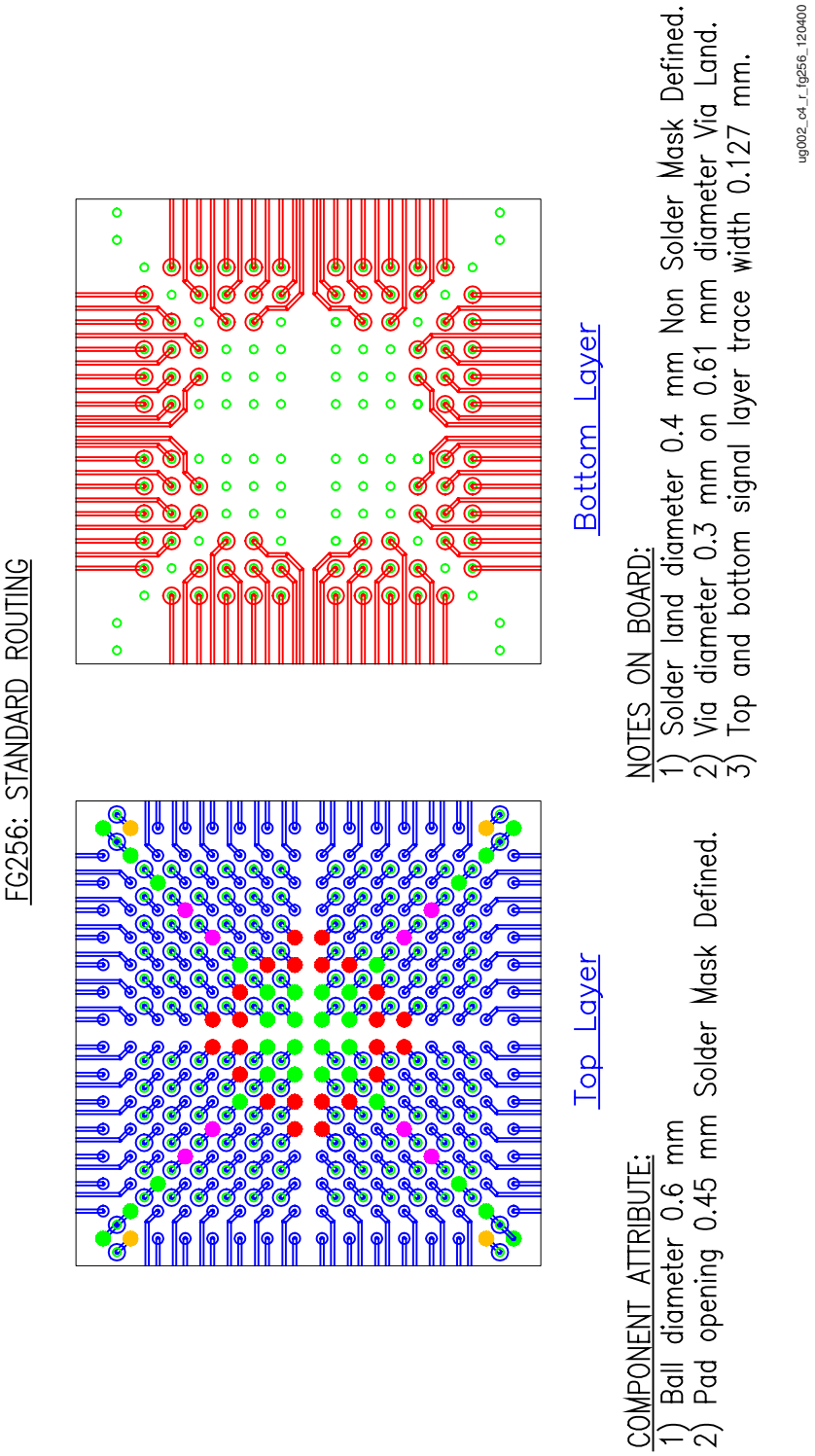


Figure 4-50: **FG256 Standard Routing**

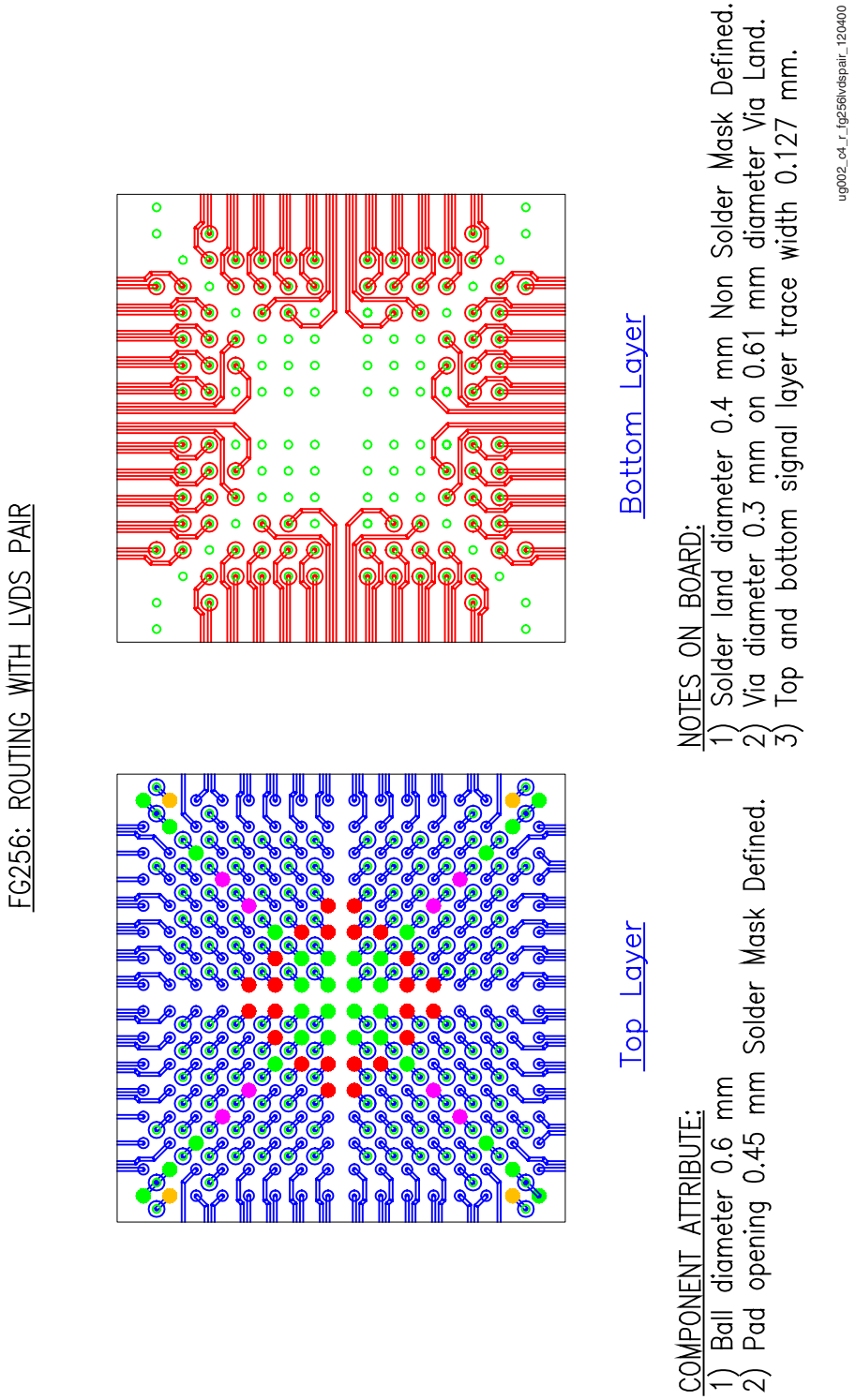


Figure 4-51: **FG256 Routing With LVDS Pairs**

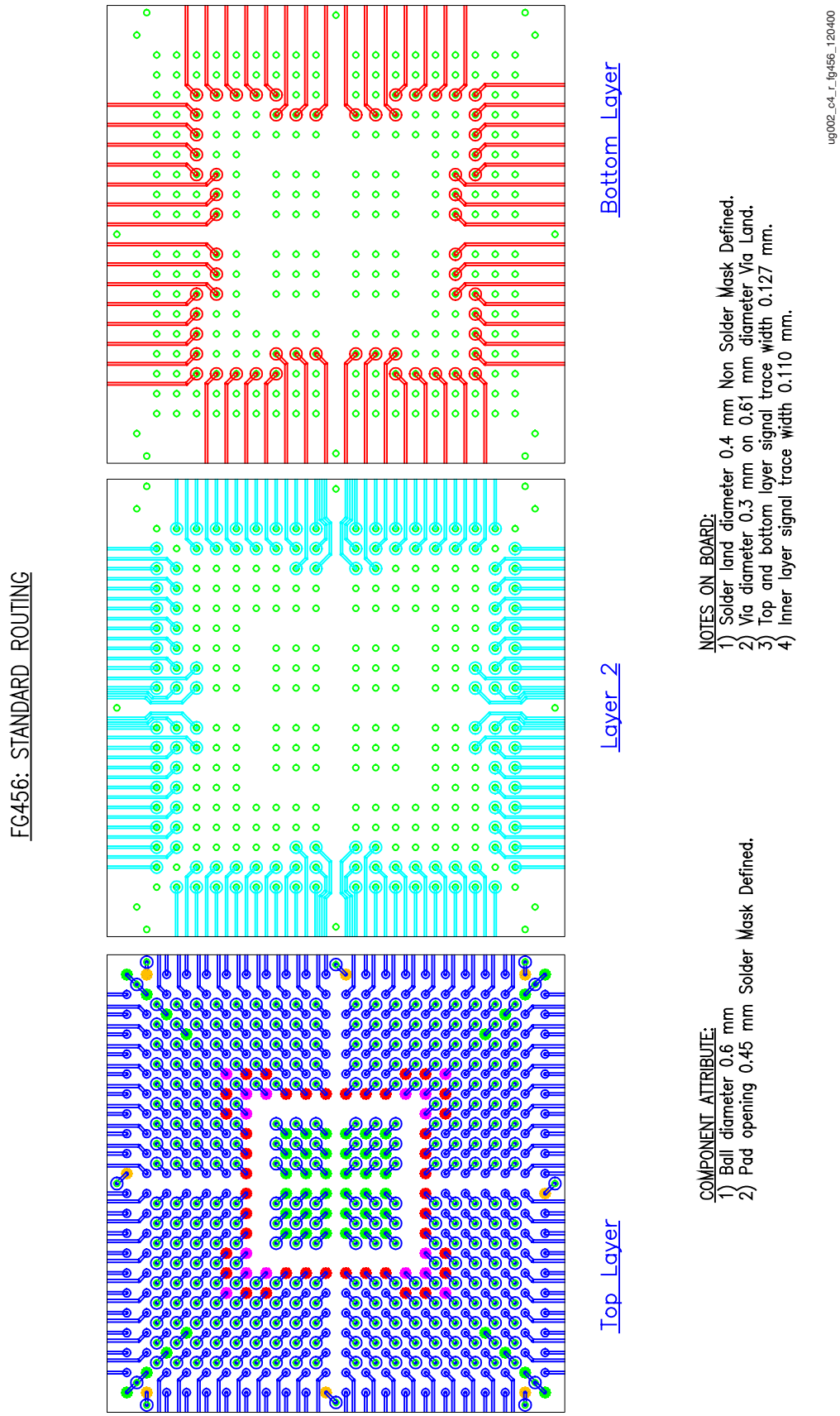


Figure 4-52: **FG456 Standard Routing**

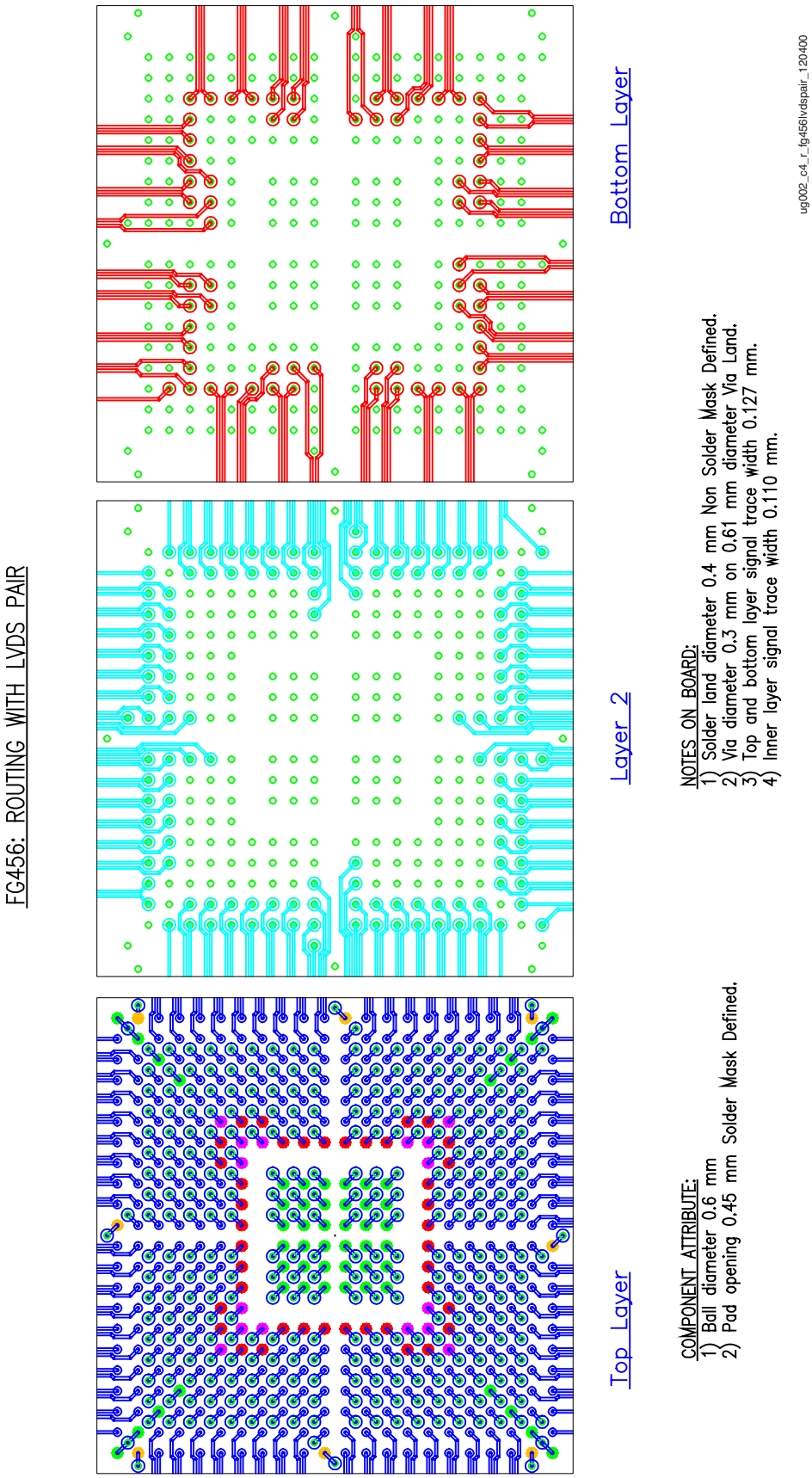


Figure 4-53: **FG456 Routing With LVDS Pairs**

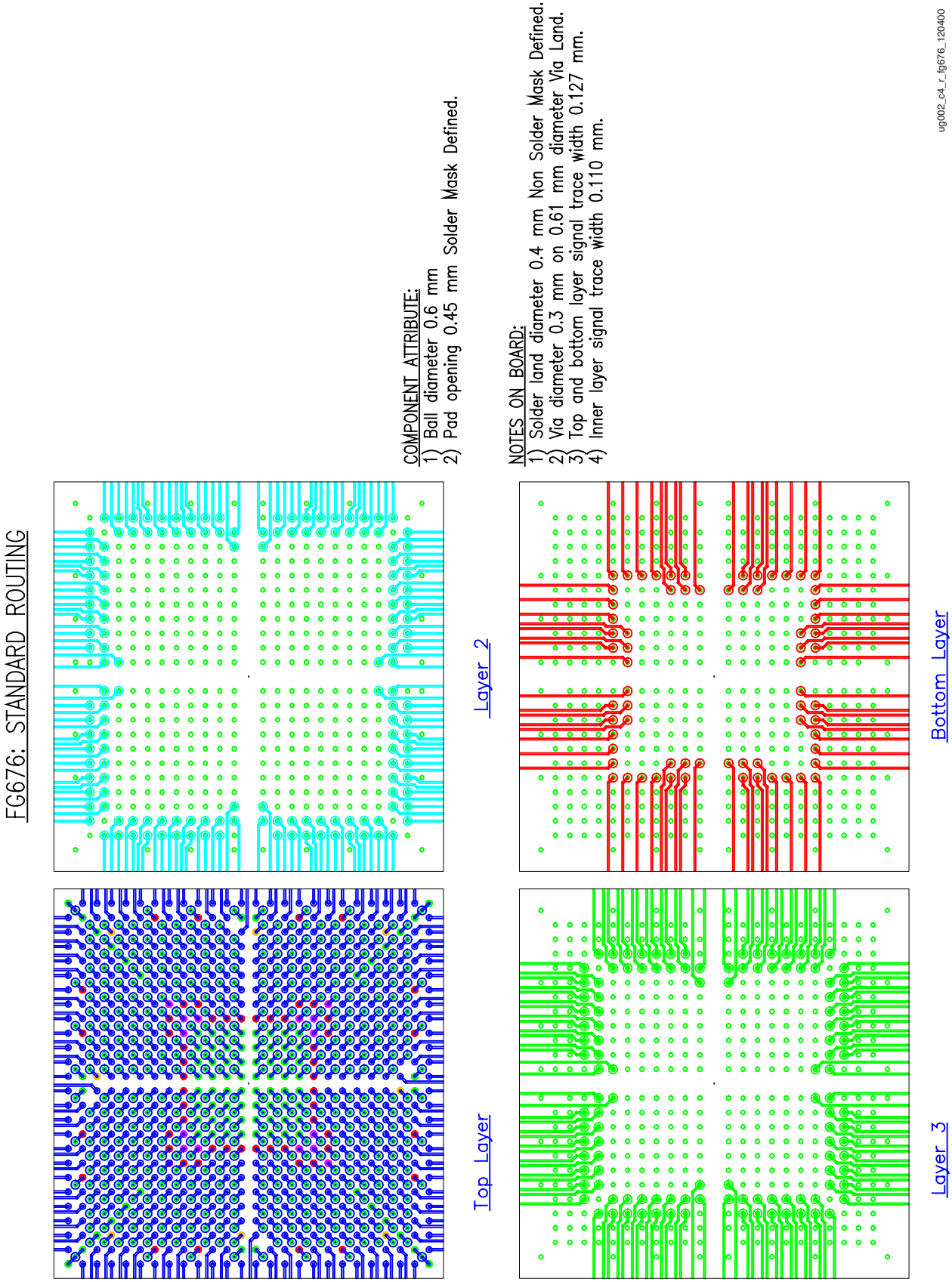


Figure 4-54: **FG676 Standard Routing**

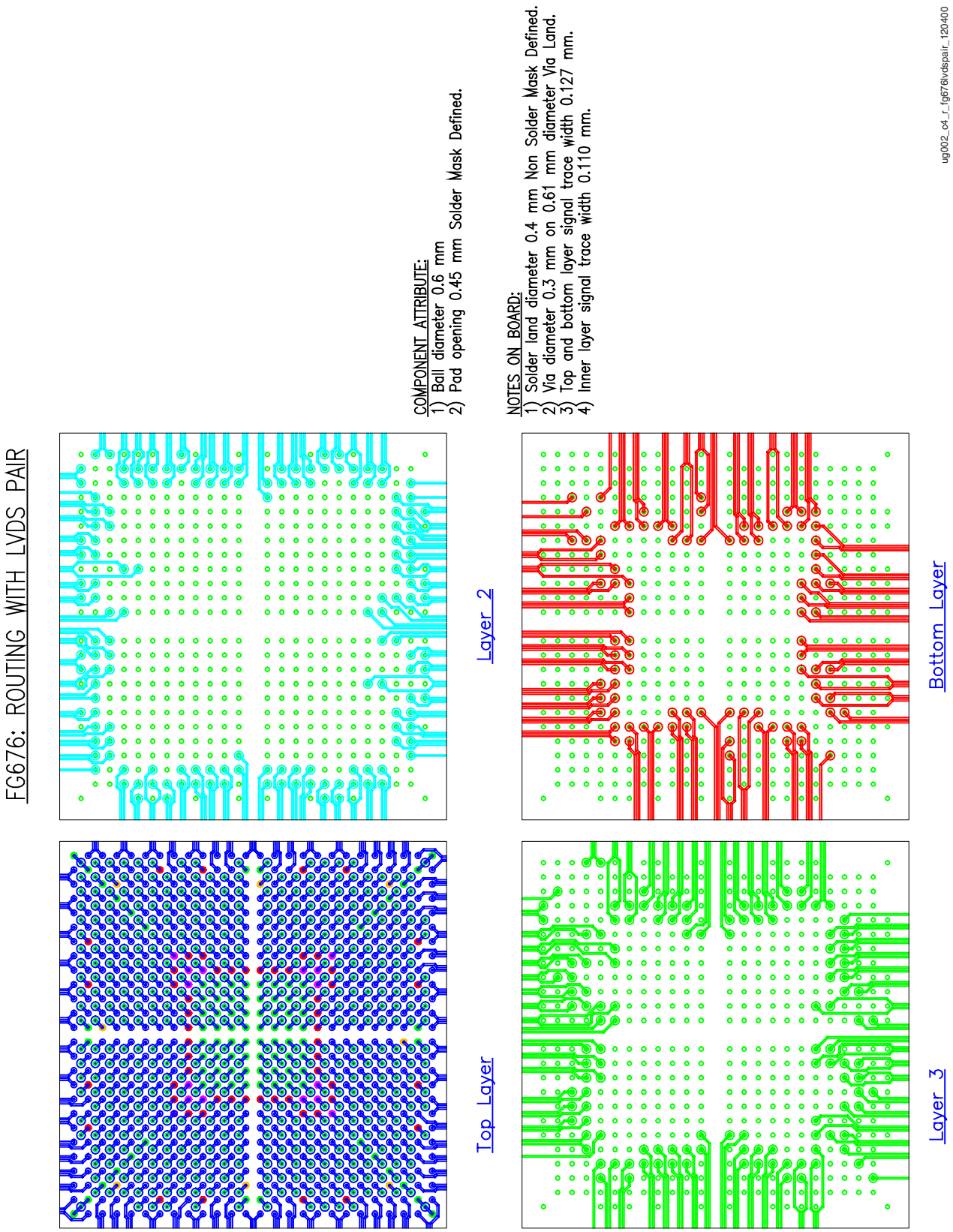


Figure 4-55: **FG676 Routing With LVDS Pairs**

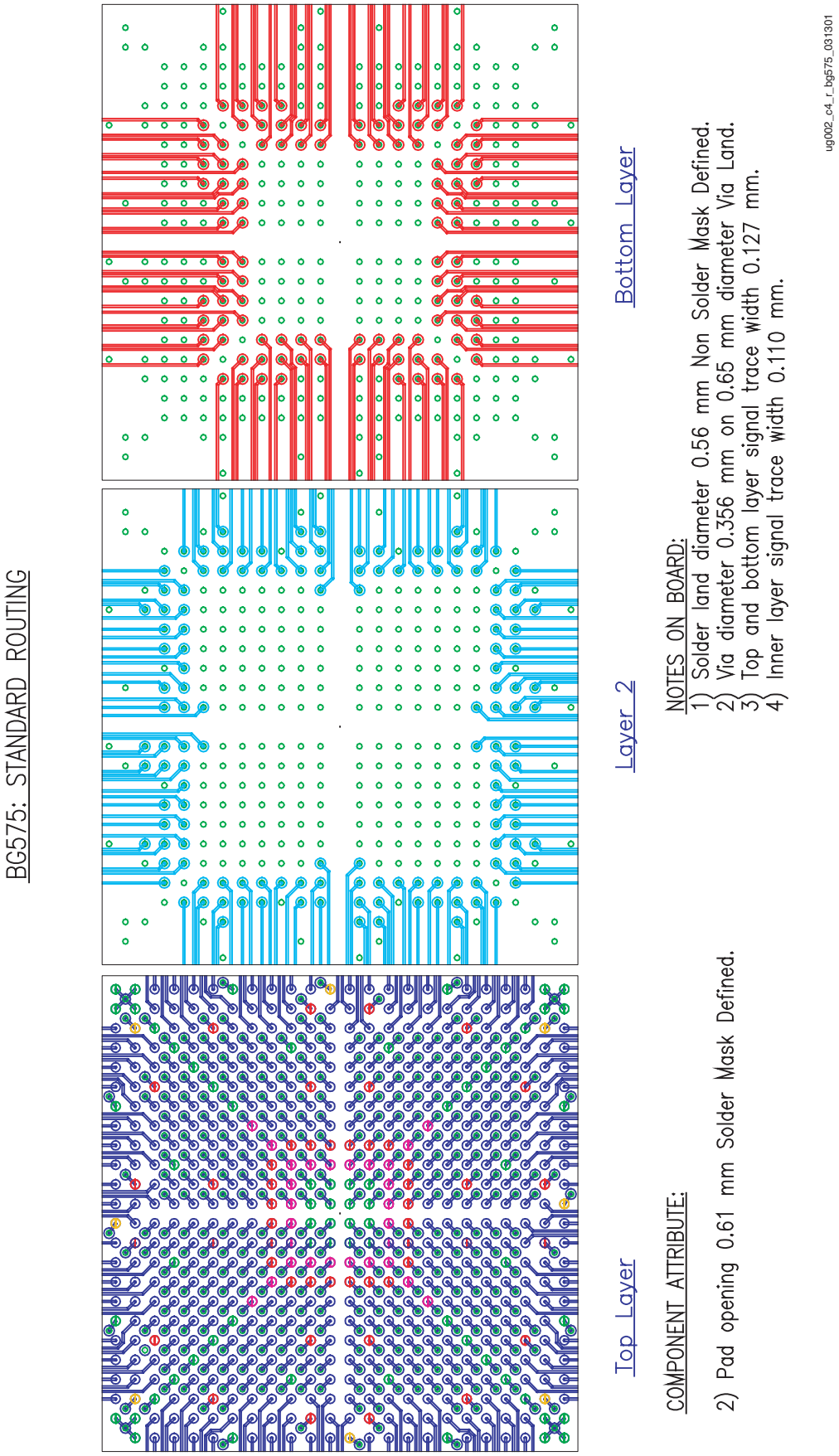


Figure 4-56: **BG575 Standard Routing**

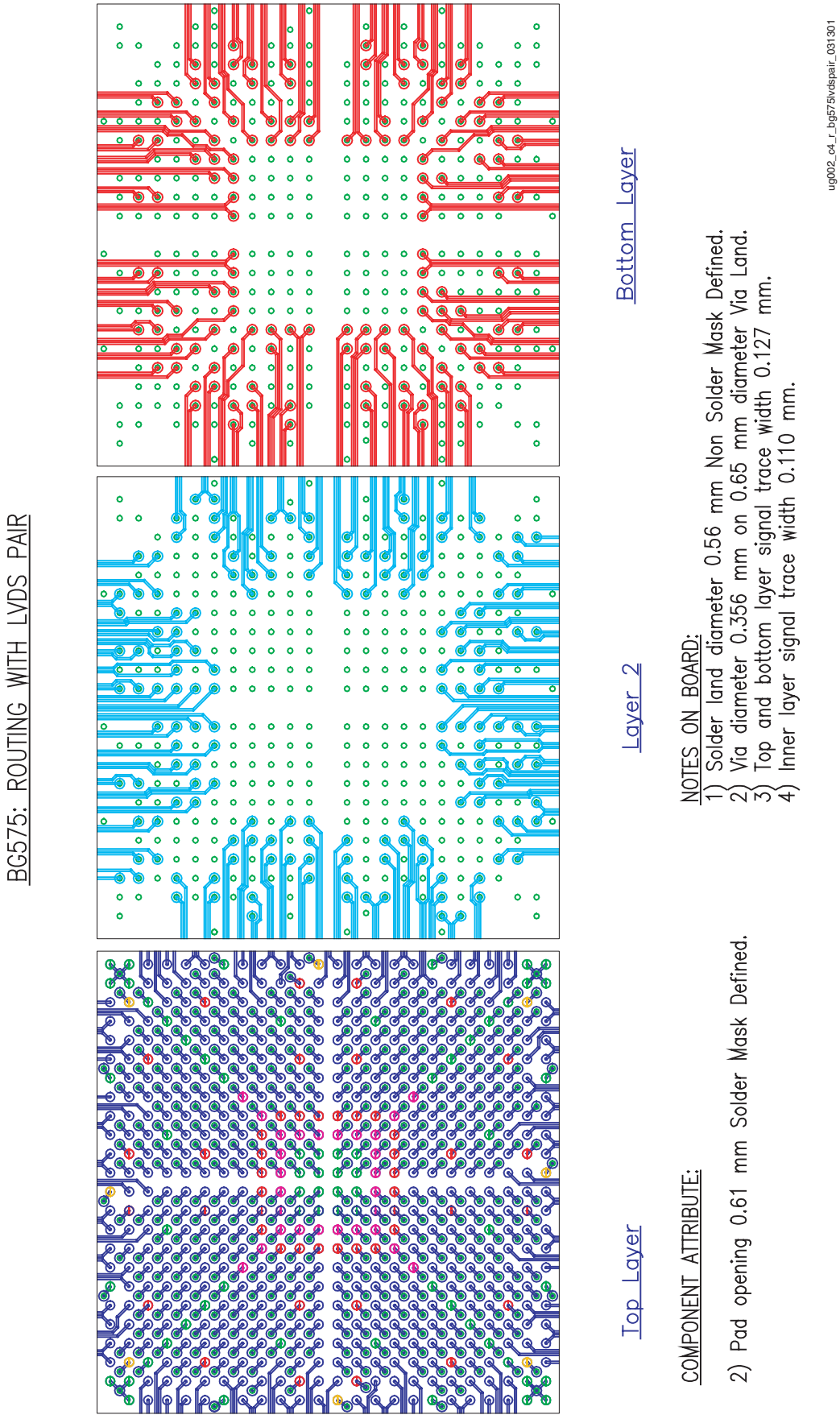


Figure 4-57: **BG575 Routing With LVDS Pairs**

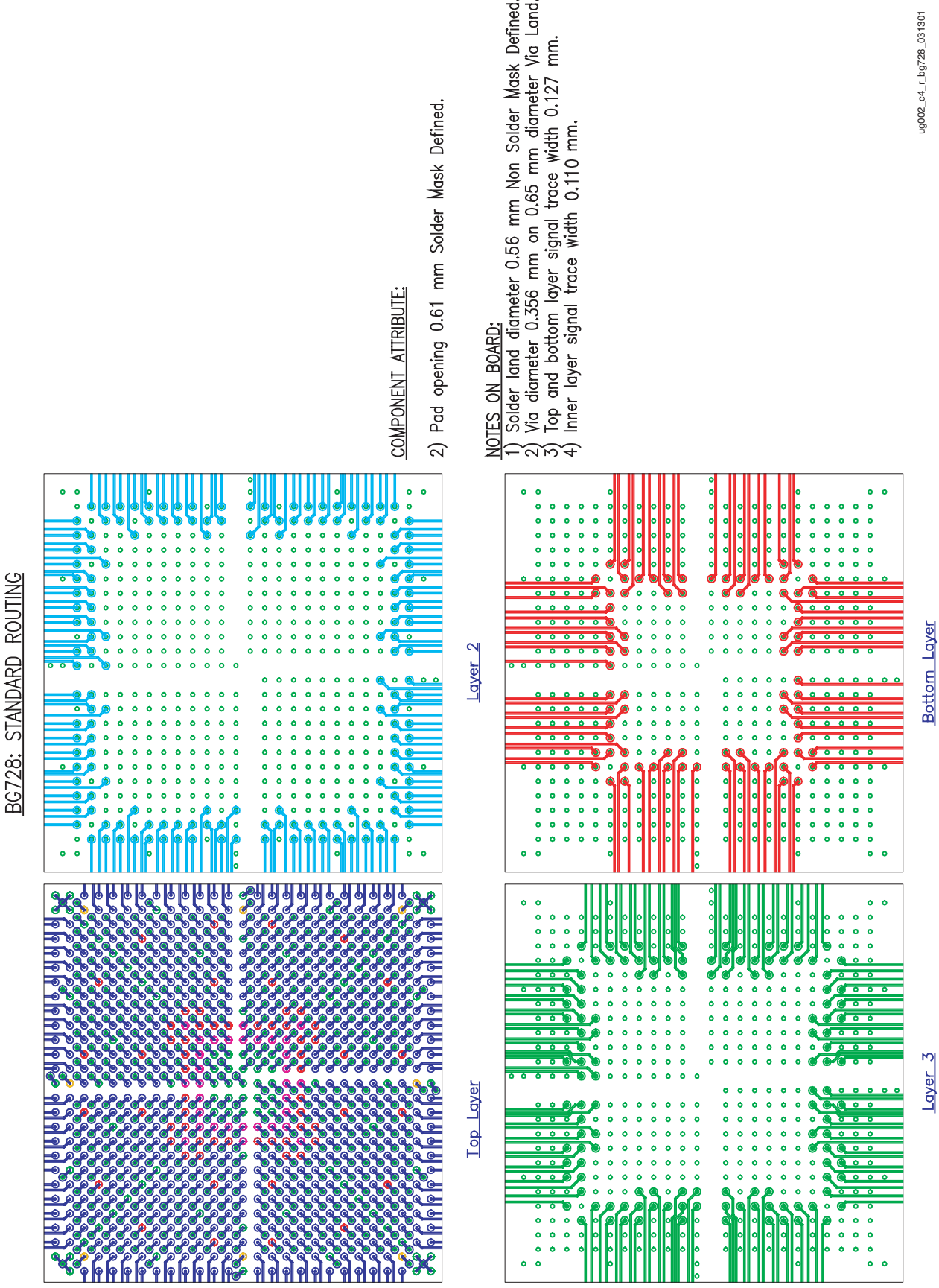


Figure 4-58: **BG728 Standard Routing**

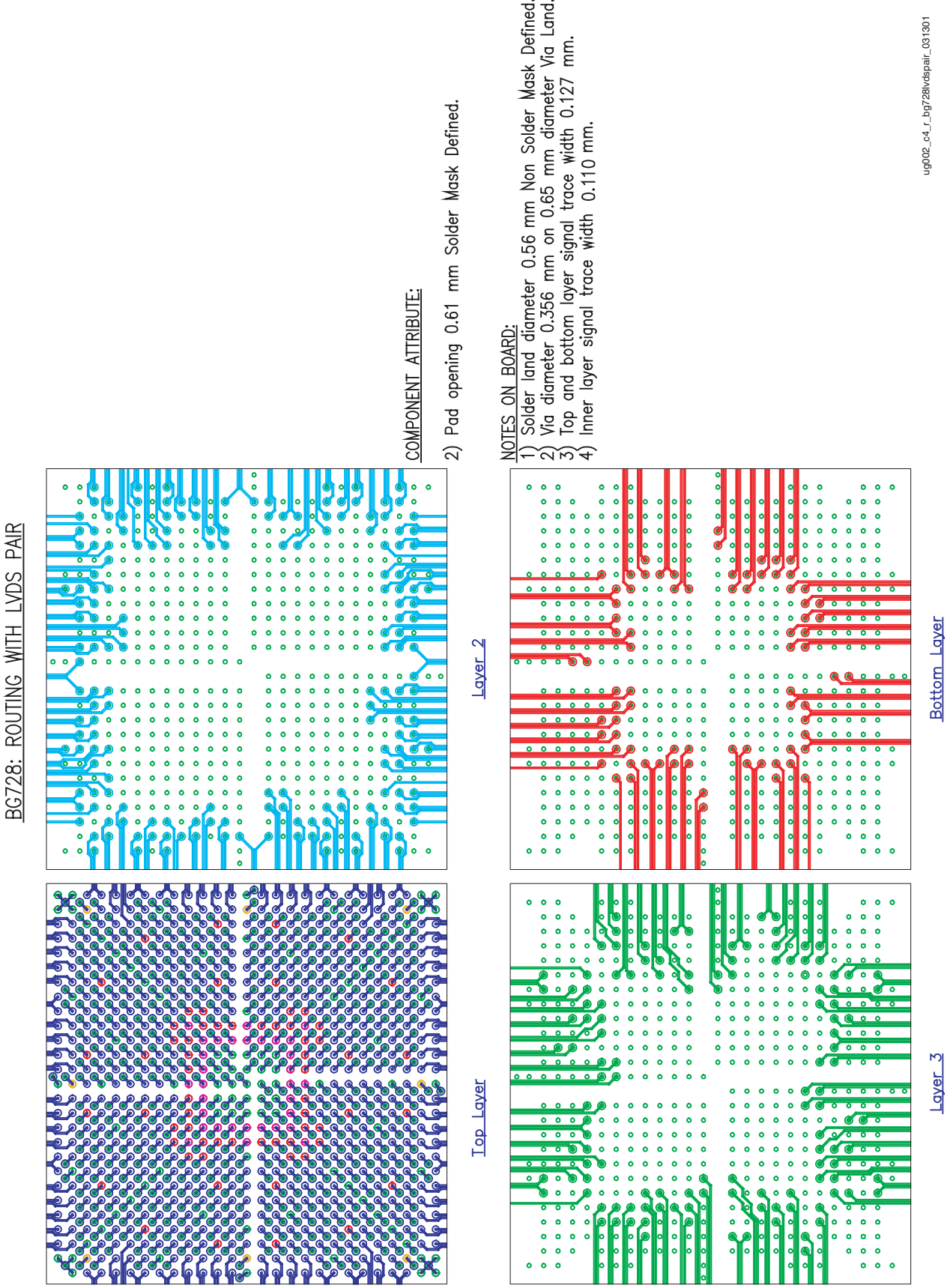


Figure 4-59: **BG728 Routing With LVDS Pairs**

Figure 4-60: **FF896 Standard Routing**

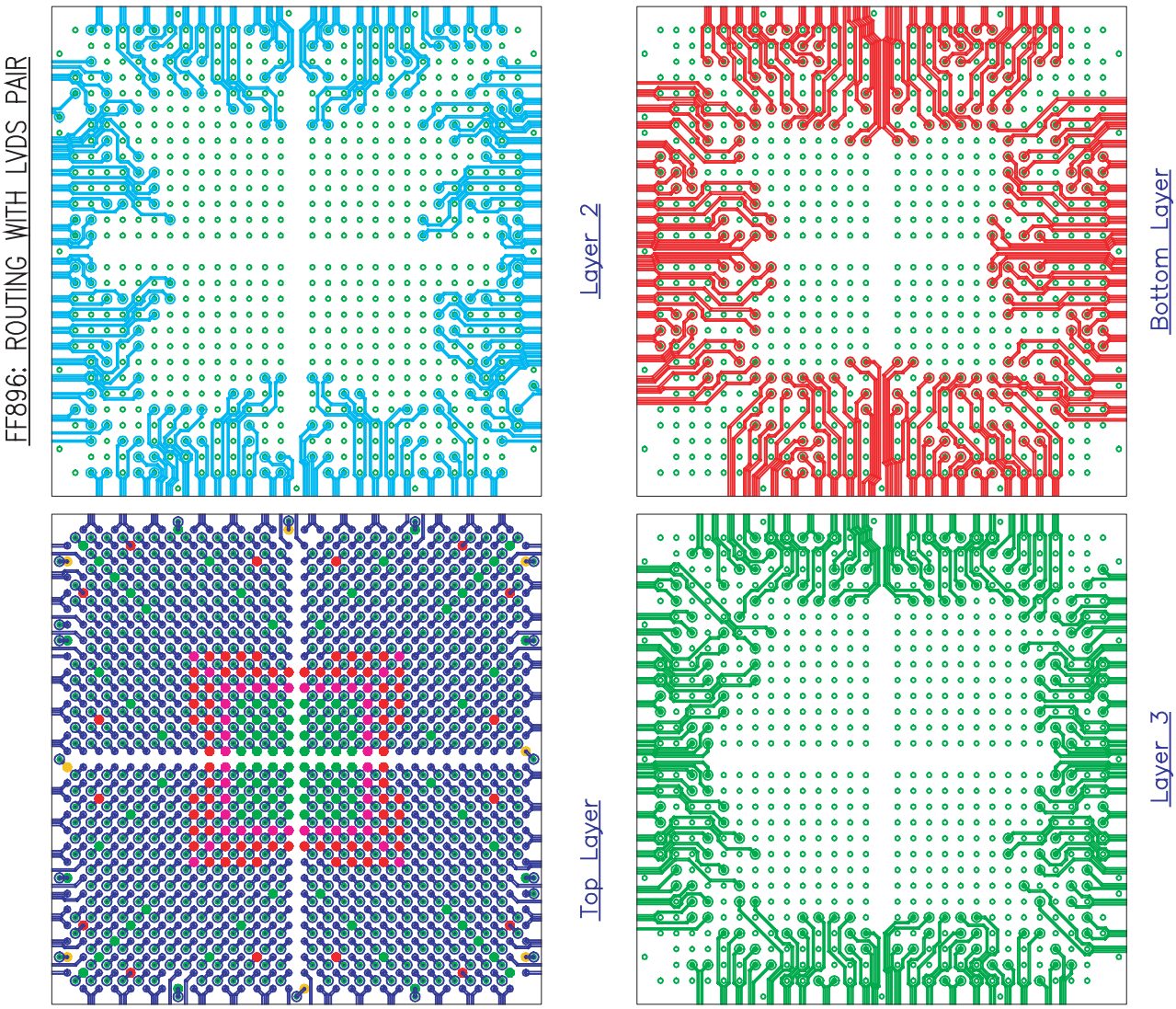


Figure 4-61: **FF896 Routing With LVDS Pairs**

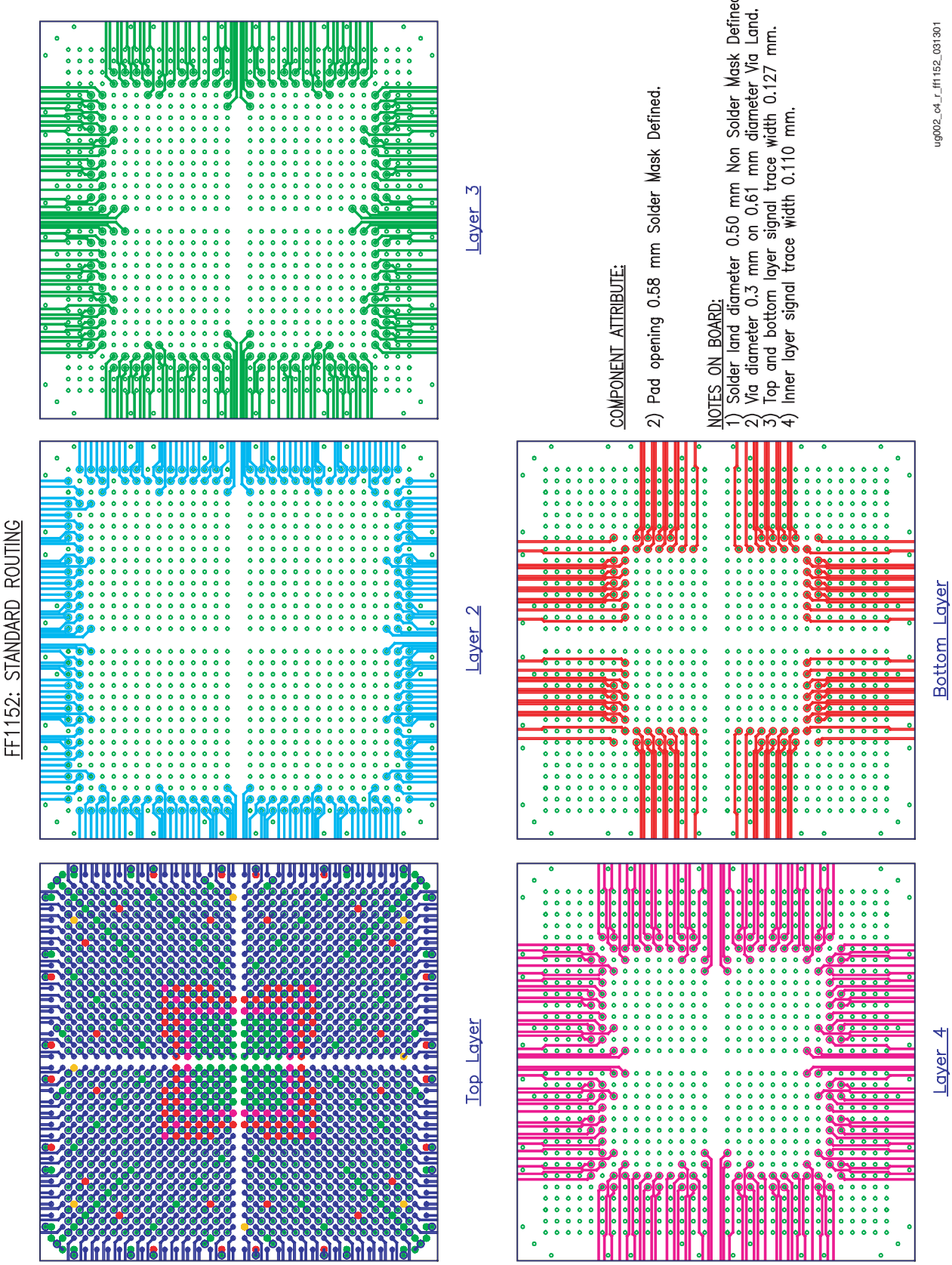


Figure 4-62: **FF1152 Standard Routing**

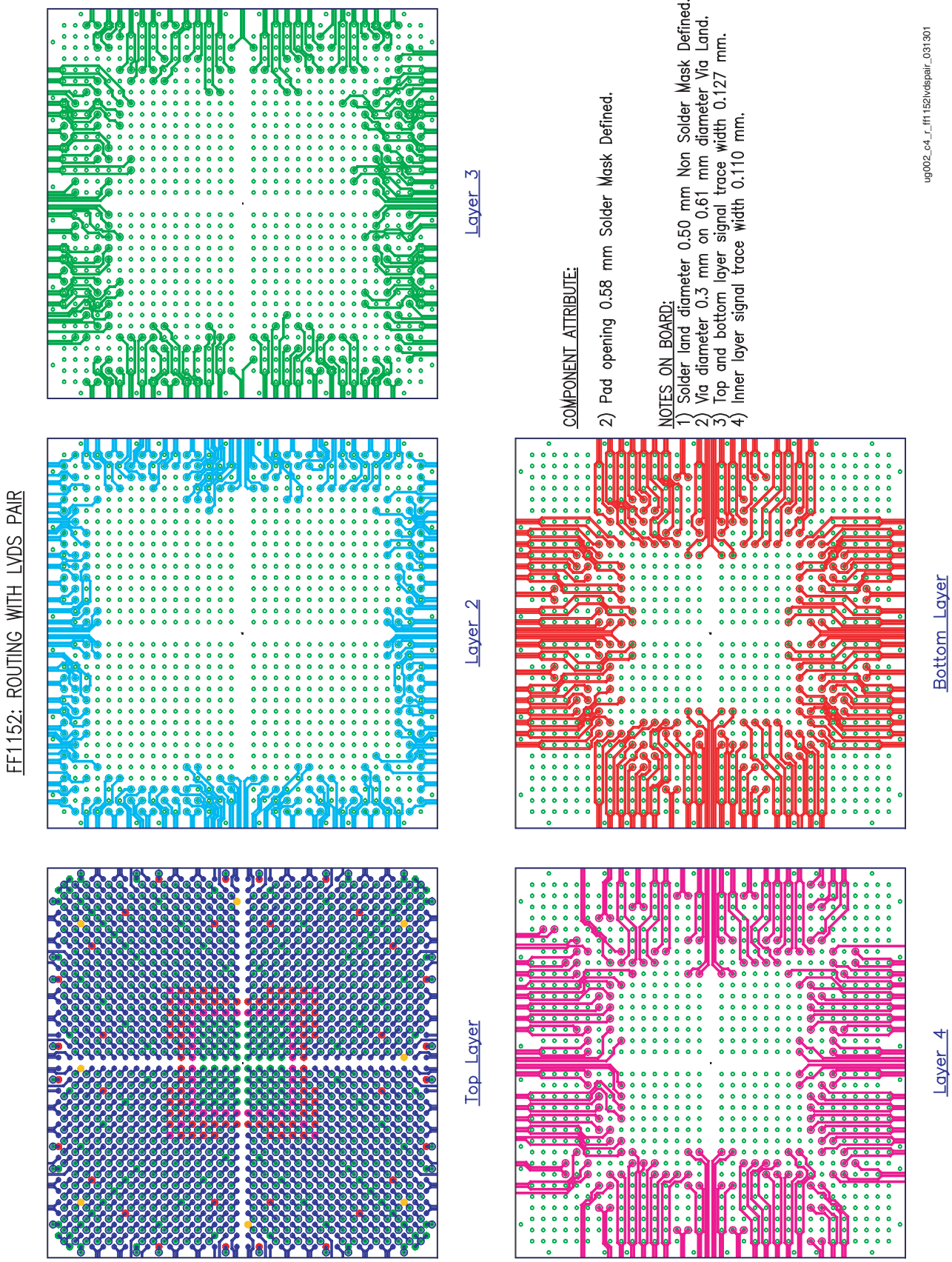


Figure 4-63: **FF1152 Routing With LVDS Pairs**

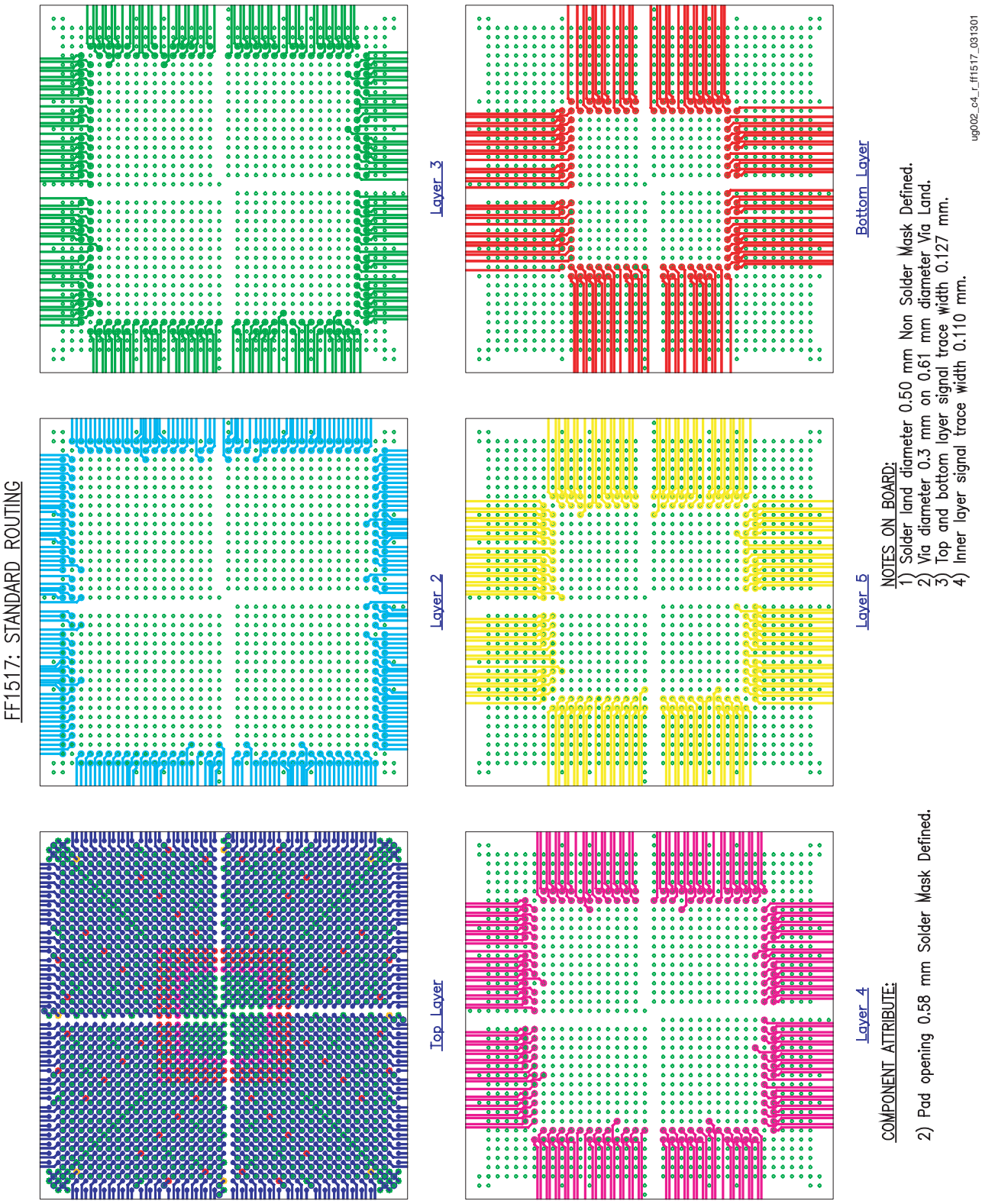


Figure 4-64: **FF1517 Standard Routing**

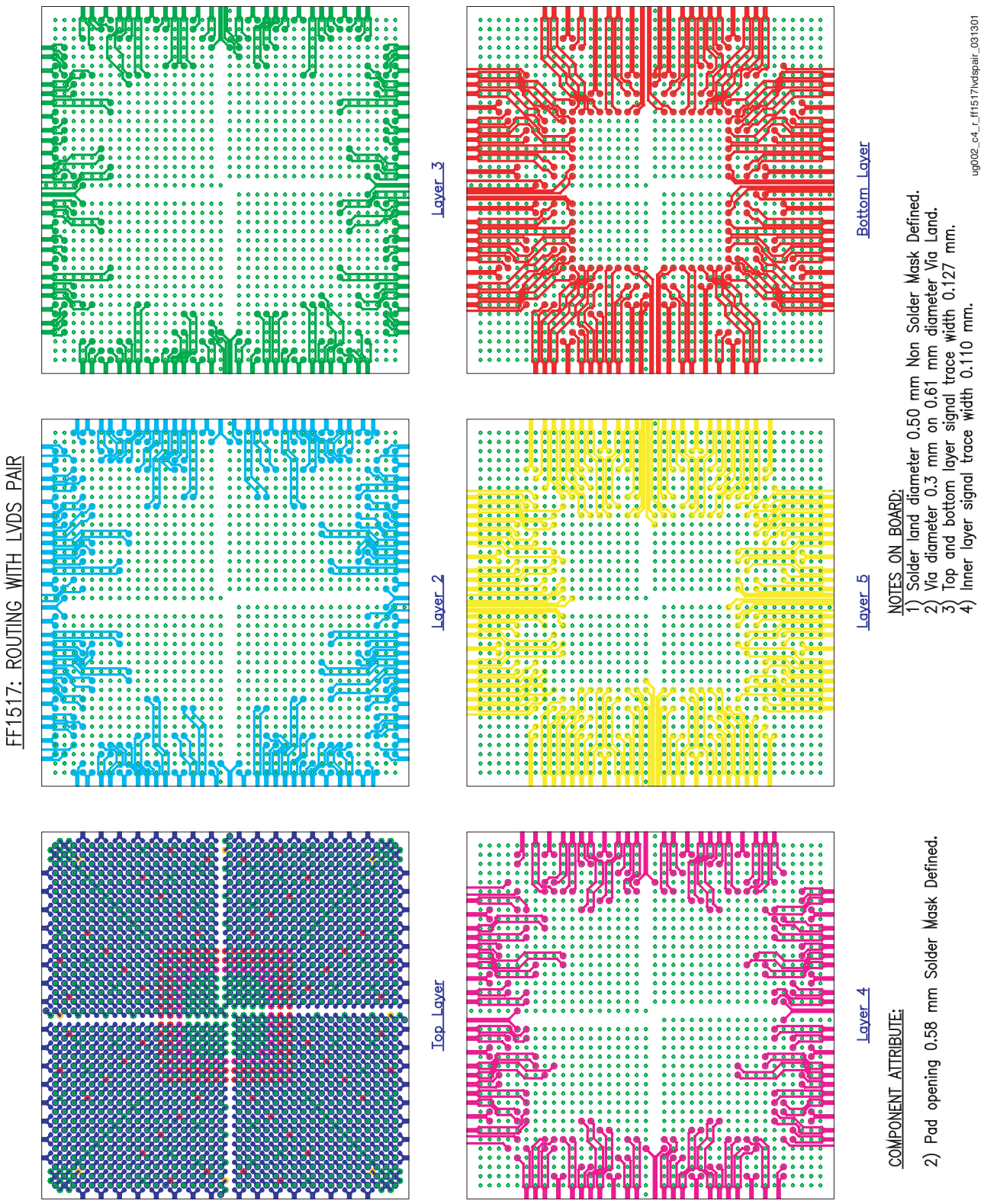


Figure 4-65: **FF1517 Routing With LVDS Pairs**

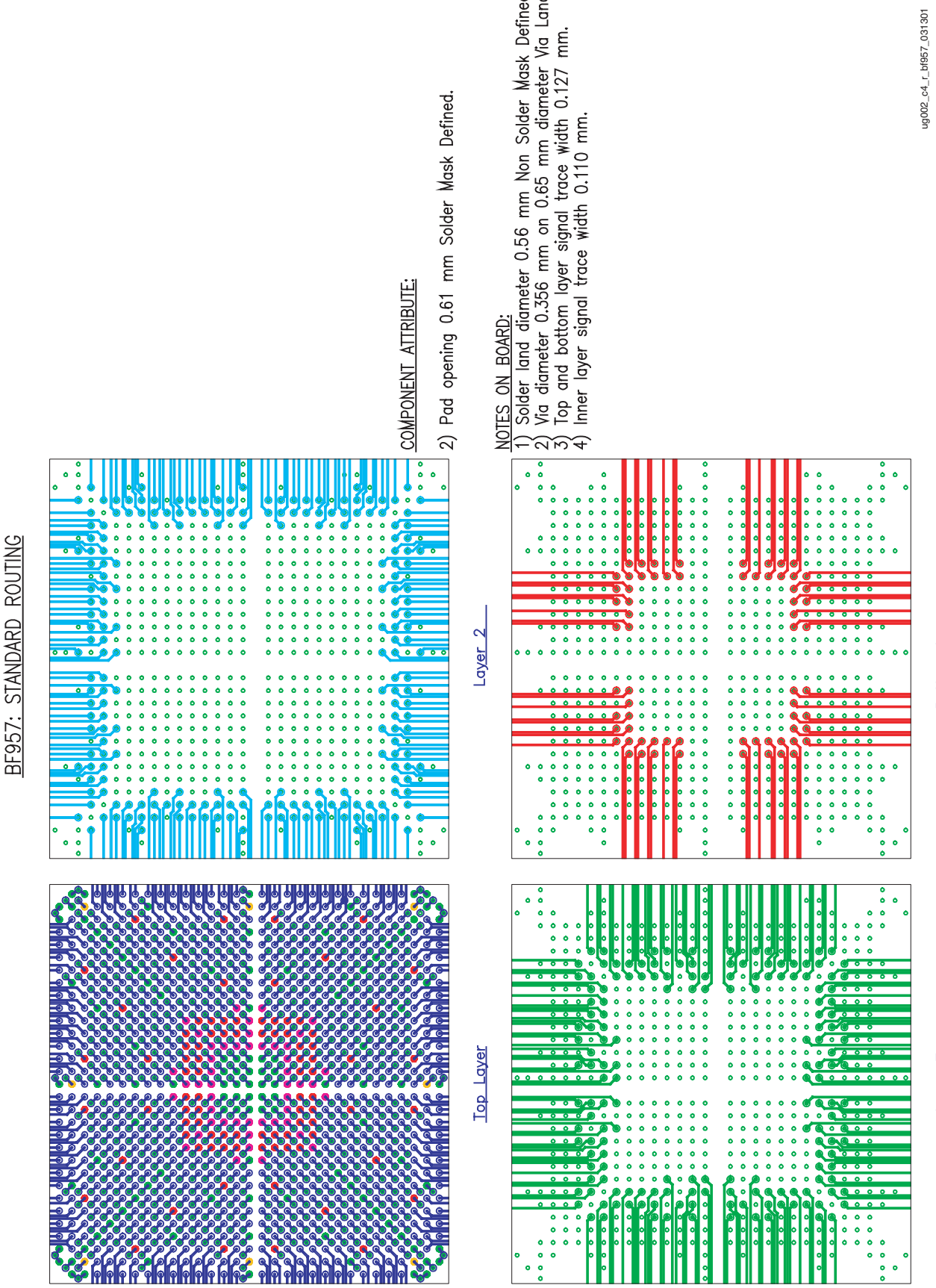


Figure 4-66: **BF957 Standard Routing**

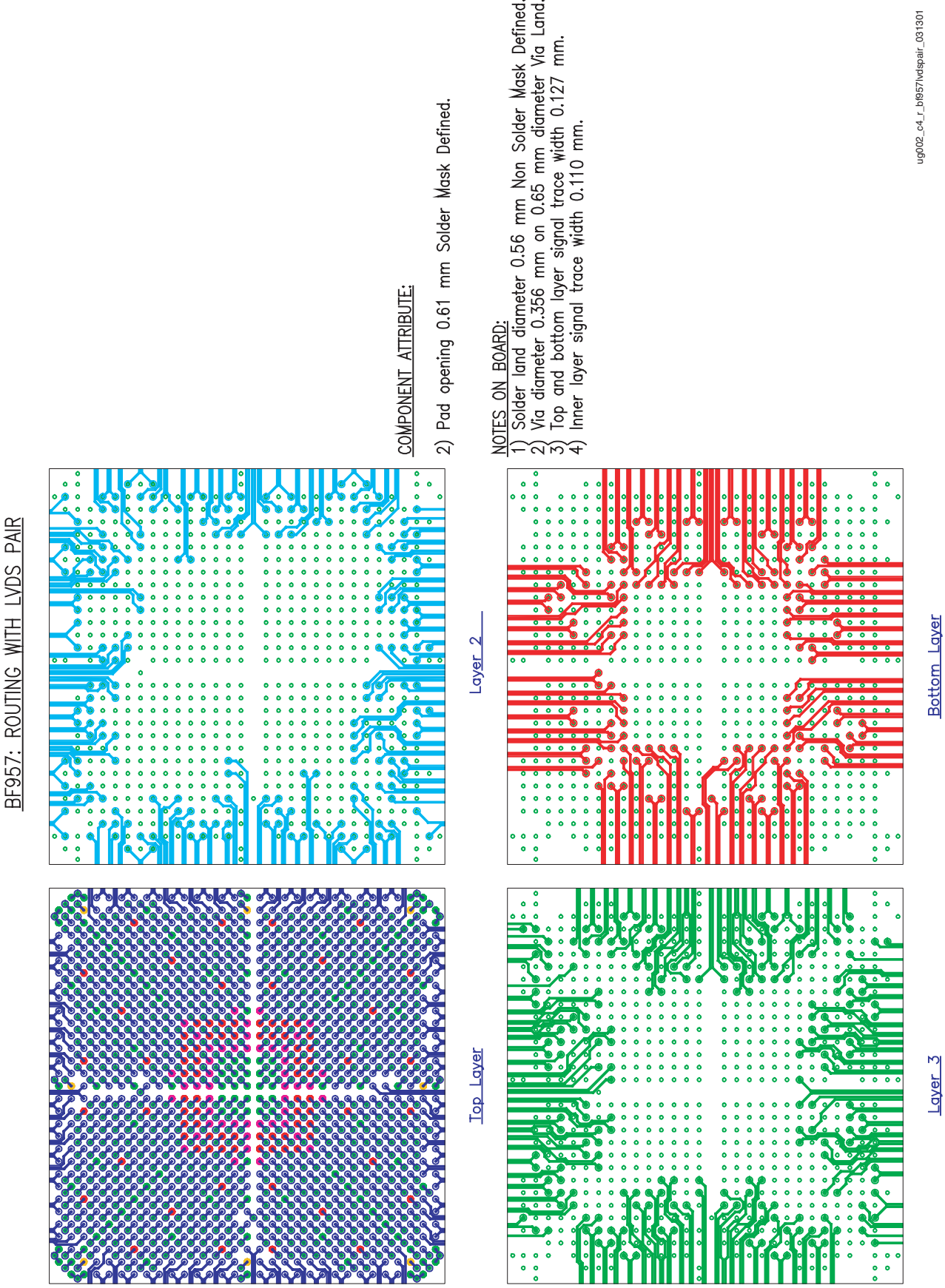


Figure 4-67: **BF957 Routing With LVDS Pairs**

Power Consumption

The Virtex-II power estimator worksheet estimates power consumption for a Virtex-II design before it is downloaded. It considers the design resource usage, toggle rates, I/O power, and many other factors in the estimation. The formulas used for calculations in the program are based on test design measurements.

Xilinx provides two versions of the power estimator, an Excel 97 version that works with Microsoft Office 97 software, and a CGI version for use with web browsers. They are identical in terms of estimations and data entries.

This section explains how to use the Power Estimator Worksheet to calculate estimated power consumption for Virtex-II designs. Since this is an estimation tool, results may not match precisely with what is measured on the board.

The power estimator consists of six categories: CLB (configurable logic block) logic power, dedicated non-multiplier power, dedicated registered multiplier power, block SelectRAM power, DCM (digital clock management), input/output power, and the results. To estimate power with the worksheet, a designer must determine how to group portions of the design into modules, what resources each module contains, the respective clock frequencies, and average toggle rates.

Note:

1. The Virtex-II power estimation is still under development. The table entries in this section may be different from the entries in the released version of the power estimation tool,

CLB Logic Power

Table 4-7 shows the data entries required for the CLB Logic Power section in the Power Estimator. This section estimates the power consumption of the CLBs for a Virtex-II design. In this section, users need to partition designs into modules, specify area utilization, and toggle rates.

Table 4-7: **CLB Logic Power**

Module	Frequency (MHz)	CLB Slices	Flip-Flops/ Latches	LUT		Average Toggle Rate (%)	Routing Amount
				Shift Register	SelectRAM		
User Module 1	0	0	0	0	0	0%	Medium
User Module 2	0	0	0	0	0	0%	Medium
User Module 3	0	0	0	0	0	0%	Medium
User Module 4	0	0	0	0	0	0%	Medium
User Module 5	0	0	0	0	0	0%	Medium
User Module 6	0	0	0	0	0	0%	Medium
User Module 7	0	0	0	0	0	0%	Medium
User Module 8	0	0	0	0	0	0%	Medium

Modules

Modules are portions of a design. A designer could treat the entire design as one module and calculate its toggle rate. However, estimating power this way is not as accurate as when the design is divided into multiple modules. Generally, with more modules the estimate is better.

The Virtex-II power estimator allows designs to be partitioned into a maximum of eight modules. Determining how to partition the design into modules depends on user preference. Three partitioning approaches are presented below as guidelines.

Grouping by Hierarchy

If a design contains hierarchical components at the top level, these components may be separated or grouped together to represent modules.

Grouping by Clocks

If a design has several different clocks, the logic associated with each clock should be treated as a module. For accuracy, it is recommended that each module contains only one clock.

Grouping by Functionality

For a design with sub-components that perform different functions, each sub-component can be considered as a module. For example, a microprocessor can be thought of as three main modules: an ALU, a Register File, and a Control System.

Frequency (MHz)

Frequency is the clock speed for the module. Again, it is strongly recommended that each module contains only one clock.

CLB Slices

This involves the total CLB usage of a module. This number is available from the synthesis report in a specific synthesis tool. For a more accurate result, MAP only this module in Xilinx Foundation software, and take the numbers from the map.mrp file. The map.mrp file is the output resource usage file produced by running the MAP program in the Xilinx Foundation software.

For schematic-based designs, obtaining this number is slightly more difficult. Designers can either estimate CLB usage based on the design structure or MAP the module and read the numbers from the map.mrp file.

Flip Flops or Latches

The total number of flip-flop and latch elements used for each module can be obtained from the synthesis report, the map.mrp file, or by adding up the registers from the schematics.

Shift Register LUTs

This is the total number of SRL16 elements used in each module.

SelectRAM LUTs

This is the total number of LUTs used as Distributed Select RAM components. For Virtex-II devices, one 16 x 1 synchronous RAM is equivalent to one LUT, and one 16 x 1 dual-port RAM is equivalent to two LUTs (split between two slices).

Average Toggle Rate (%)

The toggle rate describes how often the output changes with respect to the input clock, usually between 6% and 12% for a typical module. Functional simulation is required to accurately calculate the toggle rate. Designers need to simulate all the flip-flop outputs in each module with regard to the clock, and calculate how often the flip-flop outputs change in relation to the clock.

Measuring the toggle rate becomes a more complex and a time-consuming process as module size increases. A toggle flip-flop has a 100% toggle rate, an 8-bit counter has 28%, and 16-bit counter has 14%.

Figure 4-68 is an example of how to calculate the toggle rate for a 4-bit counter.

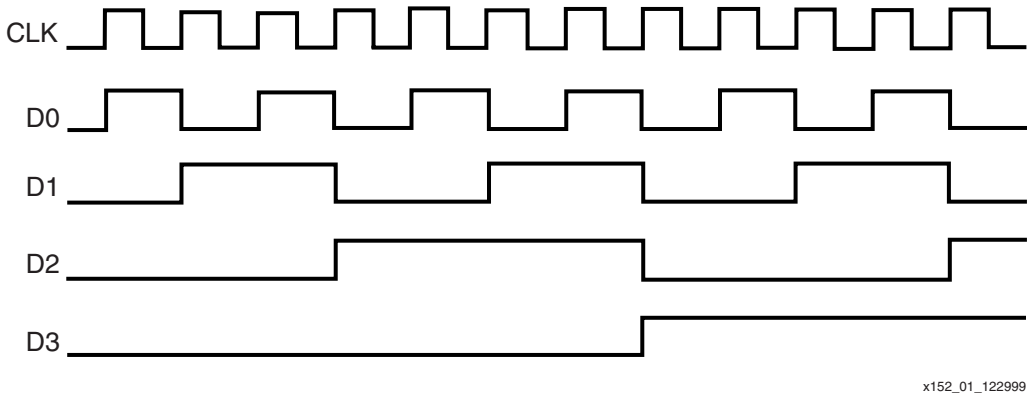


Figure 4-68: **Output Waveform of a 4-bit Counter**

Figure 4-68 shows the simulation wave form of a 4-bit counter. D0 stands for the LSB of the count, and D3 stands for the MSB. The toggle rate of D0 is 100% because D0 changes after every clock cycle. The toggle rate of D1 is 50% because D1 changes after every two clock cycles. The toggle rate of D2 is 25% because D2 changes after every four clock cycles. The toggle rate of D3 is 12.5% because D3 changes after every eight clock cycles. In this example, the average toggle rate of a 4-bit counter derived in the following equation is 46.875%.

$$\frac{(100 + 50 + 25 + 12.5)}{4} = 46.875$$

Routing Amount

There are three levels concerning the amount of routing to be used: low, medium, and high. The routing level is determined by the primary logic type of the module. Typical data path logic typically requires a low routing usage, random logic calls for a medium level, and control logic needs a high level.

Each designer needs to determine the routing that is most appropriate for each module.

Routing, which is determined by the type of logic in the module, is divided into three levels: low, medium, and high. Each designer needs to determine the routing that is most appropriate for each module.

1. Typical data path logic, which uses combinatorial logic such as multiplexers, adders, AND gates, and OR gates, usually requires a low routing usage. This also applies to any other signals that have one or two fanouts between structures.
2. Random logic, such as decoders, encoders, or any logic that has three to five fanouts, calls for a medium level of routing usage.
3. Control logic is typically logic with high fanout signals (excluding clocks) such as clock enables or reset signals. Control logic used in state machines also belongs to this category.

Block SelectRAM Power

Table 4-8 shows the data entries required for the Block SelectRAM Power section. This section is used to specify how many block RAMs are used and to determine their estimated power consumption. Before doing the calculation, designers can either treat all the RAMB16 cells as one module or break them down into smaller modules. RAMB16 is the base name for the Virtex-II Block SelectRAM component.

RAMB16 Cells

This is total number of Block Select RAMs (RAMB16 cells) used in each module.

Port A Frequency (MHz)

This is the frequency on the CLKA pin.

Port A Width

This is data width of DIA and DOA busses.

Port A Enable Rate (%)

This specifies how often ENA is enabled with respect to the clock. For a typical design, the rate may be 100% because the enable could be enabled all the time. For a FIFO design, the rate could be approximately 50% due to bursting of data into and out of the RAM.

Port B Frequency (MHz)

This is the frequency on the CLKB pin.

Port B Width

This is the data width of DIB and DOB busses.

Port B Enable Rate (%)

This specifies how often ENB is enabled with respect to the clock.

Table 4-8: **Block SelectRAM Power**

Module	RAMB16 Cells	Port A			Port B		
		Frequency (Mhz)	Width	Enable Rate (%)	Frequency (MHz)	Width	Enable Rate (%)
User Module 1	0	0	0	0	0%	0	0%
User Module 2	0	0	0	0	0%	0	0%
User Module 3	0	0	0	0	0%	0	0%
User Module 4	0	0	0	0	0%	0	0%
User Module 5	0	0	0	0	0%	0	0%
User Module 6	0	0	0	0	0%	0	0%
User Module 7	0	0	0	0	0%	0	0%
User Module 8	0	0	0	0	0%	0	0%

Digital Clock Management Power

Table 4-9 shows the data entries required for the DCM Power section and is used to estimate how much power DCMs consume. Only the clock input frequencies to the CLKIN pin needs to be entered.

Table 4-9: **Clock Delay Locked Loop Power**

Module	Clock Input Frequency (MHz)
User DCM 1	0
User DCM 2	0
User DCM 3	0
User DCM 4	0
User DCM 5	0
User DCM 6	0
User DCM 7	0
User DCM 8	0
User DCM 9	0
User DCM 10	0
User DCM 11	0
User DCM 12	0

Non-Registered Multiplier Power

The data entries for the Non-Registered Multiplier Power section are shown in Table 4-10. These entries are used to estimate Non-Registered Multiplier power consumption.

Table 4-10: **Data Entries for Non-Registered Multiplier Power**

Module	Mult18x18 Cell	Port A Width	Port B Width
User Module 1	0	0	0
User Module 2	0	0	0
User Module 3	0	0	0
User Module 4	0	0	0
User Module 5	0	0	0
User Module 6	0	0	0
User Module 7	0	0	0
User Module 8	0	0	0

Multi18x18 Cell

Multi18x18 cell is the total number of Multipliers used in each module.

Port A Width

Port A width is the data width of A busses.

Port B Width

Port B width is the data width of B busses.

Registered Multiplier Power

Data entries for the Registered Multiplier Power section are shown in Table 4-11. They are used to estimate Registered Multiplier power consumption.

Frequency

This is the frequency that the Multipliers operate at.

Multi18x18 Cell

Multi18x18 cell is the total number of Multipliers used in each module.

Port A Width

Port A width is the data width of A busses.

Port B Width

Port B width is the data width of B busses.

Average Toggle Rate

This is the toggle rate for the multiplier modules. This number can be obtained in the same way as obtaining the Average Toggle Rate in the CLB logic power section.

Table 4-11: **Data Entries for Registered Multiplier Power**

Module	Frequency (MHz)	Mult18x18 Cell	Port A Width	Port B Width	Average Toggle Rate
User Module 1	0	0	0	0	0
User Module 2	0	0	0	0	0
User Module 3	0	0	0	0	0
User Module 4	0	0	0	0	0
User Module 5	0	0	0	0	0
User Module 6	0	0	0	0	0
User Module 7	0	0	0	0	0
User Module 8	0	0	0	0	0

Input/Output Power

Table 4-12 shows the data entries for the Input/Output Power section used to estimate the power dissipation of the Inputs and Outputs. I/Os should be grouped into modules based on their I/O standard type. If the entire design has only one I/O standard type, all of the I/Os can be treated as one module. However, separating the I/Os into smaller modules makes it easier to obtain more accurate results.

Frequency (MHz)

This is the frequency of the module.

I/O Standard Type

This is the type of I/Os used in the module. Each module can have only one I/O standard type. I/O power is strongly influenced by the I/O standard used.

Inputs

This is the total number of the input buffers in each module.

Outputs

This is the total number of the output buffers in each module.

Average Output Toggle Rate (%)

This number can be obtained in the same way as obtaining the Average Toggle rate in the CLB Logic Power section.

Average Output Load (pF)

This specifies the average capacitive load on the outputs.

Table 4-12: **Data Entries for Input/Output Power**

Module	Frequency (MHz)	I/O Standard Type	Inputs	Outputs	Average Output Toggle Rate (%)	Average Output Load (pF)
User Module 1	0	LVTTL_12	0	0	0%	0
User Module 2	0	LVTTL_12	0	0	0%	0
User Module 3	0	LVTTL_12	0	0	0%	0
User Module 4	0	LVTTL_12	0	0	0%	0
User Module 5	0	LVTTL_12	0	0	0%	0
User Module 6	0	LVTTL_12	0	0	0%	0
User Module 7	0	LVTTL_12	0	0	0%	0
User Module 8	0	LVTTL_12	0	0	0%	0

Results

The results section of the power estimator are shown in Table 4-13. The four sections of the power estimator program independently estimate power consumption, and the results are displayed at the end of each section.

The total design power consumption is the summation of those, and is displayed at the very top of the program.

Table 4-13: **Power Estimator Results**

Target		Estimated Design Power Values (mW)					
Device	Package	Total Power	V_{CCINT} 1.5 V	V_{CCO} 3.3 V	V_{CCO} 2.5 V	V_{CCO} 1.5 V	Output Sink Power
XC2V500	FG256	0	0	0	0	0	0

Target Device

This refers to the target Virtex-II device size.

Note: No checking is done to verify that the module entries fit into the amount of resources available in the selected devices.

Target Package

This refers to the package of the device.

Note: No checking is done to verify that the selected device-package combination is valid.

Estimated Total Power

This section displays the total power consumption of the design. It is the summation of CLB Logic power, Block Select RAM power, Multiplier power, DCM power, and Input/Output power.

Estimated V_{CCINT} 1.5V Power

This section displays the total power consumption from the core supply voltage (V_{CCINT}). It does not include the power consumption from the input and output source voltage (V_{CCO}).

Estimated V_{CCAUX} 3.3V Power

This section displays the power consumption from auxiliary circuits.

Estimated V_{CCO} 3.3V Power

This section displays the V_{CCO} power consumption of 3.3 V applications. The I/O standards that use 3.3V V_{CCO} are LVTTL, LVCMOS33 PCI, SSTL3 Class I and II, and AGP2X.

Estimated V_{CCO} 2.5V Power

This section displays the V_{CCO} power consumption of 2.5 V applications. The supported I/O standards are LVCMOS25 and SSTL2 Class I and II.

Estimated V_{CCO} 1.5V Power

This section displays the V_{CCO} power consumption of 1.5 V applications. The supported I/O standards are LVCMOS15, and HSTL Class I, II, III, and IV.

Estimated Output Sink Power

This section displays the power consumption when sinking current to ground. The supported I/O standards are GTL and GTL+.

IBIS Models

The need for higher system performance leads to faster output transitions. Signals with fast transitions cannot be considered purely digital; it is important to understand their analog behavior for signal integrity analysis.

To simulate the signal integrity on printed circuit boards (PCB) accurately and solve design problems before the PCB is fabricated, models of the I/O characteristics are required. SPICE models are most frequently used for this purpose. A manufacturer's SPICE models, however, contain proprietary circuit-level information. Therefore, simpler models are devised to extract SPICE parameters for the proprietary information to remain protected. One such standard is the I/O Buffer Information Specification (IBIS) format originally suggested by Intel.

In the early 1990's, the IBIS Open Forum was formed and the first IBIS specification was written to promote tool independent I/O models for system signal integrity analysis.

IBIS is now the ANSI/EIA-656 and IEC 62014-1 standard. IBIS accurately describes the signal behavior of the interconnections without disclosing the actual technology and circuitry used to implement the I/O. The standard is basically a black-box approach to protecting proprietary information.

Using IBIS Models

IBIS models are used by designers for system-level analysis of signal integrity issues, such as the evaluation and matching of loads to drivers for ringing and ground bounce, examining effects of cross talk, and predicting RFI/EMI. It is useful in that complete designs can be simulated and evaluated before additional costs are incurred for PCB fabrication and assembly time.

IBIS models consist of look-up tables that predict the I/V characteristics and dV/dt of integrated circuit inputs and outputs when combined with the PCB wiring. The predictions are performed for the typical case, minimum case (weak transistors, low V_{CC}, hot temperatures), and maximum case (strong transistors, high V_{CC}, cold temperatures).

IBIS models have limitations in that they do not contain internal delay modeling and are limited in package modeling. IBIS models contain package parasitic information for simulation of ground bounce. Although the data is available within the model file, not all simulators are able to use the data to simulate ground bounce. Simulation results may not agree with the actual results due to package, die, and PCB ground plane modeling problems. Similarly, because simultaneous switching outputs (SSOs) are also difficult to model, only a first approximation is provided to the designer.

IBIS Generation

IBIS is generated either from SPICE simulations, or actual measurements of final devices. IBIS models that are derived from measurements do not have process corner information, unlike IBIS models that are derived from SPICE simulations. The measurements are of only a few parts, and the extremes of production are not represented by such a method.

SPICE is a transistor model based on detailed equations using device geometry, and properties of materials. A SPICE netlist of the CMOS buffer is required for V/I and dV/dt curve simulations. These SPICE simulations are then converted to IBIS format/syntax.

Advantages of IBIS

SPICE requires a greater knowledge of the internal workings of the circuits being modeled, and as such, errors may be made in simulation indicating a problem when there is none. IBIS models are easy to use, and because many of the decisions required for simulation parameters have been organized. IBIS simulations are faster compared to SPICE simulations, because IBIS does not contain circuit details. The voltage/current/time information provided in the IBIS model is only for the external nodes of the building block, making IBIS ideal for system-level interconnects design. Although IBIS models are not as accurate as SPICE models, they are entirely adequate for system-level analysis.

IBIS File Structure

An IBIS file contains two sections, the header and the model data for each component. One IBIS file can describe several devices. The following is the contents list in a typical IBIS file:

- IBIS Version
- File Name
- File Revision
- Component
- Package R/L/C
- Pin - name, model, R/L/C
- Model (i.e., 3-state)
- Temperature Range (typical, minimum, and maximum)
- Voltage Range (typical, minimum, and maximum)
- Pull-Up Reference
- Pull-Down Reference
- Power Clamp Reference
- Ground Clamp Reference
- V/I Tables for:
  - Pullup
  - Pulldown
  - Power Clamp
  - Ground Clamp
- Rise and Fall dV/dt for minimum, typical, and maximum conditions (driving 50 ohms)
- Package Model (optional) XXXX.pkg with RLC sections.

IBIS I/V and dV/dt Curves

A digital buffer can be measured in receive (3-state mode) and drive mode. IBIS I/V curves are based on the data of both these modes. The transition between modes is achieved by phasing in/out the difference between the driver and the receiver models, while keeping the receiver model constantly in the circuit.

The I/V curve range required by the IBIS specification is $-V_{CC}$ to ($2 \times V_{CC}$). This wide voltage range exists because the theoretical maximum overshoot due to a full reflection is twice the signal swing. The ground clamp I/V curve must be specified over the range $-V_{CC}$ to V_{CC}, and the power clamp I/V curve must be specified from V_{CC} to ($2 \times V_{CC}$).

The three supported conditions for the IBIS buffer models are typical values (required), minimum values (optional), and maximum values (optional). For CMOS buffers, the minimum condition is defined as high temperature and low supply voltage, and the maximum condition is defined as low temperature and high supply voltage.

An IBIS model of a digital buffer has four I/V curves:

- The pull-down I/V curve contains the mode data for the driver driving low. The origin of the curve is at 0 V for CMOS buffers.
- The pull-up I/V curve contains the mode data for the driver driving high. The origin of the curve is at the supply voltage (V_{CC} or V_{DD}).
- The ground clamp I/V curve contains receive (3-state) mode data, with the origin of the curve at 0 V for CMOS buffers.

- The power clamp I/V curve contains receive (3-state) mode data, with the origin of the curve at the supply voltage (V_{CC} or V_{DD}). For 3.3 V buffers that are 5 V tolerant, the power clamp is referenced to 5 V while the pullup is referenced to 3.3 V.

Ramp and dV/dt Curves

The Ramp keyword contains information on how fast the pull-up and pull-down transistors turn on/off. The dV/dt curves give the same information, while including the effects of die capacitance (C_comp). C_comp is the total die capacitance as seen at the die pad, excluding the package capacitance.

dV/dt curves describe the transient characteristics of a buffer more accurately than ramps. A minimum of four dV/dt curves is required to describe a CMOS buffer: pull-down ON, pull-up OFF, pull-down OFF, and pull-up ON. dV/dt curves incorporate the clock-to-out delay, and the length of the dV/dt curve corresponds to the clock speed at which the buffer is used. Each dV/dt curve has t = 0, where the pulse crosses the input threshold.

IBIS Simulations

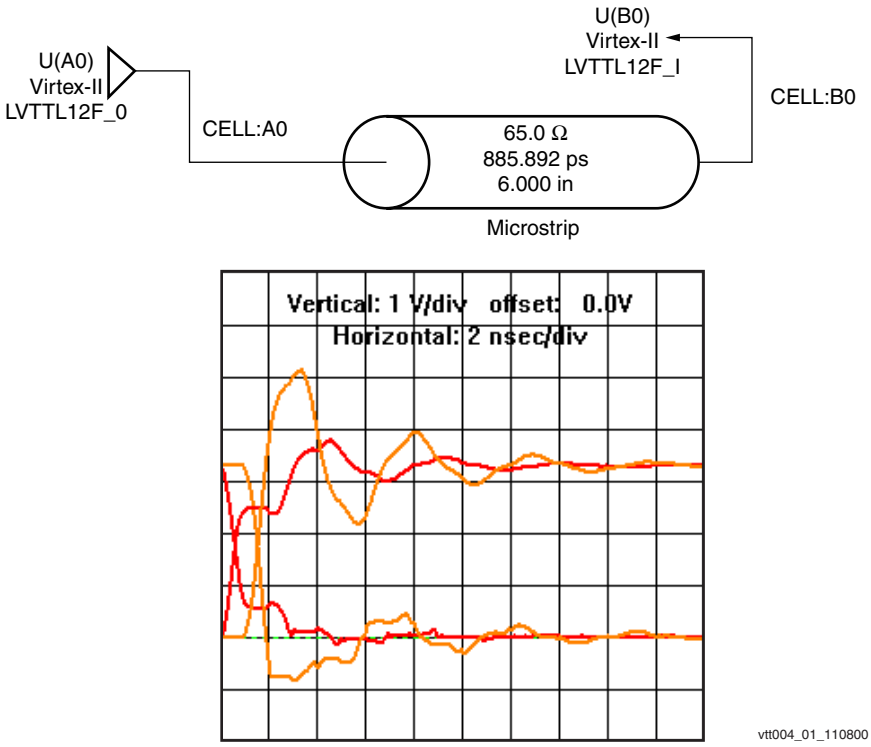


Figure 4-69: **Unterminated Example**

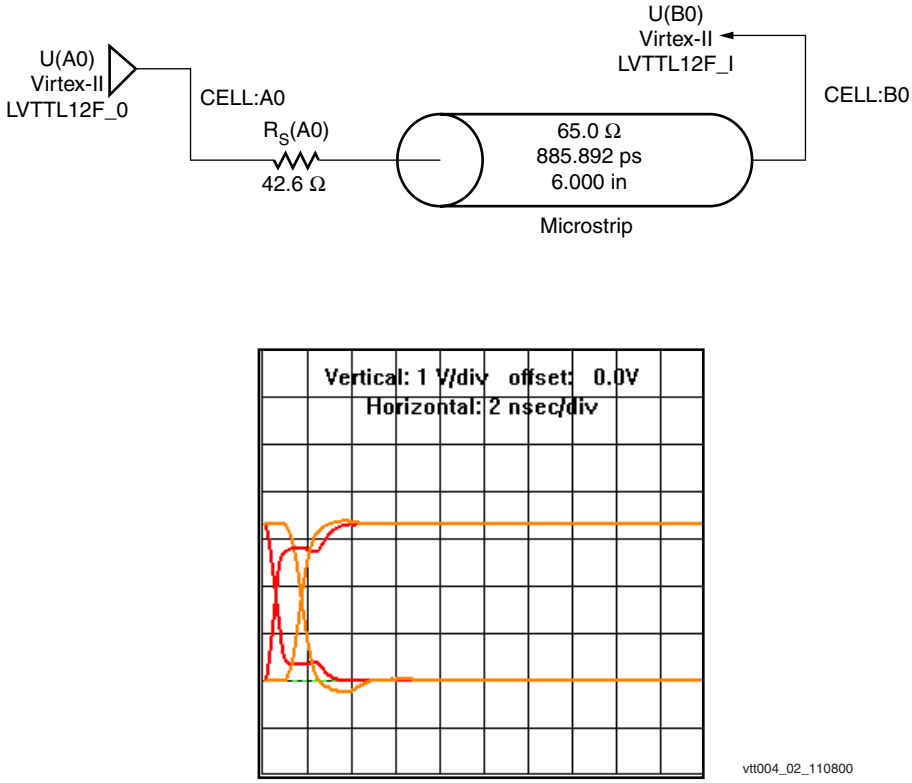


Figure 4-70: **Series Termination Example**

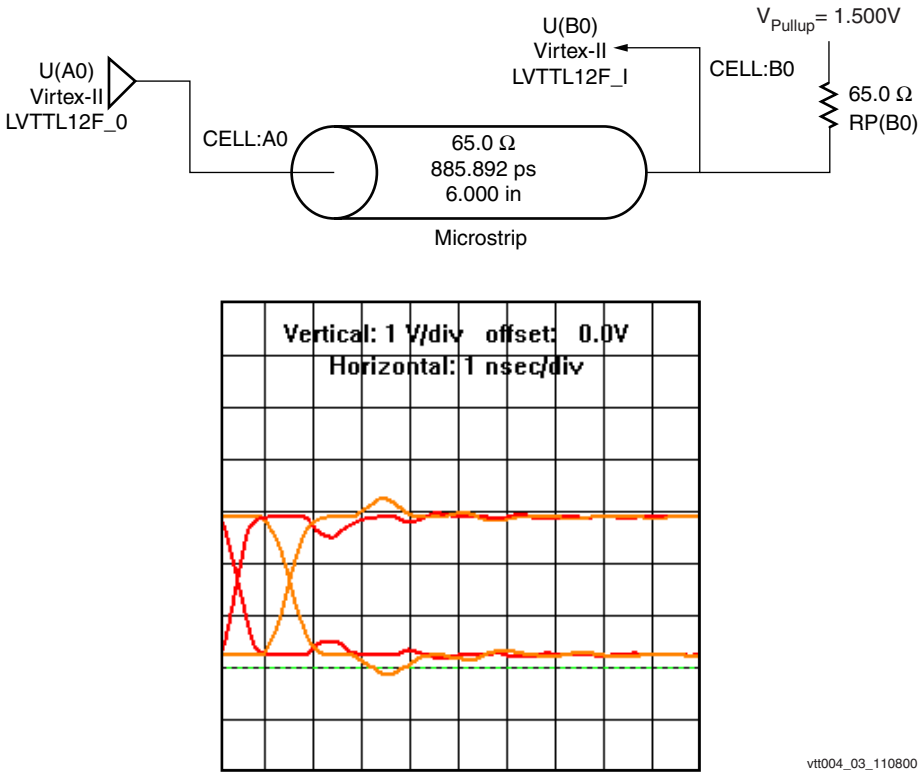


Figure 4-71: **Parallel Termination Example**

IBIS Simulators

Several different IBIS simulators are available today, and each simulator provides different results. An overshoot or undershoot of ±10% of the measured result is tolerable. Differences between the model and measurements occur, because not all parameters are modeled. Simulators for IBIS models are provided by the following vendors:

- Cadence
- Avanti Corporation
- Hyperlynx
- Mentor
- Microsim
- Intusoft
- Veribest
- Viewlogic

Xilinx IBIS Advantages

Xilinx provides preliminary IBIS files before working silicon has been verified (before tape out), as well as updated versions of IBIS files after the ICs are verified. Preliminary IBIS files are generated from SPICE models before working silicon has been verified. After the IC (device) is verified, appropriate changes are made to the existing IBIS files. These IBIS files are available at the following web site:

http://www.xilinx.com/support/sw_ibis.htm

IBIS Reference Web Site

http://www.eia.org/eig/ibis/ibis.htm

BSDL and Boundary Scan Models

Boundary scan is a technique that is used to improve the testability of ICs. With Virtex-II devices, registers are placed on I/Os that are connected together as a long shift register. Each register can be used to either save or force the state of the I/O. There are additional registers for accessing test modes.

The most common application for boundary scan is testing for continuity of the IC to the board. Some packages make visual inspection of solder joints impossible, e.g. BGA. The large number of I/Os available requires the use of such packages, and also increases the importance of testing. A large number of I/Os also means a long scan chain.

Test software is available to support testing with boundary scan. The software requires a description of the boundary scan implementation of the IC. The IEEE 1149.1 specification provides a language description for Boundary Scan Description Language (BSDL). Boundary scan test software accepts BSDL descriptions.

The IEEE 1149.1 spec also defines a 4 to 5 pin interface known as the JTAG interface. IEEE 1532 is a capability extension of IEEE 1149.1.

BSDL Files

Preliminary BSDL files are provided from the IC Design Process. Final BSDL files have been verified by an external third party test and verification vendor. The following are Virtex-II BDSL file names.

Virtex-II BSDL File Names	
XC2V40_CS144.BSD	XC2V2000_FF896.BSD
XC2V40_FG256.BSD	XC2V2000_BG575.BSD
XC2V80_CS144.BSD	XC2V2000_BG728.BSD
XC2V80_FG256.BSD	XC2V2000_BF957.BSD
XC2V250_CS144.BSD	XC2V3000_FG676.BSD
XC2V250_FG256.BSD	XC2V3000_FF1152.BSD
XC2V250_FG456.BSD	XC2V3000_BG728.BSD
XC2V500_FG256.BSD	XC2V3000_BF957.BSD
XC2V500_FG456.BSD	XC2V4000_FF1152.BSD
XC2V1000_FG256.BSD	XC2V4000_FF1517.BSD
XC2V1000_FG456.BSD	XC2V4000_BF957.BSD
XC2V1000_FF896.BSD	XC2V6000_FF1152.BSD
XC2V1000_BG575.BSD	XC2V6000_FF1517.BSD
XC2V1500_FG676.BSD	XC2V6000 _BF957.BSD
XC2V1500_FF896.BSD	XC2V8000_FF1152.BSD
XC2V1500_BG575.BSD	XC2V8000_FF1517.BSD
XC2V2000_FG676.BSD	XC2V8000_BF957.BSD