CoolRunner® XPLA3™ Development Kit

UG004 (v1.1) July 28, 2000

XILINX®

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The following table shows the revision history for this document.

Date	Version	Revision
03/10/00	1.0	Initial Xilinx release.
07/28/00	1.1	Updated to new format and text changes..

CoolRunner® XPLA3™ Development Kit 3

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Introduction

The CoolRunner XPLA3 Development Kit allows the designer to experiment with the Xilinx CoolRunner XPLA3 architecture using In-System Programming (ISP) to configure the device. Using the Xilinx Parallel Download Cable III and the PC-ISP3 Programmer software available from Xilinx WebPACK at http://www.xilinx.com/sxpresso/webpack.htm, the CoolRunner XPLA3 device can be programmed on the board directly from any PC. Any JEDEC file that targets the XCR3256XL can be downloaded to the board in this manner. The Xilinx Watch Tutorial can also be implemented on this XPLA3 Demo Board as described in the Tutorial section of this document.

This development kit consists of a Xilinx XPLA3 CoolRunner 256 macrocell device in a TQ144 package which can be programmed using the included Xilinx Parallel Download Cable III. Several power sources can be used with this board which include a +3.3V regulated input and two +10.0V maximum unregulated inputs. For low power demonstrations, this board can also be powered using grapefruits as shown in Figure 1. This is discussed later in this document in the Grapefruit Demonstration section. Two clock sources are available to the CoolRunner which can be either the 32.768 kHz low power on board clock or an external clock source (with an internal impedance of 50 ohms). A

prototyping area is also available so the designer can experiment with the CoolRunner XPLA3 architecture while interfacing to external components.

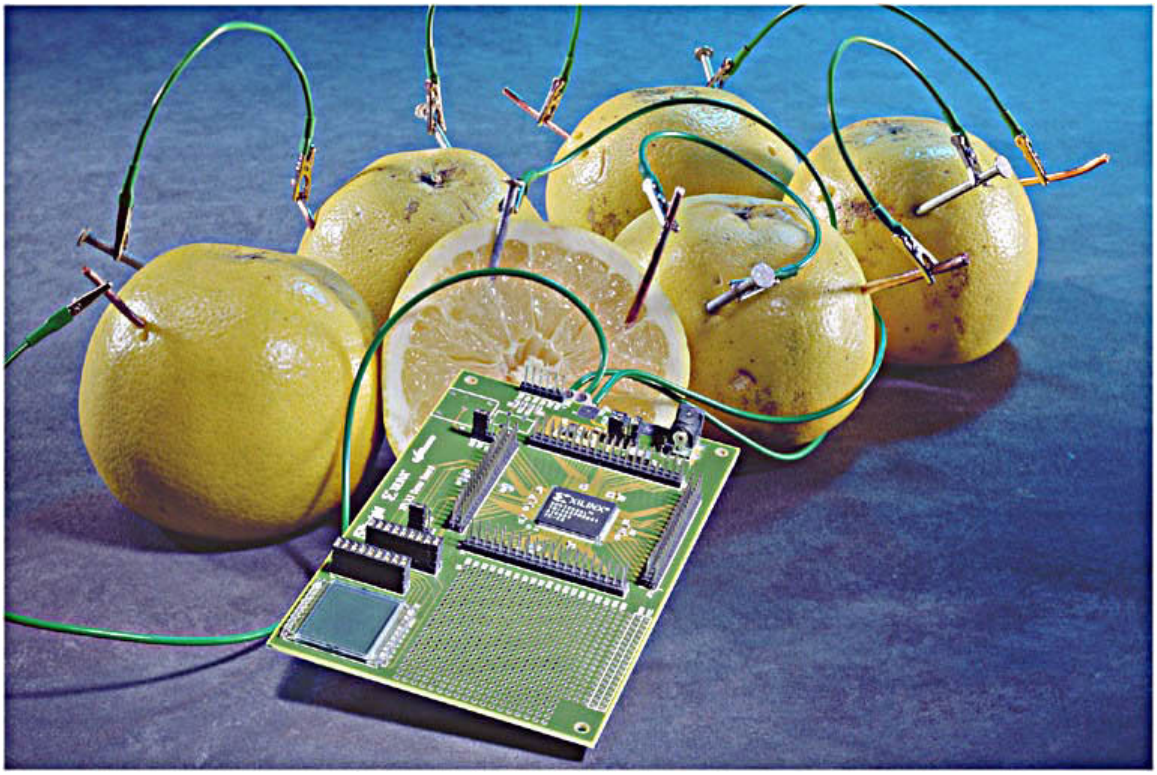

Figure 1: **CoolRunner XPLA3 Development Kit with Grapefruit Power Supply**

Getting Started

Important: Prior to powering the board the first time, please read the section entitled Power Connections.

A new CoolRunner XPLA3 Development Kit ships preprogrammed with a demonstration that uses the LCD. The demonstration simply scrolls the word "CoolrunnEr" from right to left in the LCD. In order to view the CoolRunner demonstration, apply power to the board. The demonstration will immediately begin to run.

To begin using the CoolRunner XPLA3 Development Kit follow the steps below.

1. Connect the power source to the board as specified in the section entitled Power Connections. The "CoolrunnEr" pattern should begin scrolling from right to left in the LCD.
2. Connect the Xilinx Parallel Download Cable III to the JTAG port JP6 located on the right hand side of the board. The "flying wires" from this cable should be connected to the board in a manner that the labels on the cables match the silk screen on the XPLA3 Demo Board for TCO, TCK, TMS, TDI, VDD and GND.
3. Using the Xilinx PC-ISP3 Programmer software, available for download from WebPACK at http://www.xilinx.com/sxpresso/webpack.htm, the board can be programmed with any custom JEDEC file.

Features

Power Connections

The CoolRunner XPLA3 Development Kit is designed to provide the user with maximum flexibility when connecting the power supply. A +3.3V voltage regulator is mounted to the board to allow for additional voltage flexibility. Along the right hand side of the board there are four connections. Three of these are power connections for applying power and are labeled "V", "+3.3V", and "J2". An additional connection labeled "GND" is a large pad and is used to connect ground to the board using an alligator clip type of connector. This type of pad will also allow the user to solder a wire to the board for a more permanent connection. The two power connections labeled "V" and "+3.3V" are also large pads and may be connected to the power source in the same manner. Finally, the power connection labeled "J2" is a jack to accept the external AC power adapter shipped with the CoolRunner XPLA3 Development Kit.

Located directly to the left of these power connections is JP7 which is used to manage these power connections. Figure 2 displays the arrangement of the jumpers and Table 1 describes the positioning of these jumpers to properly operate the board.

Jumper 7-8 on JP7 is used to conveniently connect or disconnect all power sources to the board. When the jumper is removed, power is disconnected from most components on the board. Power will still be present on JP7, the Voltage Regulator (U3), C1, and C2 which can be seen in the schematic as shown in Figure 6 at the end of this document. In addition, this jumper can be used for the grapefruit demo as discussed in the Grapefruit Demonstration section later in this document.

Before using the AC power adapter, configure JP7 as shown in the diagram labeled "AC Adapter" of Figure 2. If using a battery pack or grapefruit as a power source, configure JP7 as shown in the diagram labeled "+3.3V Pad Input" of Figure 2 prior to connecting the power source. If using any other external power source that needs to be regulated, configure JP7 as shown in the diagram labeled "+V Pad Input" of Figure 2 which will use the on board voltage regulator.

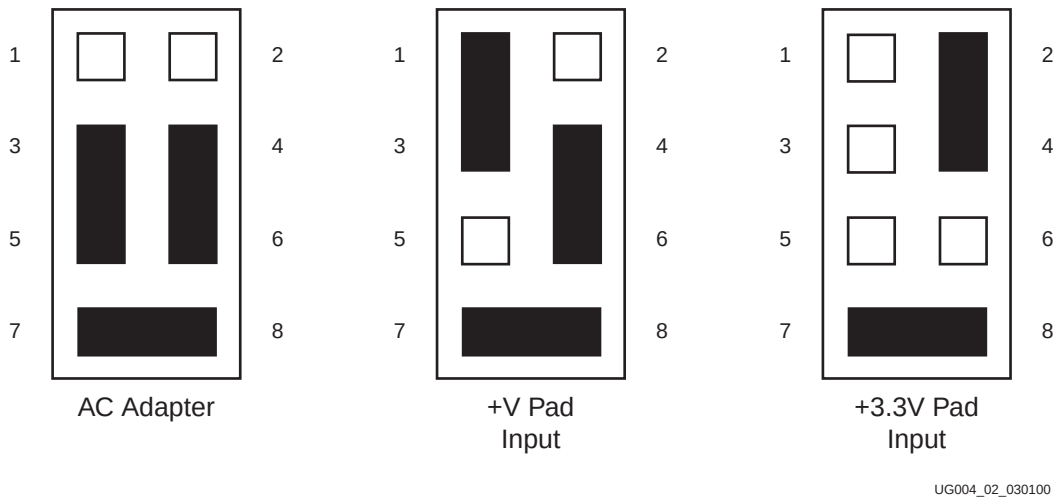

Figure 2: **JP7 Arrangement**

Table 1: **JP7 Configuration**

Pins (Closed)	Function	Description
2-4	Connects "+3.3V" pad to "VCC".	Used when an externally regulated power source set to +3.3V is connected to the "+3.3V" pad. This supply voltage must not to exceed the data sheet value for the XCR3256XL.
6-4	Connects the output of the on board regulator to "VCC".	When using an unregulated power source connected to the "V" pad or the "J2" connector, use this configuration to apply the output of the on board voltage regulator to "VCC".
1-3	Connects "V" pad to the input of the on board regulator.	When using an externally unregulated power source connected to the "V" pad, use this configuration to apply the voltage to the input of the on board +3.3V voltage regulator. This externally applied voltage must be set between the limits of +4.8V min. to +10.0V max.
5-3	Connects "J2" connector to the input of the on board regulator.	When using the external AC power adapter connected to the "J2" connector, use this configuration to apply the voltage to the input of the on board +3.3V voltage regulator. This externally applied voltage must be set between the limits of +4.8V min. to +10.0V max. The supplied AC power adapter typically delivers an unregulated +6.0V.
7-8	Connects "VCC" to the board's power plane.	Used to connect / disconnect all power sources to the board after JP7 and the on board regulator. During normal operation, this jumper must be closed. When using grapefruit as a power source, this jumper must be open for approximately 15 seconds with the grapefruit connected. Then close the jumper to initiate power up.

Clocking

Devices on the XPLA3 Demo Board can be clocked from either the on board 32.768 kHz low power clock or an external clock source. Selection between the two clock sources is

accomplished by the position of JP5. Figure 3 shows the positioning of JP5 to select either clock source.

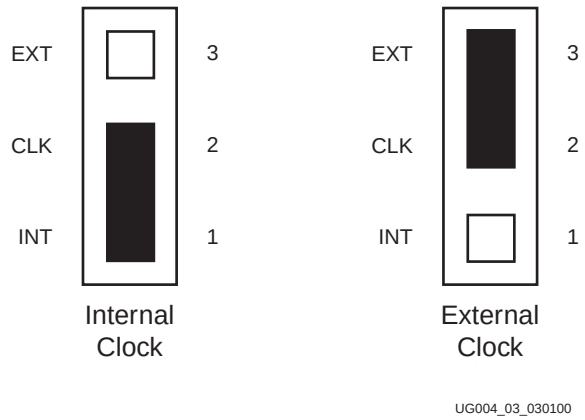

Figure 3: **JP5 Arrangement**

To use the external clock, a BNC PCB mount connector must be separately purchased and soldered to the space provided at J1 on the XPLA3 Demo Board. Use AMP part number 414460-1 or equivalent. Jumper J5 connects this clock to a 50 ohm trace. This clock network is connected to CLK0 on the XPLA3 CoolRunner CPLD.

Three additional clocks, CLK1, CLK2, and CLK3, are tied to the weak pull down resistors R5, R6, and R7 as shown in Figure 6. These are 51 ohm resistors intended to match a 50 ohm output impedance of the external clock source. These clocks may be accessed via JP1 pin 20, 19, 18, and 17 (CLK0, CLK1, CLK2, and CLK3 respectively) also shown in Figure 6.

JTAG Port

The JTAG port JP6 connects the ISP pins of the CoolRunner to the computer via the Xilinx Parallel Download Cable III. Using the Xilinx PC-ISP3 Programmer software, the XPLA3 CoolRunner can be accessed via this port for all ISP and JTAG operations. When using the cable, ensure that the labels on the "flying wires" match the silk screen on the XPLA3 Demo Board to ensure proper operation.

All ISP pins are directly connected to the JTAG port JP6 but are also available on selected headers as shown in Table 2.

Table 2: **JTAG Signal Access**

JTAG Pin	Header	Header Pin
TMS	JP2	20
TCK	JP4	17
TDI	JP2	4
TDO	JP4	32

In the event that the ISP pins were not reserved in the design, the JTAG port will no longer be accessible and will therefore prevent the user from subsequent device programming. To gain access to the ISP pins once again, it will be necessary to temporarily pull the PORT_EN signal high before programming. This will allow the user to program the device with the JTAG port. This signal is accessible via JP2 PIN 13. Once the CoolRunner has been programmed in this manner, the PORT_EN pin must be returned to the low state for normal operation.

LCD

The on-board LCD has 16 segments arranged as shown in Figure 4. In the default configuration, the segments of the LCD are connected to the I/Os via jumpers LCD1 and LCD2 as described in Table 3. By removing the jumpers, the I/Os will be disconnected from the LCD segments.

The LCD ground pin is connected to an I/O pin. Since the characteristic of LCDs is such that a charge builds up in the segment over time while held at DC levels, this board has been designed with the ability to drive the LCD reference pin with an oscillating signal at approximately a 50% duty cycle. A segment is darkened when driven by an inverted signal with respect to the LCD reference pin; a segment is transparent when driven by a signal in phase with the LCD reference pin signal. This technique is implemented in the "CoolrunnEr" demonstration pattern.

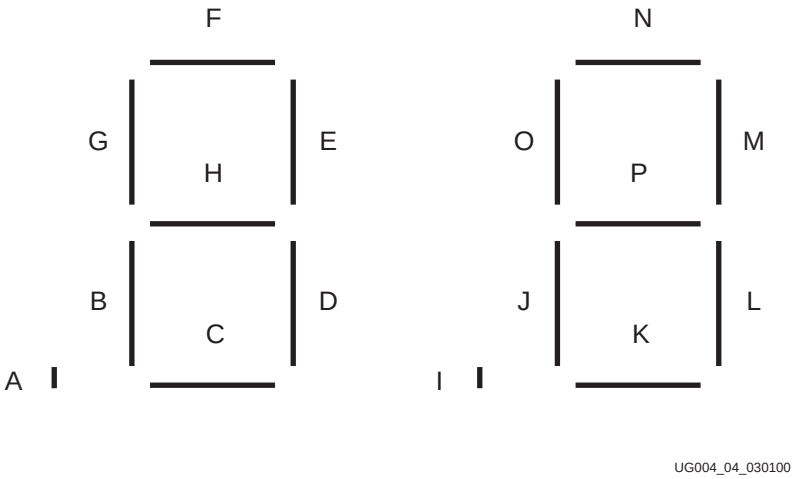

Figure 4: **Segment Assignments for the LCD**

Table 3: **LCD Jumper Arrangement**

LCD Segment	I/O Number	Pin Number	Jumper	Pins (Closed)
A	IO58	74	LCD2	1-2
B	IO59	75	LCD2	3-4
C	IO60	77	LCD2	5-6
D	IO61	78	LCD2	7-8
E	IO62	79	LCD2	9-10
F	IO63	80	LCD2	11-12
G	IO64	81	LCD2	13-14
H	IO65	82	LCD2	15-16
I	IO67	84	LCD1	1-2
J	IO68	86	LCD1	3-4
K	IO69	87	LCD1	5-6
L	IO70	88	LCD1	7-8
M	IO71	90	LCD1	9-10
N	IO72	91	LCD1	11-12

Table 3: **LCD Jumper Arrangement *(Continued)***

LCD Segment	I/O Number	Pin Number	Jumper	Pins (Closed)
O	IO73	92	LCD1	13-14
P	IO74	93	LCD1	15-16
GND	IO66	83	LCD2	17-18

User Prototyping Area

Immediately below the LCD is a User Prototyping Area which is an array of holes and pads set up on 0.1" centers accepting common DIP packages. Most pads are not connected to anything within the board. The exceptions to this are bottom two rows and the right hand most column of pads. The bottom most row is connected to V_{CC} and the row directly above that is connected to ground as labeled on the silk screen. Along the right hand side of the User Prototyping Area, the pads are connected to I/Os 87 through 106 which correspond to pins 109 through 138 on the CoolRunner as shown in Figure 6 and described in detail in Table 4. This table also specifies which Function Block and Macrocell number correspond to these I/Os. The User Access Headers, described in the section below, include further access to the I/Os in the prototyping area via JP1 and is also specified in Table 4.

Table 4: **Prototyping Area I/O Cross Reference**

Prototyping Area I/O	XPLA3 Pin Number	Function Block	Macrocell	JP1 Pin Number
IO87	109	B	4	1
IO88	110	B	11	2
IO89	111	B	12	3
IO90	112	B	14	4
IO91	113	B	15	5
IO92	114	D	0	6
IO93	116	D	1	8
IO94	117	D	2	9
IO95	118	D	4	10
IO96	119	D	11	11
IO97	120	D	12	12
IO98	121	D	13	13
IO99	122	D	15	14
IO100	131	K	15	23
IO101	132	K	14	24
IO102	133	K	13	25
IO103	134	K	12	26

Table 4: **Prototyping Area I/O Cross Reference *(Continued)***

Prototyping Area I/O	XPLA3 Pin Number	Function Block	Macrocell	JP1 Pin Number
IO104	136	K	11	28
IO105	137	K	4	29
IO106	138	K	2	30

User Access Headers

Surrounding the CoolRunner CPLD are User Access Headers which connect to every pin on the CPLD. These headers consist of the pins within JP1, JP2, JP3, and JP4 which are connected to the CoolRunner as shown in Figure 6. Although a select few I/Os are available in the User Prototyping Area as described in Table 4, the User Access Headers allow the designer to connect a prototype circuit to any I/O, clock, JTAG, or power pin on the CoolRunner CPLD.

Grapefruit Demonstration

Demonstrating the low power capabilities of the CoolRunner is impressive when using four grapefruits as a power supply. In addition to the four grapefruits, the demonstration requires wire, alligator clips, and two dissimilar metals for electrodes. It is recommended to use copper and zinc. This is easily implemented with heavy gauge (#10 or #12) copper wire or very small copper pipe along with zinc coated nails.

Prior to starting the grapefruit demonstration, please read the Getting Starting section. Using Figure 1 as a reference, insert one copper wire and one zinc coated nail into each grapefruit. Next, the grapefruits need to be wired in series. This is accomplished by using one wire with an alligator clip at each end and attaching this wire to the copper post of one grapefruit and the zinc post of a second grapefruit. Attach a wire to the copper post of second grapefruit to the zinc post of a third grapefruit. Connect the copper post of the third grapefruit with the zinc post of a fourth grapefruit with another wire. What remains is the first grapefruit with an unconnected zinc post and the fourth grapefruit with an unconnected copper post. At this point, all other posts should be connected with one wire. Take another wire and connect it to the remaining zinc post of the first grapefruit and another wire to the remaining copper post of the fourth grapefruit. Do not connect these two together. They will be connected to the XPLA3 Demo Board momentarily. Ensure that like metals are not connected together since this will not permit current to flow.

Ensure that JP7 is arranged like the "+3.3V Pad Input" drawing in Figure 2. Remove the jumper 7-8 of JP7 prior to connecting the grapefruits. Four grapefruits typically generate about 3.5V using copper and zinc electrodes. Connect the positive end (copper) of the grapefruit array to the +3.3V pad and the negative end (zinc) to the GND pad of the XPLA3 Demo Board. Wait about 10-15 seconds and connect jumper 7-8 of JP7 to start the CoolRunner. If the start was successful, "CoolrunnEr" will start to scroll in the LCD. If the start was unsuccessful, disconnect jumper 7-8 of JP7 and wait a longer period of time prior to reconnecting the jumper.

Tutorial

Available from the Xilinx Application Note web site at http://www.xilinx.com/apps/epld.htm#tutorials is the Watch Tutorial. This design tutorial implements a runner's stop watch viewed on the LCD and controlled by two inputs. The documentation included with the tutorial describes the implementation of the design into the XPLA3 Demo Board.

Two controls required by the tutorial are the STRTSTOP and the RESET signals. To access the STRTSTOP control, the user can position the jumper on JP8 to either the V_{CC} or GND position depending on the logic level required for the design.

RESET is accessible on JP3 by positioning a jumper between jumpers 22-24 for a high logic level and between jumpers 23-24 for a low logic level. Figure 5 shows JP3 in the two configuration modes for the RESET signal.

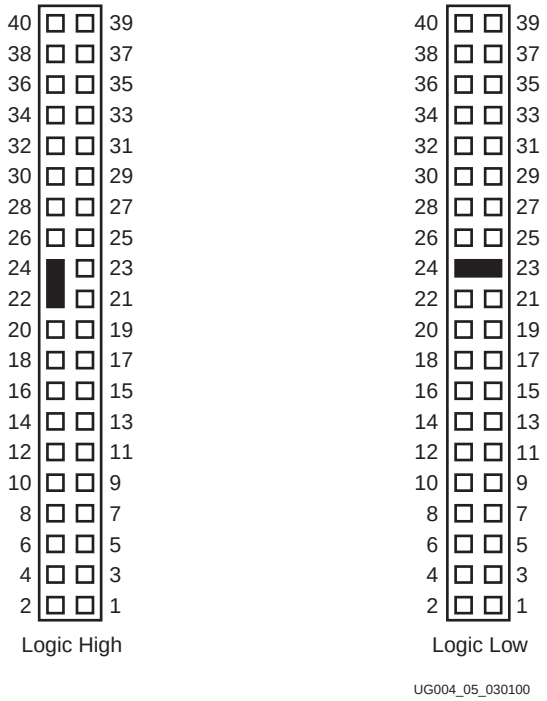

Figure 5: **JP3 Configuration Settings for the Tutorial RESET Function**

Conclusion

This board has been designed to demonstrate the CoolRunner's low power capabilities. Xilinx CoolRunner CPLDs are the perfect solution for low power applications. This CoolRunner XPLA3 Development Kit is an excellent tool to assist the designer with CoolRunner training, prototyping, and power demonstrations.

Table 5: **Xilinx Web Site Links**

Web Link	URL
WebPACK	http://www.xilinx.com/sxpresso/webpack.htm
Watch Tutorial	http://www.xilinx.com/apps/epld.htm#tutorials
Application Notes	http://www.xilinx.com/apps/appsweb.htm

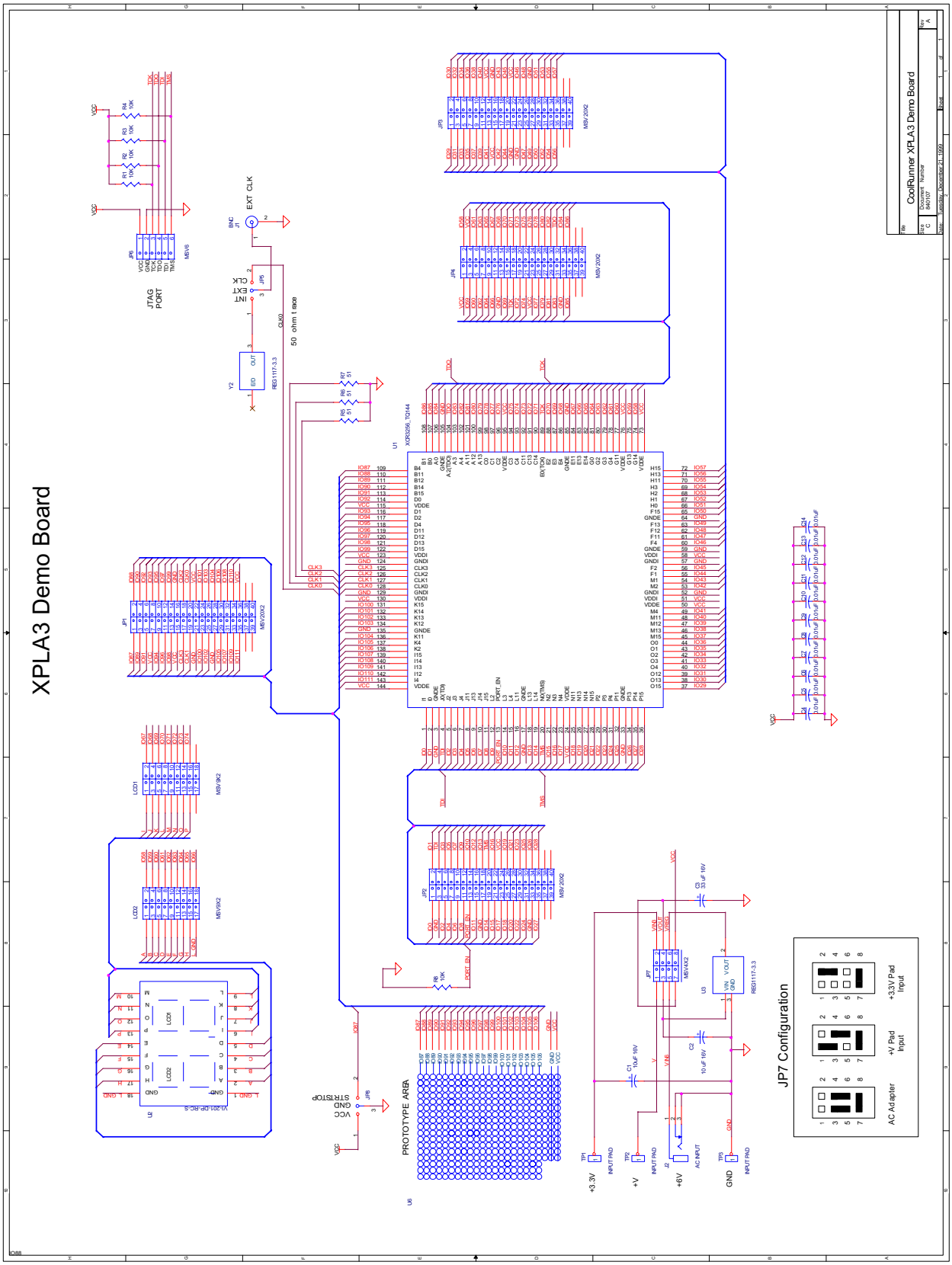

Figure 6: **CoolRunner XPLA3 Development Kit Schematic**