Dual Port Block Memory for Virtex™-II V2.0

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Features

- Fully synchronous, drop-in modules for the Virtex™-II family; uses Virtex™-II block memory for performance and efficiency.
- Supports all three Virtex™-II write mode options: read after write, read before write, and no read on write.
- Supports data widths from 1 to 256 bits and memory depths from 512 to 1M words.
- Supports RAM functions enabling simultaneous write operations to separate locations and simultaneous read operations from the same location.
- The ports are completely independent of each other
- Available in the XIlinx CORE Generator™ System V3.1i

Functional Description

The Dual Port Block Memory module is composed of single or multiple Virtex-II 18Kb blocks enabling a deeper and/or wider memory implementations. The SelectRAM+ memory is True Dual-Port™ RAM, offering fast, discrete, and large blocks of memory in the Virtex-II device.

A Memory module has two independent ports that enable shared access to a single memory space and is generated based on user-defined width and depth. Both ports are functionally identical, with each port providing read and write access to the memory. Simultaneous reads from the same memory location may occur, but all other simultaneously reading-from and writing-to the same memory location will result in correct data being written into the memory, but invalid data being read.

The Memory's Port A and Port B are configured to support user defined data input and address widths. When both ports are disabled (ENA and ENB inactive) the memory contents and output ports remain unaltered. When either port is enabled (ENA or ENB asserted) all memory operations occur on the rising edge of the clock input.

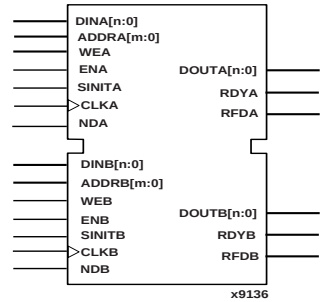

Figure 1: Core Schematic Symbol

During a write operation (WEA or WEB asserted), the data presented at the port's data input is stored in memory at the location selected by the port's address input. There are three "write mode" options supported by the Virtex™-II architecture. Each of these options determines the behavior of the corresponding data output port when a write operation occurs.

During a read operation the memory contents at the location selected by the address will appear at the module's output. When Synchronous Initialization (SINITA or SINITB) is active the module's registered outputs are synchronously reset to a user defined value; Synchronous Initialization command has no effect on the contents of the memory, and write operations may still take place. For additional information on the Virtex-II BlockRAM, refer to the *Virtex-II Handbook*.

Pinout

Port names for the core module are shown in Figure 1 and defined in Table 1. The inclusion of some ports on the module is optional; exclusion of these ports will alter the function of the module. The optional ports are marked in Table 1 and described in more detail below.

Clock Enable - CLK[AIB]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the rising edge of their corresponding CLK pin. The data bus has a clock-to-out time referenced to the CLK pin. If a falling edge

Table 1: Core Signal Pinout

SIgnal	Direction	Description
DIN[A|B]<n:0> (Optional)	Input	**Data Input**: data to be written into memory via Port [A|B].
ADDR[A|B]<m:0>	Input	**Address**: the memory location to which data will be written or read via Port [A|B].
WE[A|B] (Optional)	Input	**Write Enable**: control signal used to allow transfer of input data into memory via Port [A|B] (Active High)
EN[A|B] (Optional)	Input	**Enable**: control signal used to enable Memory accesses via read and write operations from Port [A|B]. (Active High)
SINIT[A|B] (Optional)	Input	**Synchronous Initialization**: control signal used to force the module's outputs to a predefined state. (Active High)
CLK[A|B]	Input	**Clock**: clock input, all memory access is synchronous with the clock input.
ND[A|B] (Optional)	Input	**New Data Port A**: indicates that there is a new and valid address on Port ADDR[A|B]. (Active High)
DOUT[A|B]<n:0>(Optional)	Output	**Data Output**: synchronous output of memory.
RFD[A|B] (Optional)	Output	**Ready for Data**: indicates that the memory is ready to accept new data. (Active High)
RDY[A|B] (Optional)	Output	**Ready**: indicates valid data on port DOUT [A|B]. (Active High)

operation is required, the user should invert the clock signal attached to the core's clock ports.

Enable - EN[AIB]

The enable pin affects the read, write, and SINIT functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory locations.

Write Enable - WE[AIB]

Activating the write enable pin allows the port to write to the memory locations. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (write first, read first, no change). When inactive, a read operation occurs, and the contents of the memory locations referenced by the address bus reflect on the DOUT bus, regardless of the write mode selected.

Synchronous Initialization - SINIT[AIB]

The SINIT pin forces the data output ports to the user defined SINIT value. The data output ports are each synchronously asserted to their respective SINIT value. This operation does not affect memory locations and does not disturb write operations on the other port. If the core is configured with an enable pin, then SINIT function is active only when the enable port is active.

Address Bus - ADDR[AIB]<m:0>

The address bus selects the memory location which will be accessed during a read or write operation.

Data-In Bus - DIN[AIB]<n:0>

The DIN busses provide the new data value to be written into the memory. Data input and output signals are always busses; that is, in a 1-bit width configuration, the data input signal is DIN[0] and the data output signal is DOUT[0].

Data-Out Bus - DOUT[AIB]<n:0>

The DOUT busses reflect the contents of memory locations referenced by the address bus during a read operation. During a write operation (write first or read first configuration), the DOUT busses reflect either the DIN busses or the stored value before write. During a write operation in no change mode, DOUT busses are not affected.

New Data - ND[AIB]

ND indicates that there is a new and valid address on ADDR[A|B] port. It only affects the RDY port.

Ready for Data - RFD[AIB]

RFD indicates that the memory is ready to accept new data. RFD[A|B] is always true except when EN[A|B] is inactive.

Output Ready (valid) - RDY[AIB]

Indicates valid output on port DOUT[A|B] relative to when ND is asserted. RDY[A|B] will lag ND[A|B] by the latency of the block memory.

CORE Generator Parameters

The CORE Generator parameterization windows for this module are shown in Figure 2 and Figure 3. These windows are interactive to allow user defined customization of the Block Memory. In Figure 2, the configuration for Port A and Port B can be customized. There is also an information window shown at the bottom, which verifies that, the total

number of blocks required does not exceed those available on the targeted device. In Figure 3, several other design options are available including optional pins and pipelining.

Definition of GUI Interface Fields

- **Component Name**: Enter a name for the output files generated for this module (up to 256 characters).
- **Memory Size - Port A**:
  - **Width A**: Select the data bit width. The width can be between 1 and 256.
    - **Depth A**: Select the number of words in memory. The value range is 512 to 1048576 (1M). Entries not divisible by 512 will be rounded upto the next highest multiple of 512; available depths will vary depending on the width entered for Port A; the absolute maximum number of words is 1M. Cores should not exceed the number of Block RAM primitives in the targeted device.
- **Memory Size - Port B**:
  - **Width B**: Reports width of Port B which (for this release) will be the same as the width of Port A.
  - **Depth B**: Reports the depth of Port B which (for this release) will be the same as the depth of Port A.
- **Port A Options**:
  - **Configuration**:
    - **Read and Write**: Configures Port A to have DINA and DOUTA ports allowing read and write access to the memory.
    - **Write Only**: Configures Port A to have a DINA port only enabling this port to only be used for write access. Note that only one port can be configured to be Write Only.
    - **Read Only** Configures Port A to have a DOUTA port only enabling this port to only be used for read access. Note that only one port can be configured to be Read Only.
  - **Write Mode**: Select one, the default is “read after write.”
    - **Read after Write**: On the same clock edge that writes the input data into memory, the input data is transferred onto the DOUT port.
    - **Read before Write**: On the same clock edge that writes the input data into memory, the current data in the addressed memory location is transferred onto the DOUT port.
    - **No Read on Write:** A write operation has no effect on the content of the DOUT port. The DOUT port is not updated when WE is active.
- **Port B Options**:
  - **Configuration**:
    - **Read and Write**: Configures Port B to have DINB and DOUTB ports allowing read and write access to the memory.
    - **Write Only**: Configures Port B to have a DINB port only enabling this port to only be used for write access. Note that only one port can be configured to be Write Only.
    - **Read Only**: Configures Port B to have a DOUTB port only enabling this port to only be used for read access. Note that only one port can be configured to be Read Only.
  - **Write Mode**: Select one, the default is “read after write.”
    - **Read after Write**: On the same clock edge that writes the input data into memory, the input data is transferred onto the DOUT port.
    - **Read before Write**: On the same clock edge that writes the input data into memory, the current data in the addressed memory location is transferred onto the DOUT port.
    - **No Read on Write**: A write operation has no effect on the content of the DOUT port. The DOUT port is not updated when WE is active.
- **Design Options**: Select to open another window with additional configuration options.
- **Information Panel**: Lists the resulting configuration of the core.
  - **Address Width A**: Displays the number of address bits required for Port A for this configuration.
  - **Address Width B**: Displays the number of address bits required for Port B for this configuration.
  - **Blocks Used**: Displays the number of BlockRAM primitives needed to implement this configuration. It is recommended to verify that the required number of blocks does not exceed those available in the target Virtex-II part.
  - **Port A Read Pipeline Latency**: Displays the total latency from a new address presented to the memory to a valid output. Registering the inputs and adding an additional output register will each increase the total latency by one.
  - **Port B Read Pipeline Latency**: Displays the total latency from a new address presented to the memory to a valid output. Registering the inputs and adding an additional output register will each increase the total latency by one.
- **Generate**: Select to generate the block memory module. Make sure that the parameters are correctly selected for the particular application before executing this option.
- **Cancel:** Select to close window and return to the Core Generator.
- **Datasheet:** Select to open a PDF version of this document.

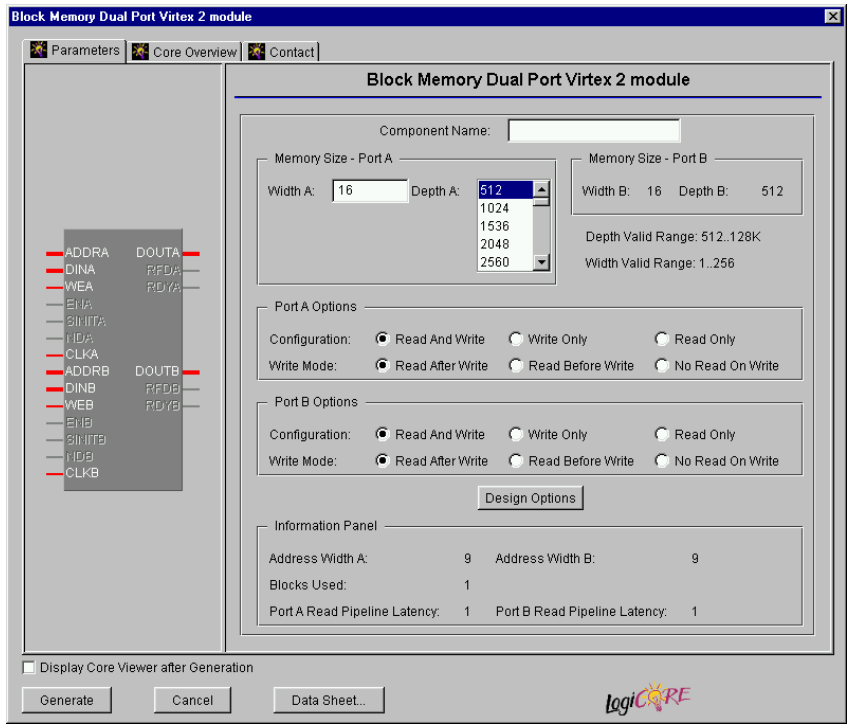

Figure 2: Block Memory Dual Port Main Parameterization Window

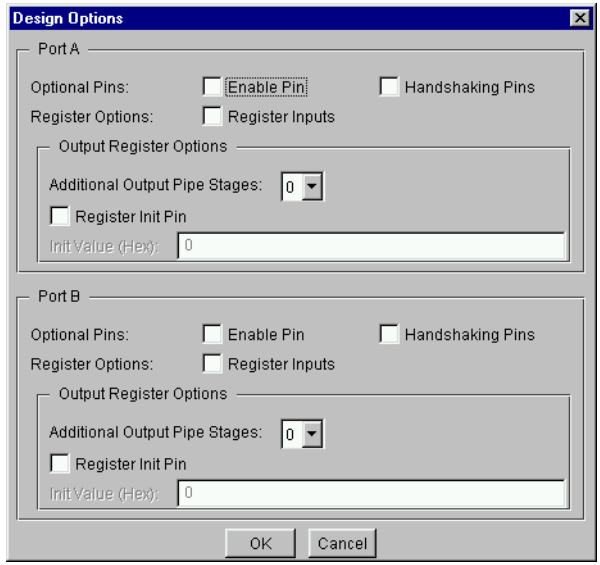

Figure 3: Block Memory Dual Port Design Options Window

Design Options

Port A or Port B

- **Optional Pins**:
  - **Enable Pin**: Check the box to include the enable EN[A\B] port on the module; uncheck the box to remove it.
  - **Handshaking Pin**: Check the box to include the following ports; uncheck the box to remove them.
    - **ND** [New Data]: Signals a new and valid memory address whenever active.
    - **RFD** [Ready For Data]: Indicates that the memory can accept new addresses.
    - **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid.
- **Register Options**:
  - **Register Inputs**: Check this box to register ports DIN, ADDR, and WE prior to accessing block memory. See Figure 4.
- **Output Register Options:**
  - **Additional Output Pipe Stages**: Select "1" to enable an additional register on the output of the memory; select "0" to disable an additional register on the output of the memory. See Figure 4.
  - **Register Init pin (SINIT)**: Check box to add the synchronous port SINIT to the memory.
  - **Init value** (HEX value): Enter the HEX value that the output port will get set to when the SINIT port is true.
- **Close**: Select to close window and return to the main parameterization window.

Operating Modes

To maximize utilization of the True Dual-Port memory at each clock edge, the block SelectRAM-II memory supports three different write modes. Each port's write mode is independently configurable. The "read before write" mode offers the flexibility of using the data output bus during a write operation on the same port. Output port behavior is determined by the configuration. This choice increases the effective bandwidth of the Block Memory.

Read Operations

Read operations are synchronous to the rising edge of the clock. The data in the memory location selected by the address apears on the DOUT port after the rising edge of the clock.

Write Operations

Write operations are synchronous to the rising edge of the clock. The data on the DIN port is written into the memory location selected by the address on the rising edge of the clock when WE is active. The user can configure the memory in one of three ways to determine the behavior of the DOUT port during a write cycle. Each port's write mode is independently configurable. Note that the timing diagram and description of the write modes below assume that the memory has been configured without input registering and additional output registers.

Write First or Read-After-Write Mode

In write first mode, data input is loaded simultaneously with a write operation on the DOUT port. As shown in Figure 5, the data input is stored in memory and mirrored on the output.

Read First or Read-Before-Write

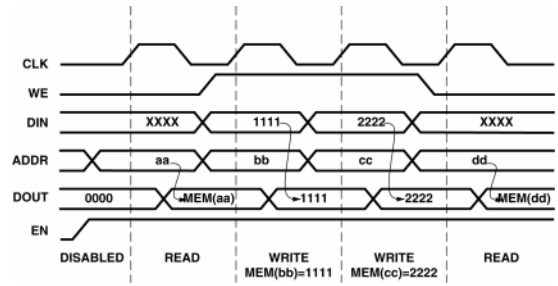

Figure 5: Write First Mode Waveform

Mode

In read first mode, data previously stored at the write address appears on the DOUT port. Data input is stored in memory and the prior contents of that location is driven on the output, during the same clock cycle (shown in Figure 6).

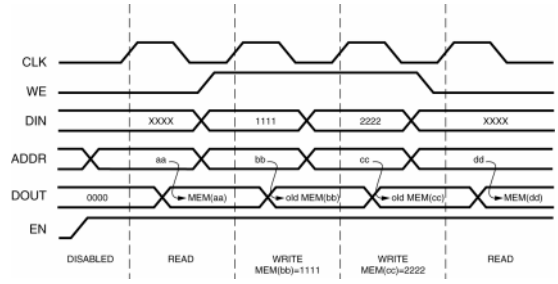

Figure 6: Read First Mode Waveform

No Read-on-Write Mode

In no "Read-on-Write" mode, the DOUT port remains unchanged during a write operation. As shown in Figure 7, data output is still the last read data and is unaffected by a write operation on the same port. Mode configuration is static. One of these three modes is set individually for each port by an attribute. The default mode is write first.

Conflict Resolution

Virtex-II block memory is True Dual-Port RAM that allows both ports to simultaneously access the same memory location. When one port writes to a given memory location,

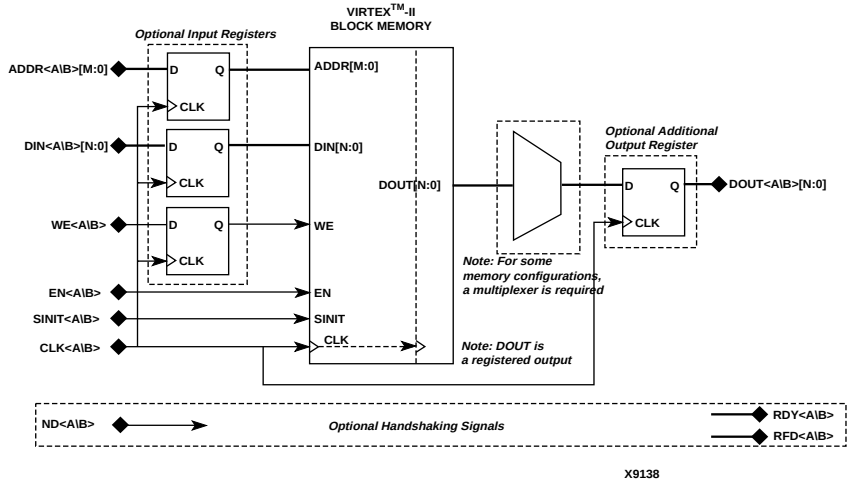

Figure 4: Dual Port Memory Block Diagram

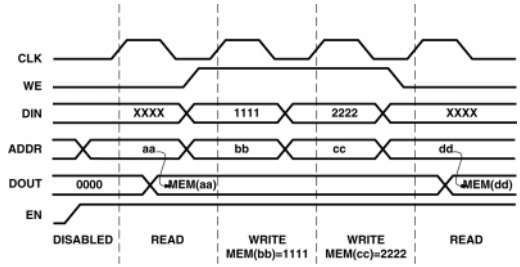

Figure 7: No Read-on-Write Mode Waveform

the other port must not address that memory locationl (for a write/read) within the clock-to-clock setup window. Conflicts do not cause any physical damage to BlockRAM cells. For more information on conflict resolution, refer to the *Virtex™-II Handbook*.

Core Resource Utilization

The number of Block RAM primitives required is dependent on the values of the depth and data width fields selected in the CORE generator parameterization window, and is at least: (depth* width)/18432 and will exceed this number for many configurations.

For some memory depths extra logic is required to decode the address and multiplex the outputs from various primitives. Virtex-II CLB slices are used to provide this functionality. The number of slices required depends on the way that the depth is constructed from the primitives, the data width, and the implementation of any decoding or multiplexing.

Table 2: Parameter File Information

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width	Integer	Ranges from 1 to 256
Depth	Integer	Ranges from 512 to 1Meg with increments of 512
Write Modes	String	Default: Read after Write Options are: Read after Write; Read before Write; and No Read on Write
Enable ENA, ENB	Boolean	Default=false
Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Register Inputs	Boolean	Default=false
Additional Output Pipe Stages	Integer	Default=0 0=No additional output registers
Synchronous Initialization	Boolean	Default=false
Synchronous Initialization Value	Integer (Hex)	Default=0

Ordering Information

This core may be downloaded free of cost from the Xilinx IP Center (http://www.xilinx.com/ipcenter) for use with the Xilinx CORE Generator™ System V3.1i and later. The CORE Generator System tool is bundled with all Xilinx Alliance and Foundation Series Software packages.

To order online, visit the Xilinx Silicon Expresso Cafe at http://toolbox.xilinx.com/cgi-bin/xilinx.storefront/241669816/catalog//1006).

Xilinx software may also be ordered through your local Xilinx sales office. Information on the sales office nearest you is available at http://www.xilinx.com/company/sales.htm.