Sine/Cosine Look-Up Table V2.1

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Features

- Drop-in module for Spartan™-II, Virtex™, and Virtex™–E FPGAs
- User selectable option for table value storage in either Distributed or Block Memory
- Supports THETA input widths of 3 to10 bits for Distributed ROM and 3 to 16 bits for Block ROM
- Supports output Sine/Cosine widths of 4 to 32 bits
- Supports negative Sine/Cosine outputs
- Automatically selects between quarter wave storage and full 360-degree wave storage for the most efficient implementation
- High performance and density guaranteed through Relationally Placed Macros (RPM) mapping and placement technology. (Distributed ROM implementation only)
- Variable pipelining option to improve overall clock rates
- Works with 3.1i or later versions of the Xilinx Core Generator

Functional Description

The Sine/Cosine module accepts an input THETA value and produces outputs of SINE (THETA) and/or COSINE (THETA). The user controls the input THETA width and output SINE and /or COSINE width values.

The values for the sine and cosine wave are stored in an internal ROM. Depending on what the user specifies for the THETA input width and SINE and/or COSINE output width, either a full wave or quarter wave is stored in the ROM table. When only a quarter wave is stored, the full 360-degree output is generated using additional internal logic. The selection of quarter or full wave storage is performed automatically to produce the most efficient implementation.

Latency

The performance of the module can be controlled by the user by specifying an appropriate combination of input and output registering and pipelining. In general the higher the number of pipeline stages, the higher the clock performance. For Distributed Memory implementations, the output can be anywhere from fully combinatorial to fully pipelined with up to five clock cycles of latency. Block ROM implementations have a minimum of one clock cycle of latency and a maximum of four. For both distributed and block memory implementations, the actual maximum latency is dependent on the depth of the internal ROM table. Tables 1 and 2 list the supported ranges.

Table 1: Distributed Memory-based Latency

Input width (bits)	Latency Ranges (clocks)
3 to 6	0 to 2
7 to 8	0 to 4
9 to 10	0 to 5

Table 2: Block Memory-based Latency

Input Width (bits)	Output Width (bits)	Latency Ranges (clocks)
Less than 9	Less than 17	1 to 3
Less than 10	Less than 9	1 to 3
Less than 11	Less than 5	1 to 3
All other cases		1 to 4

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 3.

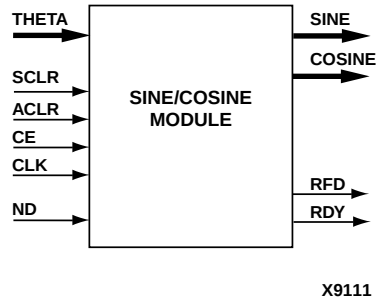

Figure 1: Sine/Cosine Module Schematic Symbol

Table 3: Core Signal Pinout

Signal	Signal Direction	Optional/ Required	Active Level	Description
THETA	Input	Required	N/A	Input value for which the sine and/or cosine is generated
SCLR	Input	Optional[1]	HIGH	Synchronous Clear input. All module registers are cleared to logic Low level when this signal is active (High) and a clock edge is detected.
ACLR	Input	Optional[1]	HIGH	Asynchronous Clear input. All module registers are cleared to logic Low level
CE	Input	Optional[2]	HIGH	Clock enable signal, active High
CLK	Input	Optional[2]	Rising edge	Clock input value, rising edge active
ND	Input	Optional[4]	HIGH	New Data input signal. Indicates to the module that a new THETA value is being input on the THETA input port. Assertion of ND initiates the generation of the Sine and/or the Cosine output value
SINE	Output	Optional[3]	N/A	Sine value output for the THETA input value
COSINE	Output	Optional[3]	N/A	Cosine value output for the THETA input value
RFD	Output	Optional[4]	HIGH	Ready For Data output signal indicates that the module can accept new THETA input values.
RDY	Output	Optional[4]	HIGH	Ready output signal indicates that a valid Sine and/or Cosine value is available on the output ports.

Notes:

1. Clear options are available only when the output is registered.
2. A CLK signal is required when Block ROM implementation is specified, and when input or output registering is requested.
3. Either the Sine, Cosine, or both outputs must be specified.
4. ND, RFD, and RDY are handshaking signals which are activated as a group when the **Handshaking Options** setting is enabled.

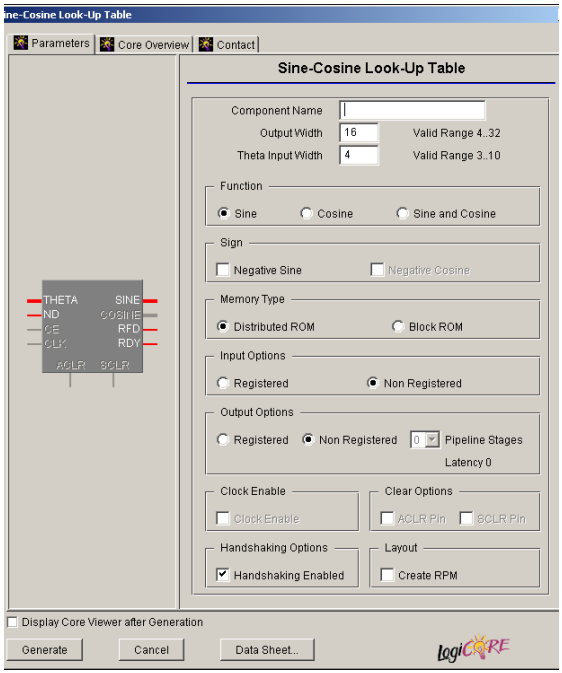

Figure 2: Sine Cosine Look-up Table GUI

CORE Generator Parameters

- **Component Name**: User defined name for component
- **Output Width**: Specify an output width for both the Sine and Cosine output values. The valid range is 4 to 32.
- **Theta Input Width**: Specify an output width for the input THETA value from which the Sine/Cosine is taken. The valid range is 3 to 10.
- **Function:** There are three output options: Sine Output Only, Cosine Output Only, and simultaneous Sine and Cosine Outputs
- **Sign**: The Sine and Cosine outputs have the option of being made negative independently.
- **Memory Type**: Wave values may be stored in either Distributed or Block ROM by selecting the appropriate radio button
- **Input Options**: The THETA input signal may be registered or non-registered. Registering the THETA input register increases the latency by one clock cycle. The amount of logic added is equal to one flip-flop per input bit of THETA.
- **Output Options**: The SINE and COSINE outputs can also be registered. When the outputs are registered, an additional pipelining option becomes available to improve the module's performance. Adding pipeline stages adds a minimal amount of logic in most cases. Tables 4 and 5 show resource utilization cases for various size modules.
- **Handshaking Options:** The Sine/Cosine module supports a system-level interface consisting of the signals ND, RFD, and RDY. The interface provides status information regarding the state of the module. The signals are used to start the processing of a THETA value and to indicate when the module can accept a new THETA value, or to indicate when the outputs have valid results.
  - ND is used to start the processing of a New Data value on the THETA port.
  - RFD indicates that the module is Ready For Data on the input THETA port.
  - RDY indicates that the output SINE and COSINE output ports have valid values.

The handshaking logic is optional.

- **Clear Options**: Whenever an output register is requested for the module, two additional user-selectable clear pins become available for resetting the module's internal flip-flops to a known, all-zeros state—ACLR and SCLR.
  Asserting ACLR High results in an immediate asynchronous clearing of the internal flip-flops to zero, regardless of the state of the clock.
  SCLR initiates a synchronous clearing of the internal flip-flops to zero, when this signal is asserted High and a rising clock edge is detected.

Table 4: Core Resource Utilization (slice count) for Various Table Sizes (Distributed ROM Implementation)

Theta Width	Output Width	Single Output	Sine and Cosine
6*	8	17	33
	12	25	49
	16	33	65
	32	65	129
8	8	29	57
	12	40	79
	16	50	99
	32	90	179
10	8	80	159
	12	118	235
	16	157	313
	32	309	617

* Fullwave gets stored.

Table 5: Core Resource Utilization (slice count) for Various Table Sizes (Block ROM Implementation)

Theta Width	Output Width	Single Output		Sine and Cosine	
		No. of Slices	No. of Block ROMs	No. of Slices	No. of Block ROMs
6	8*	1	1	2	1
	12*	1	1	2	1
	16*	1	1	2	1
	32	24	1	47	2
8	8*	1	1	2	1
	12*	1	1	2	1
	16*	1	1	2	1
	32	26	1	52	2
10	8	17	1	33	1
	12	19	1	37	1
	16	21	1	41	1
	32	29	2	57	2
13	8	22	4	41	4
	12	24	6	45	6
	16	26	8	49	8
	32	34	16	65	16
16	8	32	28	61	28
	12	38	44	73	44
	16	44	60	85	60
	32	68	124	133	124

* Fullwave gets stored.

Table 6: XCO Parameters and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and containing only characters from the following character set: a.. z, 0..9 and _	blank
theta_width	With distributed ROM option: integer in the range 3 to 10. With block ROM option: integer in the range 3 to 16	4
input_options	One of the following keywords: registered, non_registered	non_registered
output_width	Integer in the range 4 to 32	16
function	One of the following keywords: sine, cosine, sine_and_cosine,	sine
memory_type	One of the following keywords: dist_rom, block_rom	dist_rom
pipeline_stages	With distributed ROM option: integer in the range 0 to 3 With block ROM option: integer in the range 1 to 2	0
output_options	One of the following keywords: registered, non_registered	non_registered
negative_sine	One of the following keywords: true, false	false
negative_cosine	One of the following keywords: true, false	false
sclr_pin	One of the following keywords: true, false	false
aclr_pin	One of the following keywords: true, false	false
clock_enable	One of the following keywords: true, false	false
handshaking_enabled	One of the following keywords: true, false	false
create_rpm	One of the following keywords: true, false	false

Parameter Values in the XCO File

Names of XCO file parameters and their parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case insensitive.

Table 6 shows the XCO file parameters and values, as well as summarizing the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET function = Sine_and_Cosine
CSET aclr_pin = false
CSET component_name = my_sin_cosine_table
CSET output_options = Non_Registered
CSET pipeline_stages = 1
CSET memory_type = Block_ROM
CSET negative_sine = false
CSET input_options = Registered
CSET negative_cosine = false
CSET output_width = 4
CSET sclr_pin = false
CSET theta_input_width = 9
CSET clock_enable = true
CSET handshaking_enabled = true
CSET create_rpm = false
CSET aclr_pin = false
```

Ordering Information

This macro is downloadable free of charge from the Xilinx IP Center (www.xilinx.com/ipcenter) for use with 3.1i and later versions of the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative. Information on the Xilinx sales representative nearest you is available at http://www.xilinx.com/company/sales.htm.