Bit Multiplexer V3.0

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Features

- Drop-in module for Virtex™, Virtex™-E, Virtex™–II and Spartan™–II FPGAs
- 256:1 multiplexing range
- Optional registered output with optional clock enable and asynchronous and synchronous controls
- Optional pipelining of Bit Multiplexer, by the use of the latency control.
- Incorporates Xilinx Smart-IP technology for maximum performance
- To be used with version 3.1i and later of the Xilinx CORE Generator System

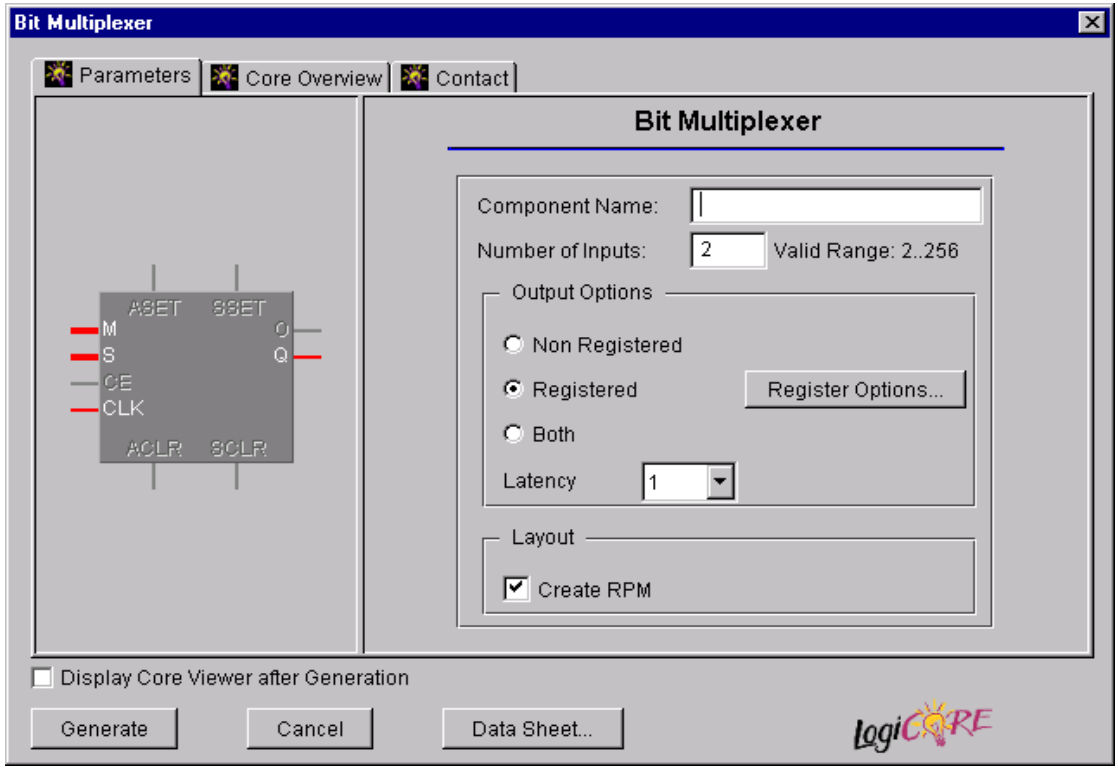

Figure 1: Main Bit Multiplexer Parameterization Screen

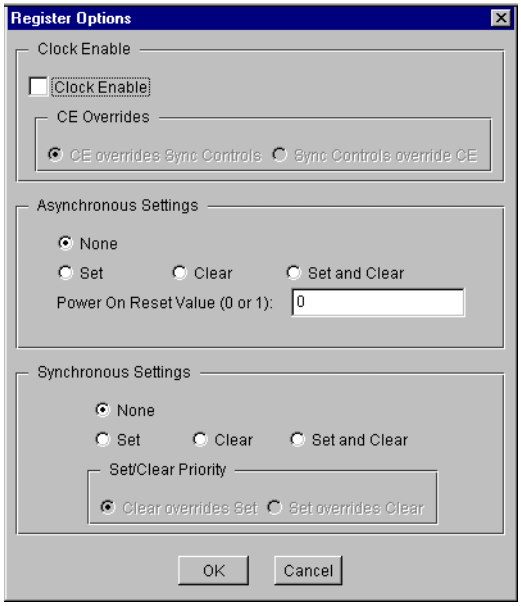

Figure 2: Bit Multiplexer Register Options Parameterization Screen

Functional Description

The Bit Multiplexer is a member of the BaseBLOX series of building blocks for the Virtex architecture. Options are provided for selecting the multiplexer size, registered outputs and non-registered outputs. When a registered output is selected, options are also provided for **Clock Enable**, **Asynchronous Set and Clear**, and **Synchronous Set and Clear.** The module can optionally be generated as a Relationally Placed Macro (RPM) or as unplaced logic. When an RPM is generated the logic is placed in a column.

Pinout

Signal names for this core are shown in Figure 3 and described in Table 1.

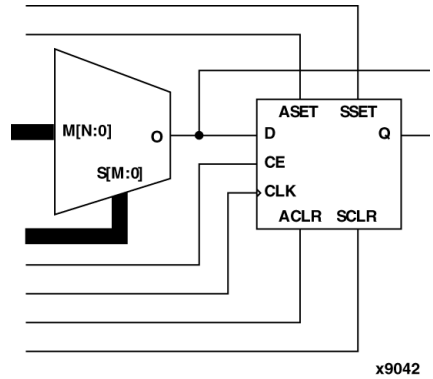

Figure 3: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
M[N:0]	Input	Multiplexer inputs
S[M:0]	Input	Binary encoded multiplexer select inputs where M = RoundUp(Log2n)
O	Output	Multiplexer output for non-registered module
D	Internal	Internal data input connection to optional output register
CE	Input	Clock Enable
CLK	Input	Clock: rising edge
ASET	Input	Asynchronous Set: forces the registered output to a high state when driven
ACLR	Input	Asynchronous Clear: forces outputs to a Low state when driven
SSET	Input	Synchronous Set: forces the registered output to a High state on next concurrent clock edge
SCLR	Input	Synchronous Clear: forces the registered output to a Low state on next concurrent clock edge.
Q	Output	Multiplexer output for registered module

Note:
All control inputs are Active High. Should an Active Low input be required for a particular control pin an inverter must be placed in the path to the pin. The inverter will be absorbed appropriately during mapping.

CORE Generator Parameters

The main CORE Generator parameterization screen for this module is shown in Figure 1. The parameters are as follows:

- **Component Name**: The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and "_".
- **Number of Inputs**: Enter the number of multiplexer inputs. The valid range is 2 to 256. The default value is 2.
- **Output Options**: Select the appropriate radio button for the types of outputs required.
- **Register Options**: This button is only enabled when a registered output has been requested via the Output Options. Clicking on this button brings up the Register Options parameterization screen (see figure 2).
- **Latency**: This control will allow the user to create a bit multiplexer, which is pipelined.
  The values that the Coregen GUI will allow latency to take depend on which output options have been selected.
  Nonregistered output : latency fixed at 0
  Both outputs : latency fixed at 1 (one output is registered, and the other is nonregistered)
  Registered output : Normally, this is set to 1. However, if the multiplexer is bigger than 8:1 in size, the user can select higher latency values.
  Mux in range 9:1 to 64:1 Latency 1 (registered output), or 2 (pipelined).
  Mux in range 65:1 to 256:1 Latency 1 (registered output), 2 (pipelined), or 3 (pipelined).
- **Create RPM**: When this box is checked the module is generated with relative location attributes attached. The resulting placement of the module is in a column with two bits per slice. The default operation is to create an RPM.
  Note that when a module is created as an RPM it is possible that one or more of the module dimensions may exceed those of the device being targeted. If this is the case, mapping errors will occur and the compilation process will fail. In this case the module should be re-generated with the **Create RPM** checkbox unchecked.

The Register Options parameterization screen for this module is shown in Figure 2. The parameters are as follows:

- **Clock Enable**: When this box is checked the module is generated with a clock enable input. The default setting is unchecked.
- **CE Overrides**: This parameter controls whether or not the SSET and SCLR inputs are qualified by CE. This parameter is only enabled when a **Clock Enable** input has been requested.

  When **CE Overrides Sync Controls** is selected an active level on any of the synchronous control inputs will only be acted upon when the CE pin is also Active. Note that this is not the way that the dedicated inputs on the flip-flop primitives work, and so setting the **CE Overrides** parameter to **CE Overrides Sync Controls** will force any synchronous control functionality to be implemented using logic in the Look Up Tables (LUTs) preceding the output register. This results in increased FPGA resource utilization.

  When **Sync Controls Override CE** is selected an active level on any of the synchronous control inputs is acted upon irrespective of the state of the CE pin. This setting allows the dedicated inputs on the flip-flop primitives to be used for the synchronous control functions provided that asynchronous controls are not requested. If both asynchronous and synchronous controls are requested, the synchronous control functionality must be implemented using logic in the LUTs preceding the output register. In this case, the CE input has to be gated with the synchronous control inputs so that each synchronous control input and the CE input can generate a CE signal to the flip-flops. This results in a performance degradation for the module due to the additional gating in the CE path.

  The default setting is **Sync Controls Override CE** so that a more efficient implementation can be generated.
- **Asynchronous Settings**: All asynchronous controls are implemented using the dedicated inputs on the flip-flop primitives. The module can be generated with the following asynchronous control inputs by clicking on the appropriate button:
  - **None**: No asynchronous control inputs. This is the default setting.
  - **Set**: An ASET control pin is generated.
  - **Clear**: An ACLR control pin is generated.
  - **Set and Clear**: Both ASET and ACLR control pins are generated. ACLR has priority over ASET when both are asserted at the same time.
- **Power On Reset Value**: This text box accepts a value of 0 or 1 and defines the power on value for the output register. The default value is 0.
- **Synchronous Settings**: When no asynchronous controls are requested (i.e. the **Asynchronous Setting** is **None**) the synchronous controls can be implemented using the dedicated inputs on the flip-flop primitives. There are exceptions to this which are described in the sections for the **Set/Clear Priority** and **CE Overrides** parameters.
  When asynchronous controls are present any synchronous control functionality must be implemented using logic in the Look Up Tables (LUTs) preceding the output register. With modules where a non-registered output is not required there are combinations of parameters that allow this logic to be absorbed into the same LUTs used

to implement the function. In cases where this absorption is not possible the synchronous control logic will require an additional LUT per output bit.

The module can be generated with the following synchronous control inputs by clicking on the appropriate button:

- **None**: No synchronous control inputs. This is the default setting.
- **Set**: An SSET control pin is generated.
- **Clear**: An SCLR control pin is generated.
- **Set and Clear**: Both SSET and SCLR control pins are generated. SCLR/SSET priority is defined by the setting of the **Set/Clear Priority** parameter.

- **Set/Clear Priority**: By selecting the appropriate radio button the relative priority of SCLR and SSET can be controlled. This parameter is only enabled when **Set and Clear** is selected for **Synchronous Settings**.

A setting of **Clear Overrides Set** corresponds to the native operation of the flip-flop primitive. This setting will result in a more efficient implementation when asynchronous controls are not requested. A setting of **Set Overrides Clear** can only be implemented using logic in the LUTs preceding the output register.

The default setting is **Clear Overrides Set** so that the dedicated inputs on the flip-flops can be used if available.

Parameter Values in the XCO File

Names of XCO file parameters and parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case sensitive.

Table 2 shows the XCO file parameters and values, as well as summarizing the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET component_name = abc123
CSET number_of_inputs = 2
CSET output_options = registered
CSET latency = 1
CSET create_rpm = TRUE
CSET clock_enable = FALSE
CSET ce_overrides = sync_controls_override_ce
CSET asynchronous_settings = none
CSET power_on_reset_value = 0
CSET synchronous_settings = none
CSET set_clear_priority = clear_overrides_set
```

Core Resource Utilization

For an accurate measure of the usage of primitives, slices, and CLBs for a particular point solution, check the **Display Core Viewer after Generation** checkbox in CORE Generator.

Ordering Information

This core is downloadable free of charge from the Xilinx IP Center (www.xilinx.com/ipcenter), for use with the Xilinx Core Generator System version 3.1i and later. The Core Generator System 3.1i tool is bundled with the Alliance 3.1i and Foundation 3.1i implementation tools.

To order Xilinx software contact your local Xilinx sales representative at www.xilinx.com/company/sales.htm.

Table 2: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a .. z, 0..9 and _	blank
number_of_inputs	Integer in the range 2 to 256	2
output_options	One of the following keywords: non_registered, registered, both	registered
latency	Integer in the range 0 to 3	0, non_registered output 1, both output 1, registered output (if number_of_inputs exceeds 8, then higher latencies can be selected).
create_rpm	One of the following keywords: true, false	true
clock_enable	One of the following keywords: true, false	false
ce_overrides	One of the following keywords: sync_controls_override_ce, ce_overrides_sync_controls	sync_controls_override_ce
asynchronous_settings	One of the following keywords: none, set, clear, set_and_clear	none
power_on_reset_value	0 or 1	0
synchronous_settings	One of the following keywords: none, set, clear, set_and_clear	none
set_clear_priority	One of the following keywords: clear_overrides_set or set_overrides_clear	clear_overrides_set