Direct Digital Synthesizer (DDS) V2.0

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Features

- Drop-in module for Virtex™, Virtex™-E, Spartan®-II FPGAs
- Sine, Cosine or quadrature outputs
- Look-up table can be allocated to distributed or block memory
- Sine/cosine table depths from 8 to 65536 samples
- 4-to-32 bit output sample precision
- High precision synthesizer with fine frequency resolution ($\Delta f = 0.02$ Hz @ fclk = 100 MHz, 32-bit phase accumulator)
- Optional phase offset capability so that several synthesizers with precisely controlled phase differences can be supported
- Simple fixed output frequency option
- Incorporates Xilinx Smart-IP technology for maximum performance
- To be used with version 3.1i or later of the Xilinx CORE Generator System

General Description

Direct digital synthesizers (DDS), or numerically controlled oscillators (NCO), are important components in many digital communication systems. Quadrature synthesizers are used for constructing digital down and up converters, demodulators, and implementing various types of modulation schemes, including PSK (phase shift keying), FSK (frequency shift keying), and MSK (minimum shift keying). A common method for digitally generating a complex or real valued sinusoid employs a look-up table scheme. The look-up table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table to the desired output waveform.

Typical applications of a DDS include

- Digital radios and modems
- Software-defined radios (SDR)
- Digital down/up converters for cellular and PCS base stations
- Waveform synthesis in digital phase locked loops
- Generating injection frequencies for analog mixers

Theory of Operation

A high-level view of the DDS Core is presented in Figure 1. The integrator (components D1 and A1) computes a phase slope that is mapped to a sinusoid (possibly complex) by the look-up table T1. The quantizer Q1, which is simply a slicer, accepts the high-precision phase angle $\Theta(n)$ and generates a lower precision representation of the angle denoted as $\Theta(n)$ in the figure. This value is presented to the address port of a look-up table that performs the mapping from phase-space to time.

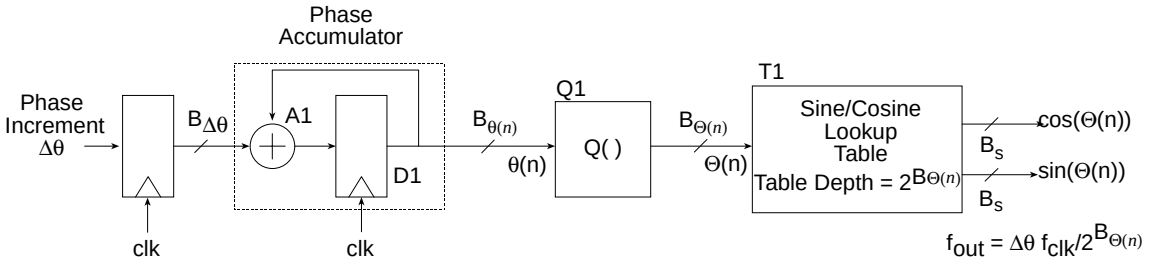

Figure 1: Phase truncation DDS. This is a simplified view of the DDS Core.

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal, and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum.

Direct digital synthesizers use an addressing scheme with an appropriate look-up table to form samples of an arbitrary frequency sinusoid. If an analog output is required, the DDS presents these samples to a digital-to-analog converter (DAC) and a low-pass filter to obtain an analog waveform with the specific frequency structure. Of course, the samples are also commonly used directly in the digital domain. The look-up table traditionally stores uniformly spaced samples of a cosine and a sine wave. These samples represent a single cycle of a length $N = 2^{B_{\Theta(n)}}$ prototype complex sinusoid and correspond to specific values of the sinusoid's argument $\Theta(n)$ as shown in Eq.(1).

$$\Theta(n) = n\frac{2\pi}{N} \tag{1}$$

where *n* is the time series sample index.

Quarter wave symmetry in the basis waveform can be exploited to construct a DDS that uses shortened tables. In this case, the two most significant bits of the quantized phase angle $\Theta(n)$ are used to perform quadrant mapping. This implementation results in a more area efficient implementation because the memory requirements are minimized – either fewer FPGA block RAMs or reduced distributed memory. Based on the Core customization parameters, the DDS core will automatically employ quarter-wave symmetry when appropriate[1].

Output Frequency

The output frequency, f_{out}, of the DDS waveform is a function of the system clock frequency f_{clk}, the number of bits $B_{\Theta(n)}$ used to address the sine/cosine lookup table and the phase increment value $\Delta\theta$. That is, $f_{out} = f\left(f_{clk}, B_{\Theta(n)}, \Delta\theta\right)$.

The output frequency in Hertz is defined as

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^{B_{\Theta(n)}}} \text{ Hz} \tag{2}$$

1. For very short tables, FPGA logic resources are actually minimized by storing a complete cycle. The user is not required to make any design decisions in this context – the Core Generator will always produce the smallest Core possible.

For example, if the DDS parameters are

$$\begin{aligned} f_{clk} &= 120 \text{ MHz} \\ B_{\Theta(n)} &= 10 \\ \Delta\theta &= 12_{10} \end{aligned} \tag{3}$$

the output frequency will be

$$\begin{aligned} f_{out} &= \frac{f_{clk}\Delta\theta}{2^{B_{\Theta(n)}}} \text{ Hz} \\ &= \frac{120\times10^6\times12}{2^{10}} \\ &= 1.406250 \text{ MHz} \end{aligned} \tag{4}$$

The phase increment value $\Delta\theta$ required to generate an output frequency f_{out} Hz is

$$\Delta\theta = \frac{f_{out}\,2^{B_{\Theta(n)}}}{f_{clk}} \tag{5}$$

Frequency Resolution

The frequency resolution Δf of the synthesizer is a function of the clock frequency and the number of bits $B_{\theta(n)}$ employed in the phase accumulator. The frequency resolution can be determined using the following equation

$$\Delta f = \frac{f_{clk}}{2^{B_{\theta(n)}}} \tag{6}$$

For example, for the DDS parameters

$$\begin{aligned} f_{clk} &= 120 \text{ MHz} \\ B_{\theta(n)} &= 32 \end{aligned} \tag{7}$$

the frequency resolution is

$$\begin{aligned} \Delta f &= \frac{f_{clk}}{2^{B_{\theta(n)}}} \\ &= \frac{120\times10^6}{2^{32}} \\ &= 0.0279396 \text{ Hz} \end{aligned} \tag{8}$$

Phase Increment

The phase increment term $\Delta\theta$ defines the synthesizer output frequency. Consider a DDS with the following parameterization

$$\begin{aligned} f_{clk} &= 100 \text{ MHz} \\ B_{\theta(n)} &= 28 \\ B_{\Theta} &= 12 \end{aligned} \tag{9}$$

To generate a sinusoid with frequency $f_{out} = 19$ MHz, the required phase increment would be

$$\begin{aligned}\Delta\theta &= \frac{f_{out}\, 2^{B_{\Theta(n)}}}{f_{clk}} \\ &= \frac{19\times10^6 \times 2^{12}}{100\times10^6} \\ &= 778.24\end{aligned} \tag{10}$$

Spectral Purity Considerations

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum.

In conjunction with the system clock frequency, the phase accumulator width determines the frequency resolution of the DDS. The accumulator must have a sufficient field width to span the desired frequency resolution. For most practical applications, a large number of bits are allocated to the phase accumulator in order to satisfy the system frequency resolution requirements. By way of example, if the required resolution is 1 Hz, and the clock frequency is 100 MHz, the required field width of the accumulator is

$$\begin{aligned}B_{\theta(n)} &= \log_2\left\lceil \frac{f_{clk}}{\Delta f} \right\rceil \\ &= \left\lceil \log_2 \frac{100\times10^6}{1} \right\rceil \\ &= \lceil 26.5754 \rceil \\ &= 27 \text{ bits}\end{aligned} \tag{11}$$

where $\lceil\ \rceil$ denotes the ceiling operator. Due to excessive memory requirements, the full precision of the phase accumulator cannot be used to index the sine/cosine look-up table. A quantized (or truncated) version of the phase angle is used for this purpose. The block labeled Q1 in Figure 1 performs the phase angle quantization. The lookup table can be located in block or distributed memory.

Quantizing the phase accumulator introduces time base jitter in the output waveform. As shown in Eq. (12), this jitter results in undesired phase modulation that is proportional to the quantization error.

$$\begin{aligned}\Theta(n) &= \theta(n) + \delta\theta(n) \\ e^{j\Theta(n)} &= e^{j[\theta(n)+\delta\theta(n)]} = e^{j\theta(n)} e^{j\delta\theta(n)} \\ e^{j\Theta(n)} &\approx e^{j\theta(n)}\left[1 + j\delta\theta(n)\right] \\ &\approx e^{j\theta(n)} + j\delta\theta(n) e^{j\theta(n)}\end{aligned} \tag{12}$$

Figure 2 shows the look-up table addressing error, complex output time-series and the spectral domain representation of the output waveform produced by the DDS structure shown in Figure 1. The normalized frequency for this signal is 0.022 Hz, which corresponds to phase accumulation steps of 7.92 degrees per output sample. The angular resolution of the 256-point look-up table is 360 / 256 or 1.40625 degrees per address, which is equivalent to 7.92 / 1.40625 or 7.0549 addresses per output sample. Since the address must be an integer, the fractional part is discarded and the resultant phase jitter is the cause of the spectral artifacts. Figure 3 provides an exploded view of the spectral plot in Figure 2(c).

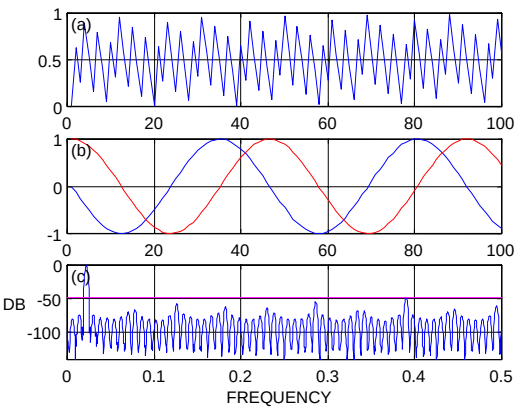

Figure 2: Phase truncation DDS. $f_{out} = 0.022$ **Hz, table depth = 256 12-bit precision samples. (a) Phase angle addressing error. (b) Complex output time series. (c) Output spectrum.**

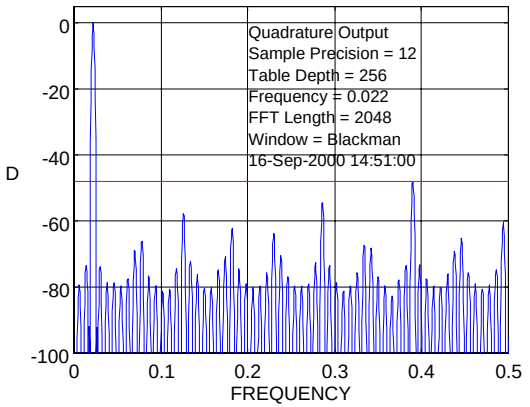

Figure 3: Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 12-bit precision samples. Exploded view of Figure 2(c).

We make two observations related to the phase jitter structure level. Observe that the fractional part of the address count is a periodic (sawtooth) error sequence which is responsible for the harmonic rich (and aliased) low-level phase modulation evident in Figure 3. We also note that the peak distortion level due to incidental phase modulation is approximately 48 dB below the desired signal level, which is consistent with 6 dB/bit of address space. Put another way, if *S* dB of spur suppression is required in the output waveform, as referenced to the 0 dB primary tone, the DDS lookup table must support at least $\lceil \log_2 S \rceil$ address bits. For example, if *S* = 70 dB, which means that the highest spur will be 70 dB below the main signal, then the minimum number of address bits for the lookup table is $\lceil \log_2 70 \rceil = 12$ bits, that is, a 4096-bit deep table.

Figure 4 and Figure 5 demonstrate the performance of a similar DDS to the one presented in Figure 2, but in this example 16-bit precision output samples have been used. Observe that the highest spur is still at the –48 dB level, and allocating 4 additional bits to the output samples has not contributed to any further spur reduction. For a phase truncation DDS, the only option to further reduce the spur levels is to increase the depth of the look-up table.

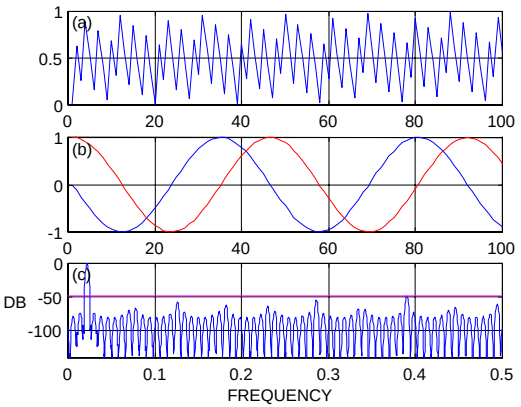

Figure 4: Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 16-bit precision samples. (a) Phase angle addressing error. (b) Complex output time series. (c) Output spectrum.

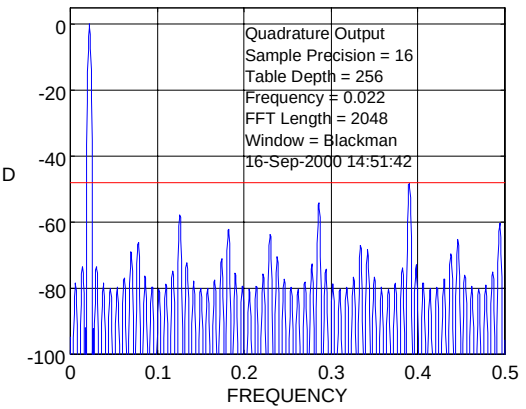

Figure 5: Phase truncation DDS. $f_{out} = 0.022$ Hz, table depth = 256 16-bit precision samples. Exploded view of Figure 4(c).

Further examples illustrating the performance of various DDS configurations are shown in Figure 6 through Figure 16. The configuration details are annotated on the plot. For some of these examples, the synthesized frequency has been swept across a small range of the available output bandwidth. For these cases, the sweep start frequency, stop frequency, frequency increment δf and the number of tones in the sweep interval (*Num Tones*) is indicated. The analysis transform length and window function applied to the output time series is also indicated on the plots.

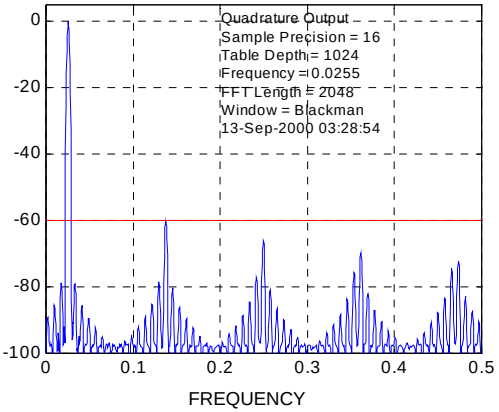

Figure 6:

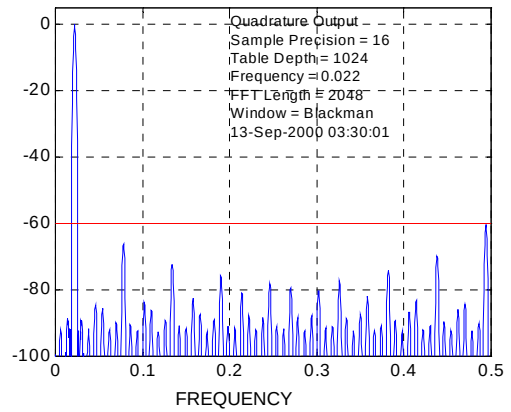

Figure 7:

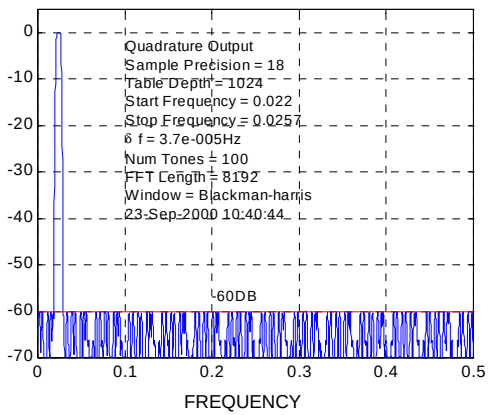

Figure 8:

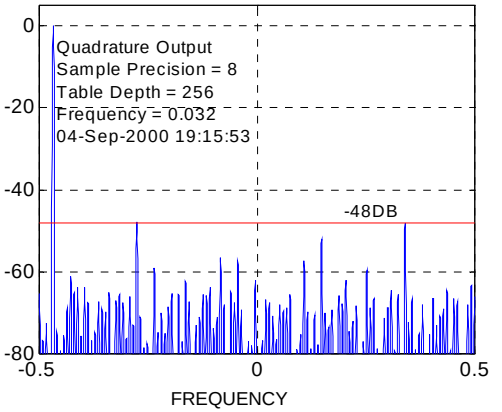

Figure 9:

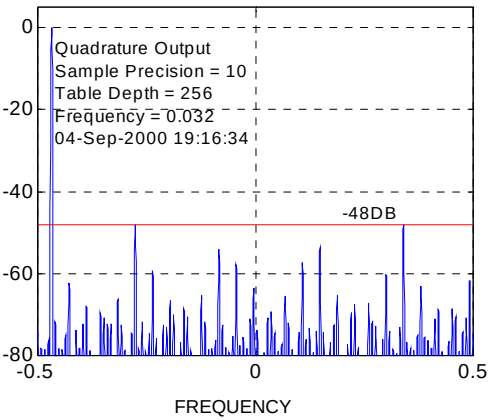

Figure 10:

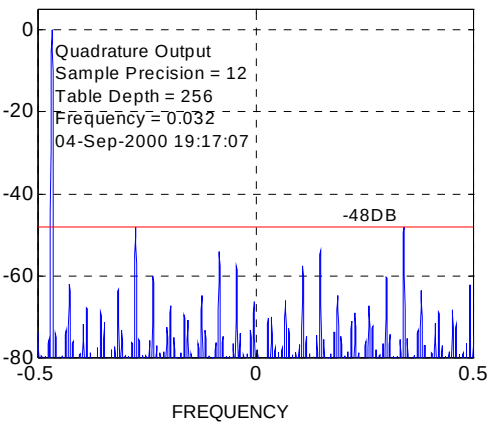

Figure 11:

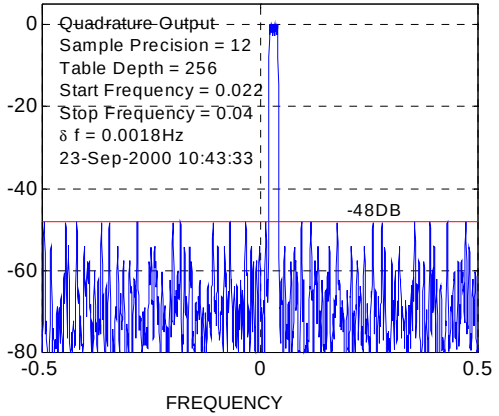

Figure 12:

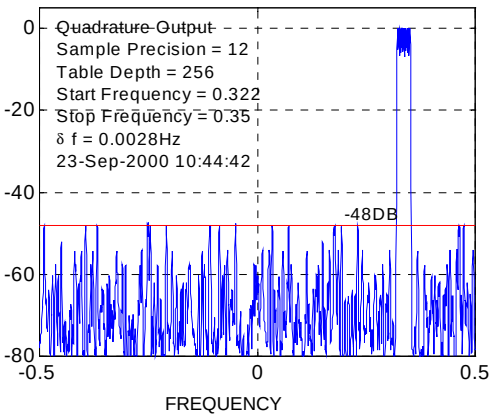

Figure 13:

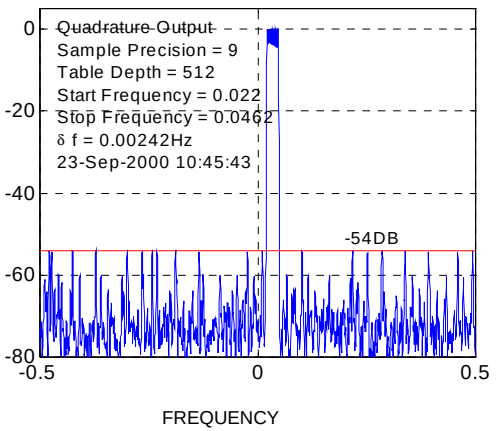

Figure 14:

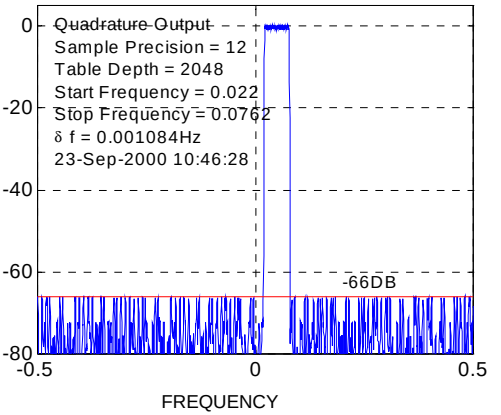

Figure 15:

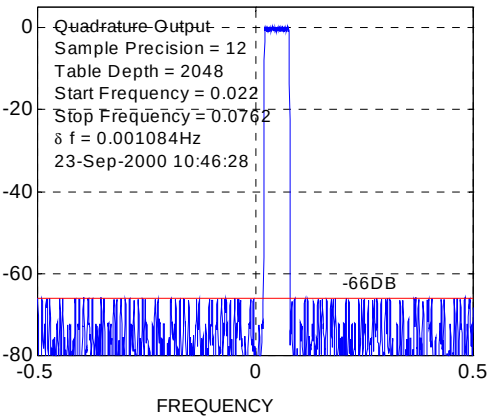

Figure 16:

Figure 1 provides a simplified view of the DDS core. A detailed view is shown in Figure 17. This detailed figure is similar to the simplified view, but also indicates the DDS control and interface *signals CE, A, WE, DATA, RFD* and *RDY*. Also note the inclusion of the *PHASE OFFSET* register designated *POFF*. This register is used for applying a constant phase offset to the phase slope computed in the phase accumulator *PACC*. When the Core is customized, the phase offset source can be defined as either a register, a constant, or it can be omitted entirely. When the *register* option is selected, the phase offset value is supplied via the *DATA* port. The phase offset value is treated as an unsigned quantity. If necessary, the phase offset is zero-extended before it is added to the phase accumulator.

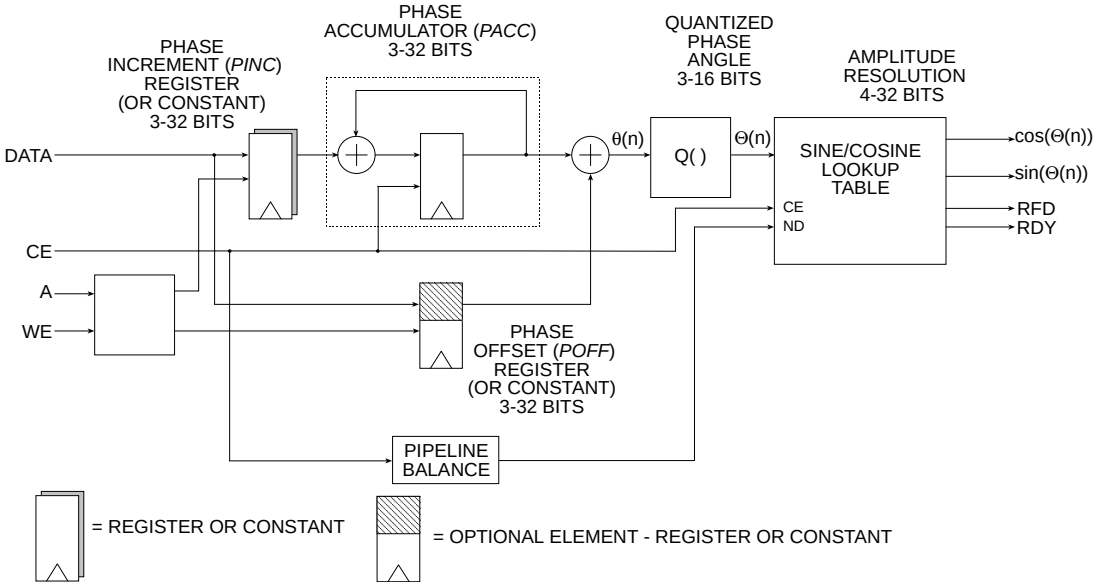

Figure 17: DDS Core—detailed view.

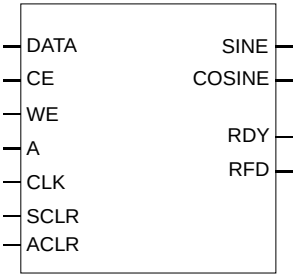

Figure 18: DDS Symbol

The phase increment value can be sourced from either a register or a constant. When the registered option is selected, the *DATA* port supplies the phase increment value to the phase increment register. When the *constant* option is selected, the DDS output frequency is fixed and cannot be adjusted once the Core is embedded in a design.

Table 1: DDS Core ports and definitions. † denotes optional pin

Signal Name	Direction	Description
CLK	Input	Master Clock (active rising edge)
A†	Input	Internal register address select. The *A* port selects either the *PINC* or *POFF* for a write operation. When *A*=0 the *PINC* register is selected. When *A*=1, the *POFF* register is selected.
WE†	Input	Write enable signal that enables a write operation to the *PINC* or *POFF* register. This is an active high signal that must be active to perform write operations to the *PINC* or *POFF* registers.
CE†	Input	Clock enable (active high). *CE* must be high during normal Core operation, but it is not required to be active during a write access to any internal registers.
DATA†	Input	Time shared data bus. The *DATA* port is used for supplying values to the *PINC* or *POFF* registers.

[2]Assuming this port is present

Table 1: DDS Core ports and definitions. † denotes optional pin (Cont.)

Signal Name	Direction	Description
ACLR†	Input	Asynchronous clear - active high. When *ACLR* is asserted, the all registers in the Core are cleared. *RDY* is also deasserted.
SCLR†	Input	Synchronous clear - active high. When *SCLR* is asserted, all registers in the Core are cleared. *RDY* is also deasserted.
RDY†	Output	Indicates when the output samples are available.
RFD†	Output	*RFD* is a dataflow control signal present on many Xilinx LogiCOREs. In the context of the DDS, it is supplied only for consistency with other LogiCores. This optional port is always tied to VCC.
SINE	Output	Sine time-series.
COSINE	Output	Cosine time-series.

Interface, Control and Timing

Figure 19 shows the timing sequence required to initialize and activate the DDS core. In this example, the DDS has both a phase increment *(PINC)* and a phase offset register *(POFF)*. The phase increment register is first initialized with the value 0x40. This is realized by supplying the phase increment value on the *DATA* port and selecting the *PINC* register by defining the address port as *A*=0. The write is performed on the positive clock edge. *WE* must be active; *i.e., WE*=1, to perform this operation. Immediately after the *PINC* register is loaded, the value 0x1 is written to the *POFF* register. This requires *A*=1 and *WE*=1. The register is loaded on the rising edge of the clock. *CE* does not have to be active to write to either the *PINC* or *POFF* registers. The DDS will start operating once the clock enable is applied (*CE*=1). Since *CE* is an optional pin, DDS configurations that do not include this pin will begin operating once the FPGA is configured and the system clock is active. After a start-up latency (measured from the assertion of *CE*[2]) that depends on the pipelining configuration chosen for the Core, in addition to the register configuration in the phase accumulator (*zero-cycle* latency or *one-cycle* latency), samples will be presented on the output port(s). This is indicated by *RDY*=1. For most configurations, the assertion by the Core of *RDY* indicates the first valid output sample. However, there is an exception. If a DDS is customized such that the *0-cycle* latency phase accumulator option is selected, and the sine-cosine look-up table is in distributed memory, and the table is purely combinatorial, any writes to the *PINC* register will be immediately reflected at the output port(s). This is irrespective of whether *CE* is asserted or not. In this situation, there are no registers between the *PINC* register and the output nodes, there is only a combinatorial arrangement of logic. Therefore, the *CE* pin cannot have any influence on this path through the system. The *CE* pin will, of course, still control the operation of the register (now in the upper arm of the phase accumulator shown in Figure 22(b)) in the *PACC*.

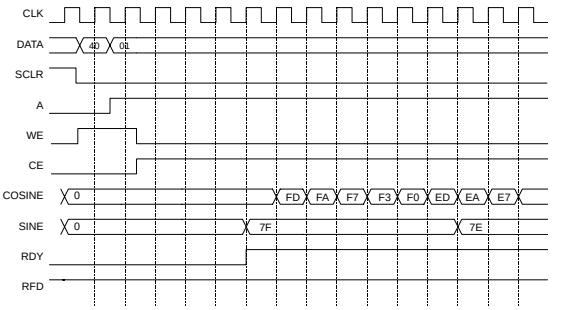

Figure 19: DDS timing.

The DDS can have an optional asynchronous clear or synchronous clear port. The option to simultaneously support both clear options is also provided. When either type of clear is applied, the Core will cease operation. This is indicated by the deassertion of the *RDY* output signal. The *SINE* and *COSINE* output ports will assume a value of 0. All internal registers will also be reset.

Parameters

The DDS parameterization screens are shown in Figure 20 and Figure 21.

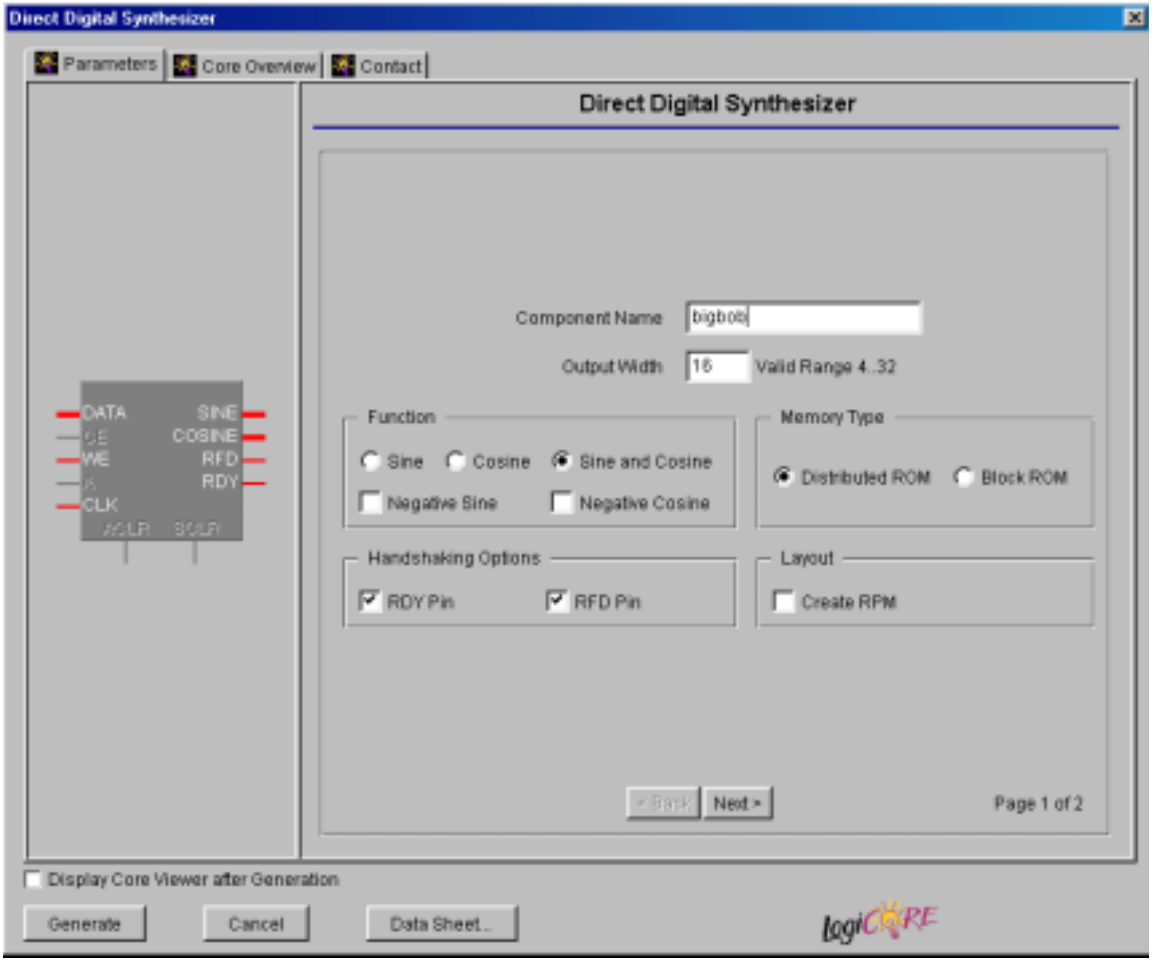

Figure 20: DDS parameterization screen - field 1.

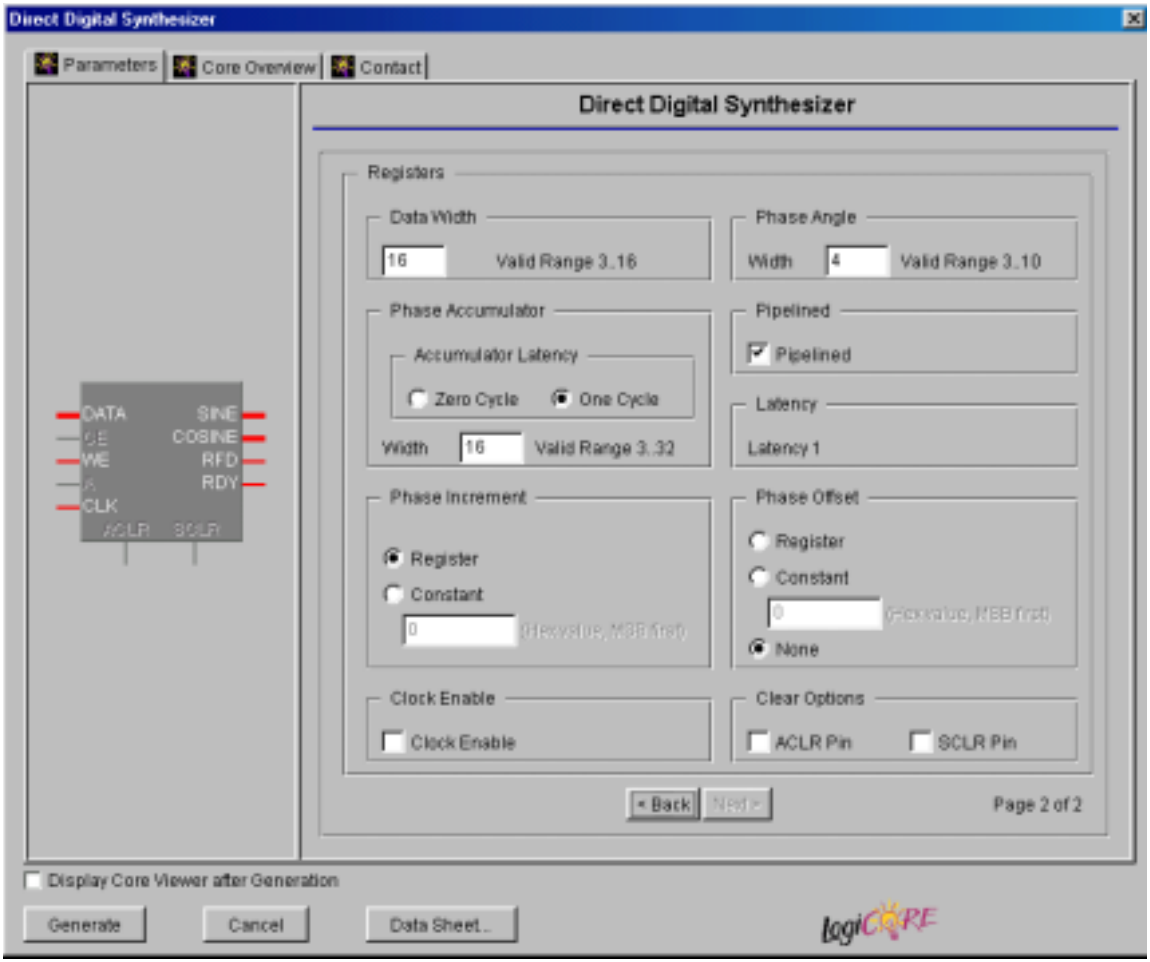

Figure 21: DDS parameterization screen - field 2.

The customization parameter definitions are:

- **Component Name:** The user-defined DDS component name.
- **Output Width:** The output precision of the *SINE* and *COSINE* outputs. Depending on the customization selection, only one of these ports might be present on a component. If both the sine and cosine components are present, the bit precision for each signal will be the same.
- **Function:** The DDS may have a quadrature output (sine and cosine), or a single output port — either sine or cosine. In addition, the sign of the output signal(s) can be defined using the *Negative Sine* and *Negative Cosine* checkboxes. For example, if the quadrature output option is selected (*Sine and Cosine* GUI option) and both the *Negative Sine* and *Negative Cosine* boxes are unchecked, then the output signal *s(n)* is

$$s(n) = e^{j\Theta(n)} = \cos\Theta(n) + j\sin\Theta(n) \quad (13)$$

If the Negative Sine box had been checked, the output signal is defined by

$$s(n) = e^{-j\Theta(n)} = \cos\Theta(n) - j\sin\Theta(n) \quad (14)$$

- **Memory Type:** This field controls the location of the DDS trigonometric lookup table. When the *Distributed ROM* is selected, the table is placed in distributed

memory. If the *Block ROM* option is selected, the table will be implemented using FPGA block memory.

- **Data Width:** The *Data Width* field defines the bit precision of the *DATA* port. This port sources the *PINC* and *POFF* registers.
- **Phase Offset:** The phase offset value shown in Figure 17 can be sourced from a register or it can be a constant that is defined when the Core is customized. This function can be completely omitted by selecting *None*. When the Register or Constant option is selected, the bit precision is determined by the *DATA* port. Using the *Register* option, the phase offset value can be changed on-line using the Core *DATA* port and associated control signals.

  If the *Constant* option is selected, the value in the textbox is used as the phase offset value. Just like the *Register* option, this is an unsigned value that, if necessary, is zero-extended before it is added to the high-precision phase angle supplied by the phase accumulator.

  The bit field range of the phase offset is always less than or equal to the precision carried by the phase accumulator.

- **Phase Increment:** The phase increment can be sourced from either a register or a constant. This is an unsigned value that, if necessary, is zero-extended before it is applied to the summing junction at the input of the phase accumulator. The phase increment value can be changed on-line using the Core *DATA* port and associated control signals.

  If the *Constant* option is employed, the value in the textbox will define the output frequency of a fixed-frequency synthesizer.

- **Phase Accumulator:** Phase accumulator precision. This field defines the precision of the *PACC* register (Figure 17). The location of the register in the phase accumulator is controlled by the latency selection options. When the *one-cycle* latency option is selected, the phase accumulator will be as shown in Figure 22(a). When the *zero-cycle* option is selected, the arrangement in Figure 22(b) is employed.

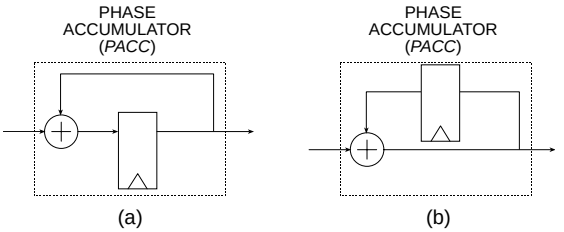

Figure 22: Register options for the phase accumulator - PACC.

- **Phase Angle:** This is the number of bits allocated to the quantized phase angle - $B_{\Theta(n)}$ in Figure 17. $B_{\Theta(n)}$ is the number of address bits used to address the sine/cosine lookup table. This value defines the depth of the lookup table.
- **Clock Enable:** The Core can have an optional clock enable port.
- **Handshaking Options:** Optional handshaking ports - *RDY* and *RFD* - can be included on the Core. The *RFD* output signal is simply tied to VCC and is an optional port that can be included for compatibility with other Xilinx LogiCores that employ this style of dataflow inferface. As shown in Figure 19, the *RDY* output signal identifies when valid sine/cosine samples appear on these ports after the Core is started from rest — either after system power-on or a reset (synchronous or asynchronous). Any type of Core reset will cause RDY to be removed (*RDY*=0).
- **Layout:** This checkbox controls whether a relationally placed MACRO (RPM) or a module with no placement information is generated. When checked, an RPM is produced. The RPM option is supported only for the distributed ROM implementation.

XCO File Parameters

The parameters supplied via the filter GUI are captured and logged to the *.xco* file. The full name of this file is simply the Component Name with an .xco file extension. Table 2 defines the *.xco* file parameter names and range specifications.

Table 2: XCO File Parameter Names, Definitions, and Range Specifications

Parameter Name	Definition	Range
BusFormat	Controls the notation employed for identifying buses in the output edif netlist file.	{BusFormatAngleBracket | BusFormatParen}
SimulationOutputProducts	Core HDL simulation selection — either VHDL or Verilog.	{VHDL | VERILOG}
ViewlogicLibraryAlias	Pathname to Viewlogic directory	Valid path name for the user's operating system.

Table 2: XCO File Parameter Names, Definitions, and Range Specifications (Cont.)

Parameter Name	Definition	Range
XilinxFamily	The FPGA target device family.	{Virtex | Spartan2}
DesignFlow	HDL flow specifier.	{VHDL | VERILOG}
FlowVendor	Design flow vendor information.	{Other | Synplicity | Exemplar | Synopsis | Foundation}
function	The DDS may be customized to provide a sine only output (*function=Sine*), cosine only output (*function=Cosine*) or both sine and cosine (quadrature) outputs (*function=Sine_and_Cosine*).	{Sine | Cosine | Sine_and Cosine}
data_width	The bit precision of the input *DATA* port. The *DATA* port is a time shared bus that is used for supplying values to the phase increment (*PINC*) and phase offset (*POFF*) registers. The maximum allowable number of bits for this port must be less than or equal to the field width defined for the phase accumulator (*PACC*). The field width of the *PINC* and *POFF* registers is inherited from the width of the *DATA* port.	[3,…,32]
phase_increment	The phase increment value, that is the delta phase increment supplied to the phase accumulator, may be sourced (by the *PACC*) from either a register (*phase_increment-=REG*) or it may be a constant (*phase_increment=Constant*).	{REG | Constant}
phase_increment_value	When *phase_increment=Constant* the DDS produces a fixed output frequency as defined by the *phase_increment_value*	Any hexadecimal value not to exceed the range supported by *data_width*
phase_offset	As shown in Figure 17 an optional phase offset can be introduced at the output of the phase accumulator. When *phase_offset=REG* this value is supplied by a register. When *phase_offset=Constant* the phase offset is a constant that is supplied by the *phase_offset_value* field when the Core is elaborated. If *phase_offset=None* no phase offset is included in the datapath.	{REG | Constant | None }
phase_offset_value	Initialization value for the phase offset constant. The field width of this value must be less than or equal to the number of bits specified for the phase accumulator. The field width of the phase offset value is always the same as that of the phase offset value.	[3,…,32]
accumulator_width	The field width for the phase accumulator (*PACC*).	[3,…,32]

Table 2: XCO File Parameter Names, Definitions, and Range Specifications (Cont.)

Parameter Name	Definition	Range
accumulator_latency	The user may control the position of the register in the phase accumulator. When *accumulator_register=ONE_CYCLE* the register location shown in Figure 22(a) is employed. When *accumulator_register=ZERO_CYCLE* the register location shown in Figure 22(b) is employed.	{ONE_CYCLE | ZERO_CYCLE}
phase_angle_width	This is the number of bits allocated to the quantized phase angle - $B_{\Theta(n)}$ in Figure 17. $B_{\Theta(n)}$ is the number of address bits used to address the sine/cosine lookup table. This value defines the depth of the lookup table.	[3,…,16]
aclr_pin	Asynchronous clear. When *aclr_pin=true* an asychronous reset port is included on the component. When *aclr_pin=false* the asychronous reset port suppressed.	{true | false}
component_name	Textbox that defines the DDS component name.	Any valid file name for the user's operating system consisting of the letters a…z, 0…9 and '_'. The component name may be a maximum of 32 characters.
pipelined	This parameter controls the degree of pipelining employed in the sine/cosine lookup table. When set to *true* the table is fully pipelined. When set to *false* the minimum (zero for the case of a distributed ROM) number of pipeline registers are used.	{true | false}
memory_type	The sine/cosine samples can be stored in distributed or block memory. When *memory_type=Block_ROM* the samples are stored in Block memory. When *memory_type=Distributed_ROM* distributed memory is used.	{Block_ROM | Distributed_ROM}
negative_sine	Only applicable if a sine port has been specified for the particular Core instance. When *negative_sine=false*, the signal presented at the *sine* port is sin $\theta(n)$. When negative_sine=true, the signal presented at the sine port is - sin $\theta(n)$.	{true | false}
negative_cosine	Only applicable if a cosine port has been specified for the particular Core instance. When *negative_cosine=false*, the signal presented at the *cosine* port is cos $\theta(n)$. When *negative_cosine=true*, the signal presented at the cosine port is - cos $\theta(n)$.	{true | false}
output_width	The output precision of the *SINE* and/or the *COSINE* output ports.	[4,…,32]

Table 2: XCO File Parameter Names, Definitions, and Range Specifications (Cont.)

Parameter Name	Definition	Range
sclr_pin	Synchronous clear. When *sclr_pin=true* a synchronous reset port is included on the component. When *sclr_pin=false* the sychronous re reset port suppressed.	{true | false}
clock_enable	Clock enable. When *ce_enable=true* a clock enable port is included on the component. When *clock_enable=false* the clock enable port suppressed.	{true | false}
rdy_pin	When *rdy_pin=true* the DDS Core includes a *RDY* output signal. If *rdy_pin=false* the *RDY* port is suppressed.	{true | false}
rfd_pin	When *rfd_pin=true* the DDS Core includes a *RFD* output signal. If *rfd_pin=false* the *RFD* port is suppressed.	{true | false}
create_rpm	When *create_rpm=true* a Core with embedded physical placement information is generated. If *create_rpm=false* the Core is generated without placement data.	{true | false}

Figure 23 is an example .xco file.

```
# Xilinx CORE Generator 3.1i
# Username = rslous
# COREGenPath = c:\visualcafe\projects
# ProjectPath = H:\newcore
# ExpandedProjectPath = H:\newcore
SET BusFormat = BusFormatParen
SET SimulationOutputProducts = VHDL
SET ViewlogicLibraryAlias = primary
SET XilinxFamily = Virtex
SET DesignFlow = VHDL
SET FlowVendor = Synplicity
SELECT Direct_Digital_Synthesizer Virtex Xilinx,_Inc. 2.0
CSET rdy_pin = true
CSET aclr_pin = false
CSET phase_increment = Register
CSET latency = One_Cycle
CSET component_name = test
CSET data_width = 16
CSET rfd_pin = true
CSET pipelined = true
CSET outputs_required = Sine_and_Cosine
CSET phase_offset = None
CSET memory_type = Distributed_ROM
CSET negative_sine = false
CSET accumulator_width = 16
CSET phase_angle_width = 4
CSET negative_cosine = false
CSET output_width = 16
CSET sclr_pin = false
CSET clock_enable = false
CSET phase_increment_value = 0
CSET phase_offset_value = 0
CSET create_rpm = true
GENERATE
```

Figure 23: Example DDS .xco file.

DDS Design Example 1

Consider a DDS that is to satisfy the following requirements

frequency resolution $\Delta f = 0.25$ Hz

minimum spur suppression $S = 70$ dB

$f_{\text{clk}} = 120$ MHz

Quarature output: $s(n) = e^{-j(\Theta(n)+\phi)} \cos(\Theta(n)+\phi) - \sin(\Theta(n)+\phi))$

where the phase offset $\phi = +\pi/4$ radians

The field width of the phase accumulator (PACC in Figure 17) defines the DDS frequency resolution according to

$$\Delta f = \frac{f_{\text{clk}}}{2^{B_{\theta(n)}}} \tag{15}$$

Therefore, the bit-precision for the PACC register is

$$\begin{aligned} B_{\theta(n)} &= \log_2\left\lceil \frac{f_{\text{clk}}}{\Delta f} \right\rceil \\ &= \left\lceil \log_2 \frac{120\times 10^6}{0.25} \right\rceil \\ &= \lceil 28.838459 \rceil \\ &= 29 \text{ bits} \end{aligned} \tag{16}$$

The spur suppression requirement is the dominant consideration when selecting the depth of the sine/cosine lookup table. Of course, the table samples must be specified with an appropriate precision to support this value. As noted in an earlier section of this document, each sine/cosine table address bit contributes approximately 6 dB of spur suppression. To meet the -70 dB spur level, the number of address bits required is

$$B_{\Theta(n)} = \left\lceil \log_2 \frac{70}{6} \right\rceil = \lceil 11.666\dot{} \rceil = 12 \text{ bits} \quad (17)$$

The table depth *N* is

$$N = 2^{B_{\Theta(n)}} = 2^{12} = 4096 \text{ samples} \quad (18)$$

The phase offset value *POFF* is determined as

$$\text{POFF} = N\frac{\phi}{360} = 4096\frac{45}{360} = 512_{10} \quad (19)$$

To generate a 10.2 MHz output signal the phase increment would be

$$\Delta\theta = \frac{f_{\text{out}} 2^{B_{\Theta(n)}}}{f_{\text{clk}}} = \frac{10.2\times10^6 \times 2^{12}}{120\times10^6} = 348.16 \quad (20)$$

This value must be expressed in the same format as the phase accumulator. The phase accumulator is a 29-bit word. Of these bits, the top 12 are interpreted as the integer field and the bottom 17 as the fractional component. That is, a 12.17 number. The phase increment value is therefore $\Delta\theta = 000101011100.00101000111101100_2$.

Figure 24 is a spectral plot of the 10.2 MHz output signal. Observe that the highest spur meets the 70 dB spur suppression requirement.

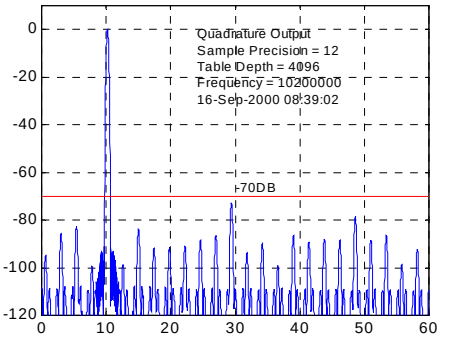

Figure 24: DDS example 1. 10.2 MHz output tone. The highest spur is below the required 70 dB suppression value.

DDS Design Example 2

Consider a DDS that is to satisfy the following requirements

frequency resolution $\Delta f = 0.3$ Hz
minimum spur suppression $S = 58$ dB
$f_{\text{clk}} = 80$ MHz
Quarature output: $s(n) = e^{-j(\Theta(n)+\phi)} \cos(\Theta(n)+\phi) - \sin(\Theta(n)+\phi))$
where the phase offset ϕ = -50 degrees

The field width of the phase accumulator (PACC in Figure 17) defines the DDS frequency resolution according to

$$\Delta f = \frac{f_{\text{clk}}}{2^{B_{\theta(n)}}} \quad (21)$$

Therefore, the bit-precision for the PACC register is

$$B_{\theta(n)} = \log_2 \left\lceil \frac{f_{\text{clk}}}{\Delta f} \right\rceil = \left\lceil \log_2 \frac{80\times10^6}{0.3} \right\rceil = \lceil 27.99046 \rceil = 28 \text{ bits} \quad (22)$$

The spur suppression requirement is the dominant consideration when selecting the depth of the sine/cosine look-up table. Of course, the table samples must be specified with an appropriate precision to support this value. As noted in an earlier section of this document, each sine/cosine table address bit contributes approximately 6 dB of spur suppression. To meet the -58 dB spur level, the number of address bits required is

$$B_{\Theta(n)} = \left\lceil \log_2 \frac{58}{6} \right\rceil = \lceil 9.666\dot{6} \rceil = 10 \text{ bits} \quad (23)$$

The table depth *N* is

$$N = 2^{B_{\Theta(n)}} = 2^{10} = 1024 \text{ samples} \quad (24)$$

In this example the required phase offset has been specified as a negative value. The DDS Core supports only positive phase offsets. This is, of course, not a problem because a phase angle of -50 degrees is the same as +315 degrees.

The phase offset value *POFF* is determined as

$$\text{POFF} = N\frac{\phi}{360} = 1024\frac{315}{360} = 896_{10} \quad (25)$$

To generate an 8.4 MHz output signal, the phase increment would be

$$\Delta\theta = \frac{f_{\text{out}} 2^{B_{\Theta(n)}}}{f_{\text{clk}}} = \frac{8.4\times10^6 \times 2^{10}}{80\times10^6} = 107.52 \quad (26)$$

This value must be expressed in the same format as the phase accumulator. The phase accumulator is a 28-bit word. Of these bits, the top 10 are interpreted as the integer field and the bottom 18 as the fractional component. That is, a 10.18 number. The phase increment value is therefore $\Delta\theta = 0001000111.101011100001010010_2$.

Figure 25 is a spectral plot of the 8.4 MHz output signal. Observe that the highest spur meets the 58 dB spur suppression requirement.

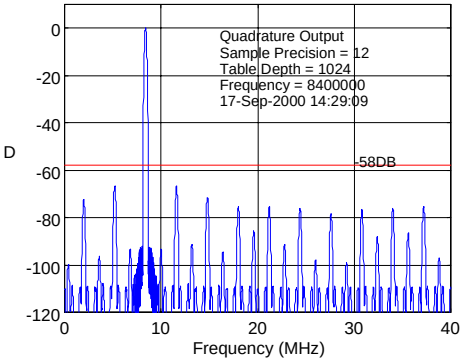

Figure 25: DDS example 2. 8.4 MHz output tone. The highest spur is below the required 58 dB suppression value.